A TECHNICAL REPORT ON SAMPLER SUBSYSTEM (FOR MARK IV B (SECOND SIDEBAND) CORRELATOR)

PREPARED BY
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UNDER THE GUIDANCE OF
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I am obliged to Dr. Yashwant Gupta and Mr. D. Anish Roshi for giving me opportunity to work on Sampler Subsystem.

Also, I sincerely thank Mr. Burse M.P., Mr. Bhonde I.S. and Mr. Irappa Halagali for their help and co-operation.

ANALOG TO DIGITAL CONVERSION

The analog signal can be given as either a voltage signal or current signal, depending on the signal source. The output of converter is an n-bit digital code given as,

$$D = A_{sig} / FS = b_n / 2^n + b_{n-1} / 2^{n-1} + \ldots + b_1/2^1$$

where A_{sig} is the analog signal, FS is the analog full scale level, and b_n is a digital value of either 0 or 1.

The *resolution* of a converter is defined as the smallest distinct change that can be resolved (produced) at an analog input (output) for an A/D (D/A) converter. This can be expressed as,

$$\Delta A_{sig} = FS / 2^N$$

where ΔA_{sig} is the smallest reproducible analog signal for an N-bit converter with full scale analog signal of FS.

The *accuracy* of a converter, often referred to also as *relative accuracy*, is the worst - case error between the actual and the ideal converter output after gain and offset errors are removed . This can be quantified as the number of equivalent bits of resolution or as a fraction of an LSB.

The *conversion rate* specifies the rate at which a digital code (analog signal) can be accurately converted into an analog signal (digital code). Accuracy is often expressed as a function of conversion rate and the two are closely linked. The conversion rate is often an underlying factor in choosing the converter architecture. The speed and accuracy of analog components are a limiting factor. Sensitive analog operations can either be done in parallel, at the expence of accuracy, or cyclically reused to allow high accuracy with lower conversion speeds.

Analog signals are continuous in time and continuous in amplitude, existing at every instant of time with any possible intermediate amplitude values. DSPs mathematically process signals represented as a series of numbers that are discrete in time and discrete in amplitude. A/D conversion consists of sampling, hold, quantize and code. Sometimes these four functions are integrated into one device.(Fig.5.)

SAMPLING :-

Sampling converts a signal that is continuous in time to one that is discrete in time. The number of samples taken per second is called the sampling rate or sampling frequency Fs. The Nyquist theorem states that , if sampling is performed at a rate exceeding the Nyquist rate, or 2 times the bandwidth of the signal, no signal information is lost .

HOLD AND QUANTIZE :-

After sampling, the signal is discrete in time but it is still continuous in amplitude. The signal is made discrete in amplitude as well by quantizing or representing each sample as a number with finite resolution. For example, this can be accomplished with a series of comparators. A hold function may be used to maintain the sampled value constant during the time it takes to quantize the signal.

Some of the techniques for quantizing include: *successive approximation* , *integration* and *flash*. Successive approximation converters use a D/A converter, comparator and control logic to perform a binary search for the digital value that is as close as possible to the input value. Integration -type converters use a ramp and a comparator to start and stop a digital counter whose output represents the value of the sample. These are relatively slow techniques, so these converters are primarily used for data rather than signal acquisition. Flash converters use a bank of comparators and voltage references , one for each quantization level. This converter is fast and is often used for signal acquisition. However, the number of comparators required rises exponentially with the number of output bits.

Unlike Nyquist sampling, which loses no information, quantizing produces an error called *quantizing noise*. Because the hardware cannot process an infinite number of bits, the amplitude of the signal cannot be represented with infinite resolution. The difference between the exact sample and value and the quantized value is *quantizing error*.

CODING :--

Coding is the representation of the quantized values in a perticular numerical format usually a form of binary. Straight binary is the natural choice for unipolar signals. The various codes used for bipolar signals differ in their representation of the sign and the transition from positive to negative values.

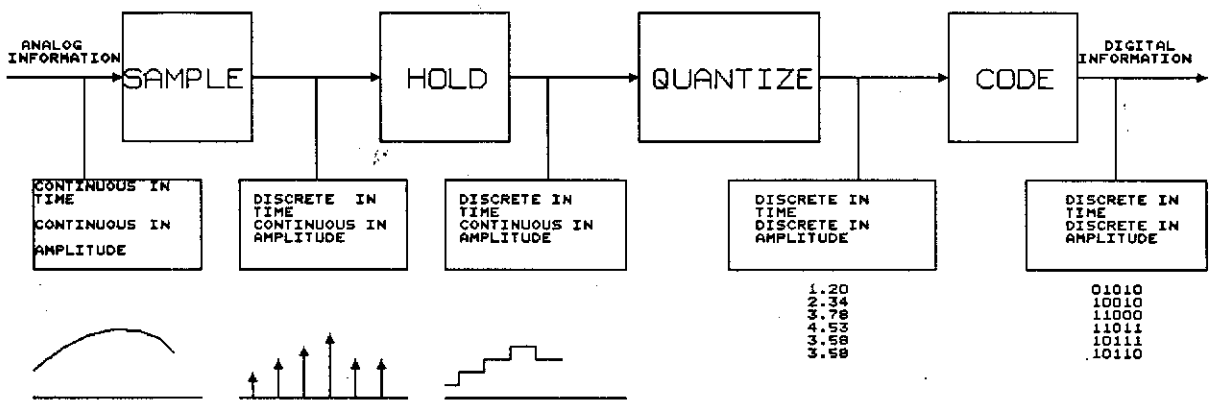

Fig.5 Analog To Digital Conversion

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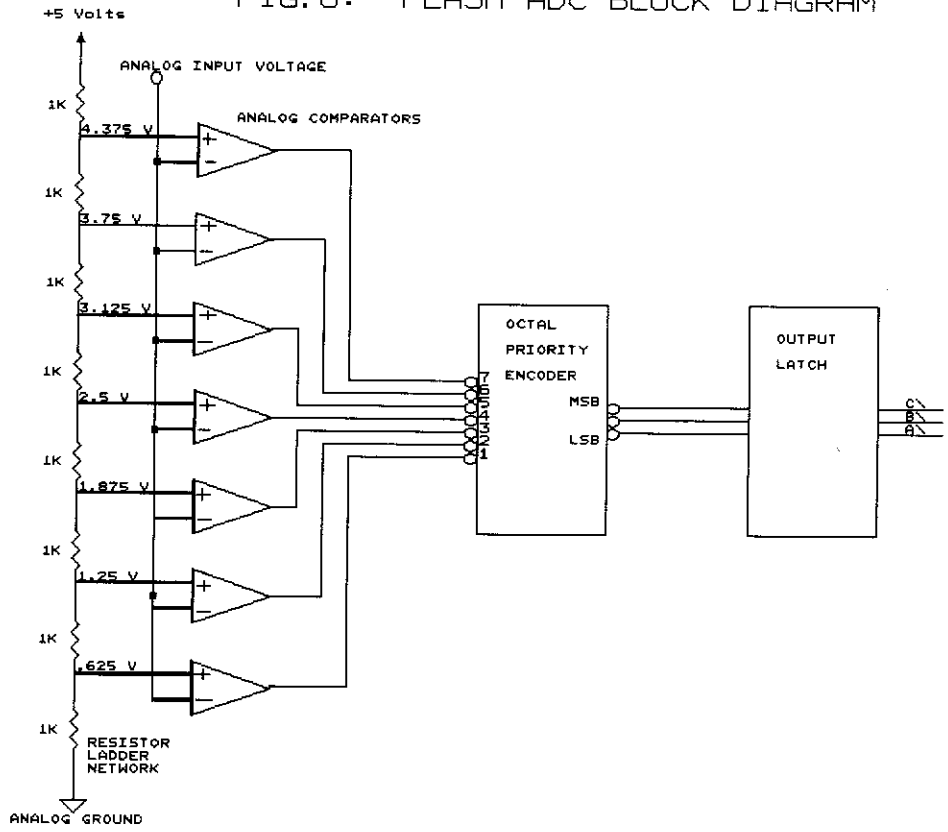
FLASH ANALOG TO DIGITAL CONVERTER

Parallel or flash ADC is used in high speed applications such as Video signal processing, medical imaging and radar detection systems. A flash ADC simultaneously compares the input analog voltage to 2^{n-1} threshold voltages to produce an n-bit digital code representing the analog voltage. Typical flash ADC with 8-bit resolution operate at 20-100MHz. The functional block diagram of flash ADC is shown in Fig.6. The circuitry consists of a precision resistor ladder network , 2^{n-1} analog comparators and a digital priority encoder. The resistor network establishes threshold voltages for each allowed quintization level. The analog comparators indicate whether or not the input voltage is above or below the threshold at each level. The output of the analog comparators is input to the digital priority encoder. The priority encoder produces the final digital output code that is stored in an output latch.

An 8 -bit flash ADC requires 255 comparators. The cost of high-resolution A/D comparaters escalates as the circuit complexity increases and as the number of analog converters rises by 2^{n-1} . As a low cost alternative, some manufacturers produce modified flash ADCs that perform the A/D conversion in two steps to reduce the amount of circuitry required. These modified flash ADCs are also called 'Half Flash ADCs' since they perform only half of the conversion simultaneously.

Flash A/D converters have conversion times ranging typically from 10 to 50ns. Flash ADC techniques enables these ICs to be used in many specialized high-speed data acquisition applications such as TV video digitizing (encoding), radar analysis, transient analysis, high speed digital oscilloscopes, medical ultrasound imaging, high -energy physics and robotic vision applications.

FIG.6: FLASH ADC BLOCK DIAGRAM



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SAMPLER

SAMPLER :

It is the front-end of the Correlator system. It performs the task of digitizing the analog signals. There are no user definable parameters for this subsystem. Hence ,there is no control system for the ADC subsystem.

THE ADC SUBSYSTEM :

The subsystem consists of the ADC cards and the backplane.

ADC CARDS INTERNAL MODULES :

A. The Amplifier Section

B. Ref. Generation Circuit

C. The ADC Chip

D. Protection Circuitry

E. Digital Section

F. Power Supply

A] THE AMPLIFIER SECTION :

Each ADC card accepts two inputs from the baseband system at 0dBm power level. These zero-mean signals are AC coupled to the amplifier circuit realized using AD9617 opamps configured as non-inv amplifier, it has a gain of 1.5. This value was chosen such that a 6σ signal would occupy the ± 1V (2 V peak- to -peak) voltage range of the ADC. The AD9617 is a current feedback amplifier. It provides fast settling , very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. It has input offset voltage of 500uV.

B] REF. GENERATION CIRCUIT :

The external ref. generation circuit was designed around the Analog devices two terminal ref. AD589. The AD589 is a two terminal , low cost temperature compensated voltage reference. The AD589 serves as a low cost precision ref. to a circuit which uses the AD708 dual op-amp with the matched pair transistors LM3904 and LM3906. The transistors drive the ref. ladder of the ADC. The loop thus established ensures stable ref. voltage inspite of the changes in the ladder impedance from one ADC to another.

C] THE ADC CHIP :

The Analog devices AD9058, a dual 8-bit 50MHz ADC forms the core of the ADC card. The two devices can be operated independently with separate analog inputs , voltage references and clocks. Analog input range is established by the voltages applied at the voltage reference inputs ($+V_{REF}$ and $-V_{REF}$). The AD9058 can operate from 0 V to +2 V (unipolar positive operation) using the internal voltage reference, or anywhere between -1 V and +2 V (bipolar operation) using external references. Input range is limited to 2 V p-p when using external references. In sampler external ref. is used .

D] PROTECTION CIRCUITRY :

A protection circuitry was needed to restrict the max. input voltage to the ADC to the rated specification of the AD9058 . A simple circuit was devised using PIN diodes to restrict voltages to within ±1.2V.

E] DIGITAL SECTION :

This section contains latches (74F574) for the ADC output ,TTL to ECL (MC10124) converters for data and ECL to TTL (MC10125) converter for the clock. The clock is converted to TTL levels and given to the ADC chip. An inverted version of this clock is given to the latches which receive the digitized data from the ADC. The inversion of the clock provides sufficient time for the ADC output to stabilize at the latch input .The latch output are given to the TTL to ECL converters which then transmit the data to the delay subsystem.

F] POWER SUPPLY :

The ADC card requires ±5V for both analog and digital sections. These are derived by using on-board voltage regulators which are fed by the linear power supplies.

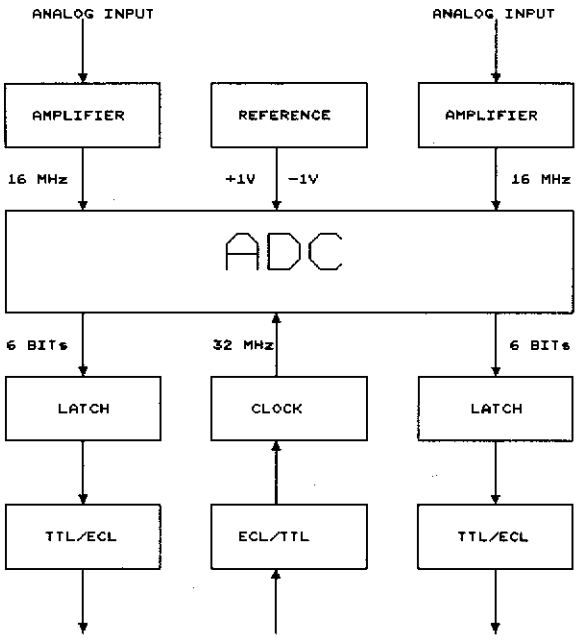

FIG. THE ADC CARD : BLOCK DIAGRAM

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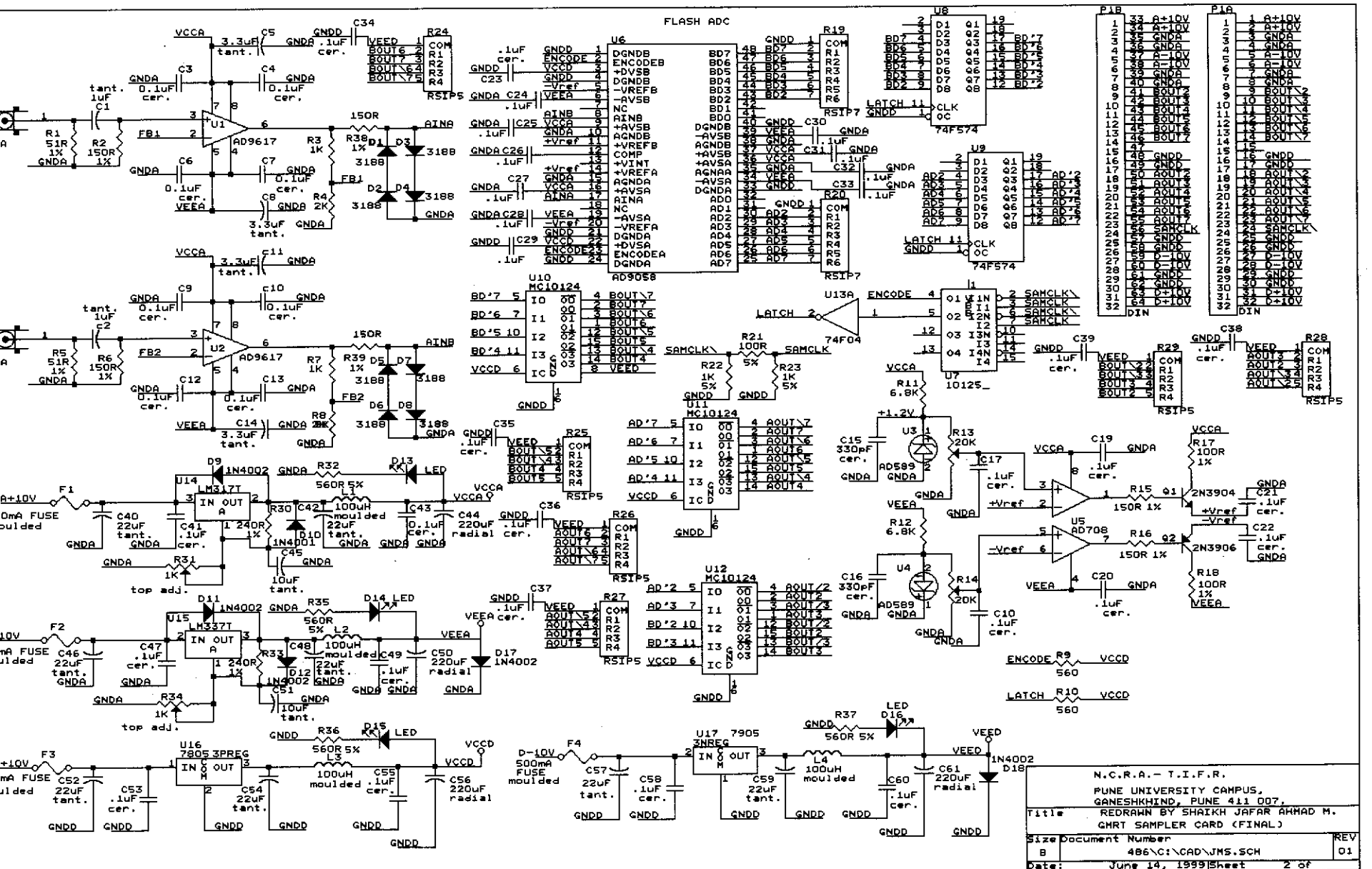
FLASH ADC
U6
AD9058
U1
AD9617
U2
AD9617
U10
MC10124
U11
MC10124
U12
MC10124
U8
74F574
U9
74F574
U7
10125_
U13A
74F04
U14
LM317T
U15
LM337T
U16
7805 3PREG
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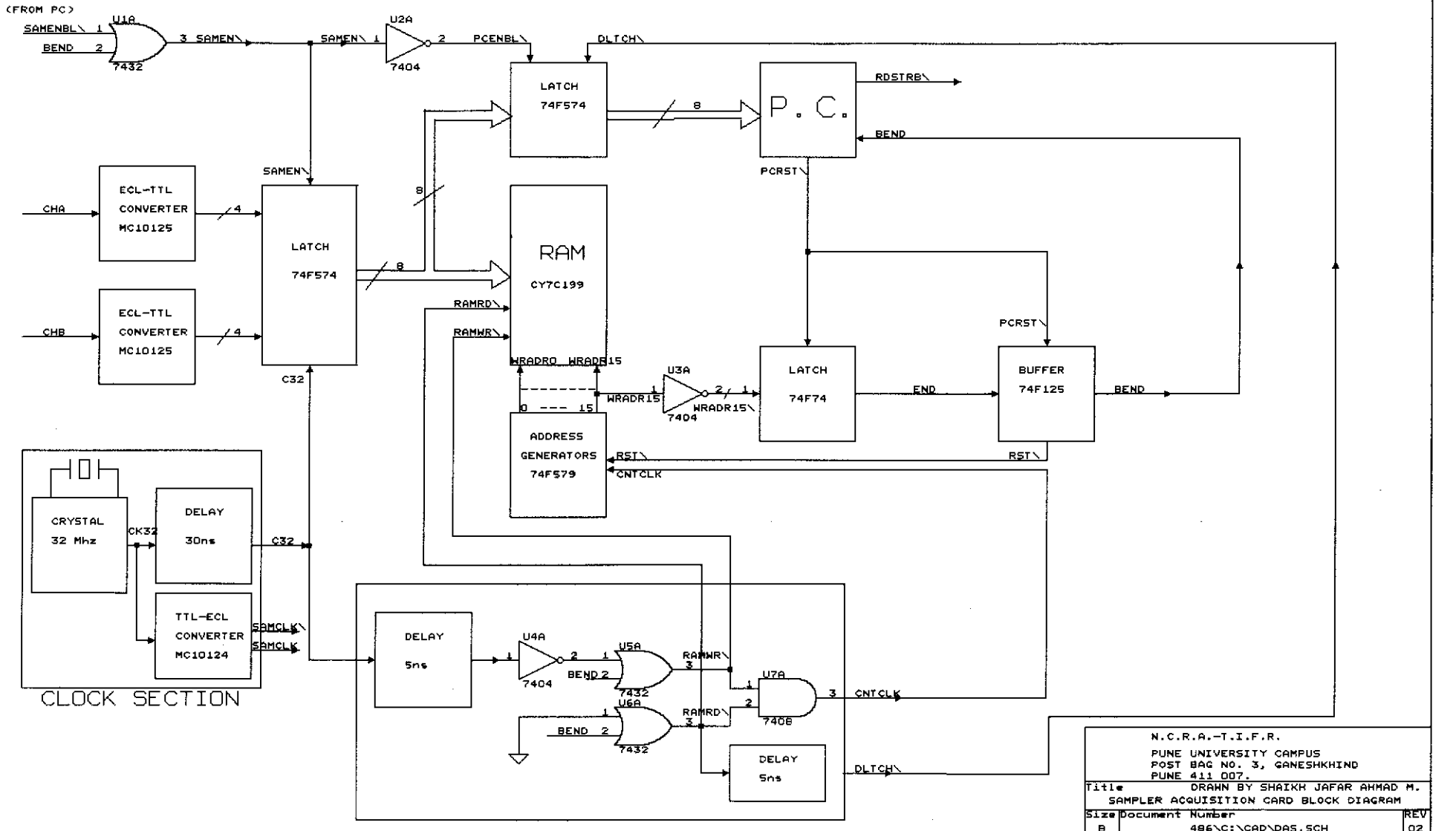
SAMPLER ACQUISITION CARD BLOCK DIAGRAM



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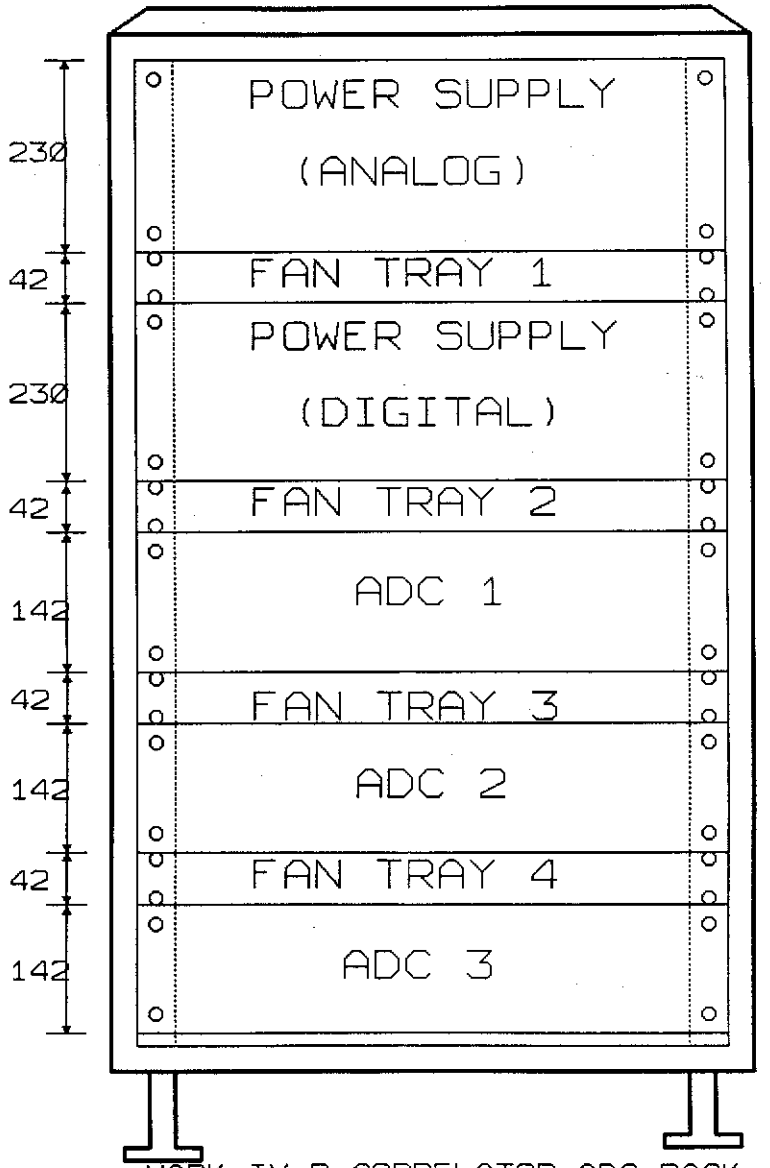

MARK IV B CORRELATOR ADC RACK.

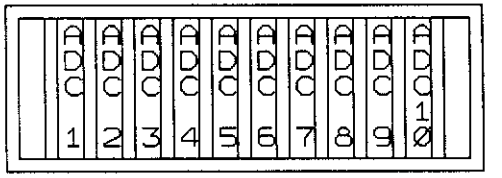

Fig. THE ADC SUBRACK

CFM : Cubic Foot per Minute

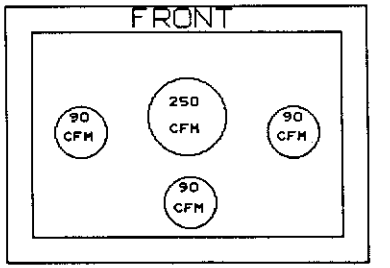

Fig. Layout of fans in the rack top

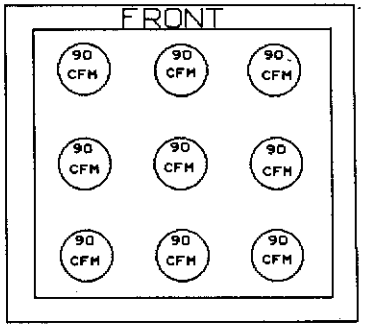

Fig. Layout of fans in the fan tray 1&2

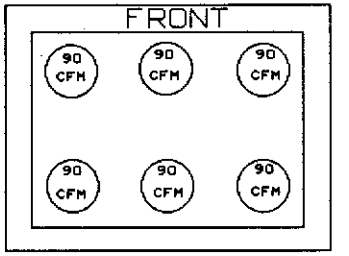

Fig. Layout of fans in the fan tray 3&4

All dimensions are in mm.

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SAMPLER TEST BENCH

Apparatus Required : 1) Sampler Bin
2) Data Acquisition System Card
3) Signal Generator
4) P.C.
5) Power Supply

Signal Generator Specifications : Marconi Instruments (PU 48)
10 KHz - 2.7GHz Signal Generator 2041

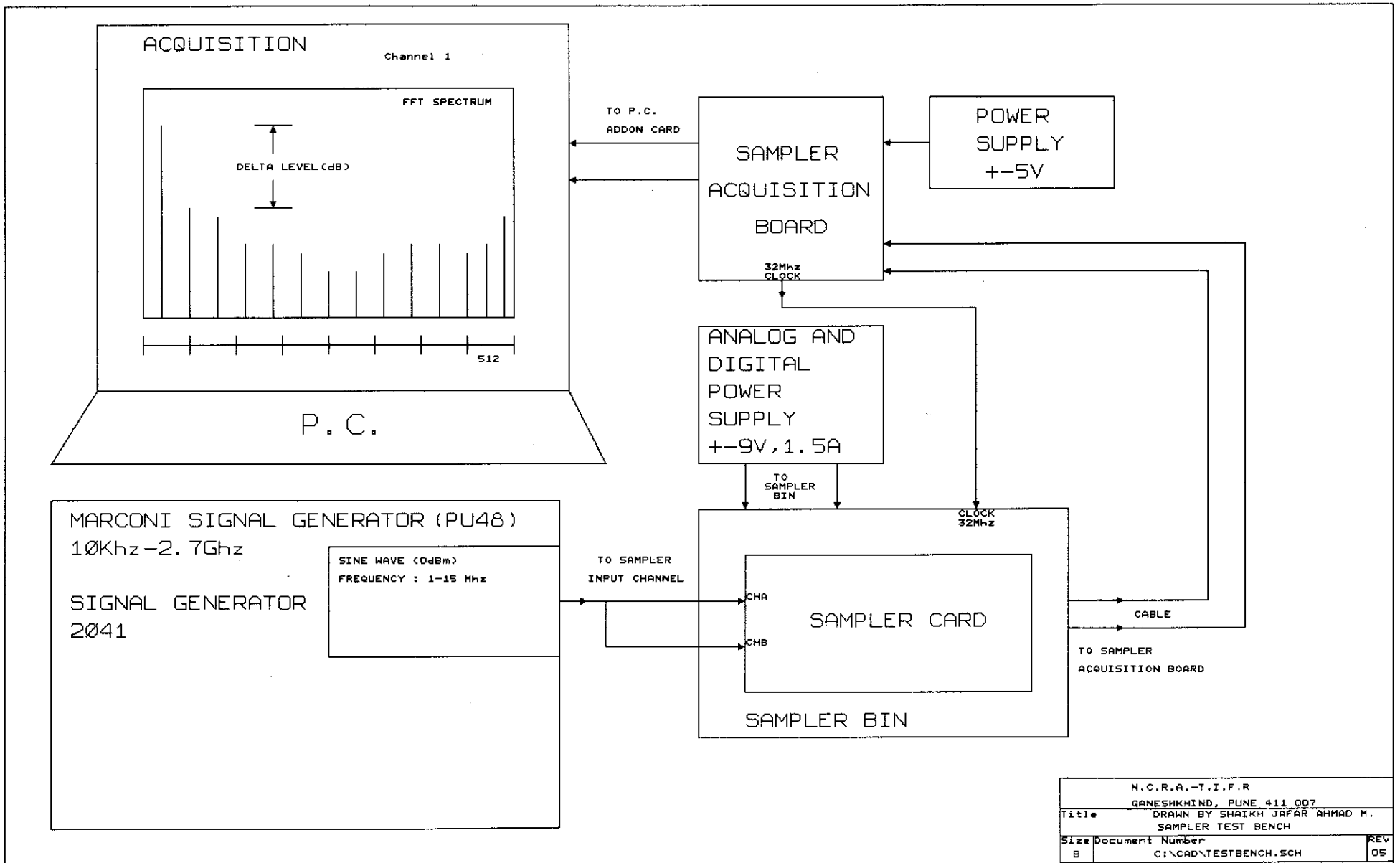
Personal Computer : MAX - P -78 (486)

Power Supply : 1) Sampler Bin - ± 9V , 1.5 A
2) DAS Card - ± 5V

Input For Sampler Card (Test Signal) : 0 dBm Sine Wave Frequency :- 1-15 MHz

Procedure : 1) Give the sampler card the sine wave as input. By varying its frequency observe the FFT spectrum on P.C.
2) For various input frequencies note down the delta level (the difference between the the fundamental component and harmonic component with maximum amplitude)

Sampler card test reports are attached alongwith the report. As a part of my training I have assembled the Sampler rack. Mr. Bhalerao Vilas B. helped me doing this job.



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