Technical Report

Clock distribution card for the GMRT correlator — Modifications and Phase stability

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Date : 10/8/97

1 Introduction

The basic clock distribution scheme for the GMRT correlator is realized by sending a 32 MHz sine wave, generated from a common source, to each of the subunits, like the sampler, delay-dpc, mac, etc. The "clock distribution card" takes this sine wave as its input, converts into square wave of the same frequency and makes copies of the square wave for different cards in the subunit (see Fig 1.). To take care of the differential propagation delay of data and control signals while capturing them the clocks have to skewed. This skewing of the clock is realised by introducing RC phase shifters (see Fig 1.).

As shown in Fig 1., the incoming sine wave is first divided into two and the two sine waves are passed through different all-pass RC phase shifters. The phase shifter output is fed to a comparator which converts the sine wave to square wave. Buffers are then used to make copies of these square waves. Thus two sets of clocks are generated whose relative phase can be changed using the phase shifter network.

The clock distribution card was designed and made by Rakesh Malik. It is used in the Mk III correlator. In this report we present modifications done on the card to improve its performance. We also present the results of various tests conducted on the improved version.

2 Problems in the existing cards

1. The maximum achievable delay between the two clocks is between 5 to 7 ns while it is preferred to have at least 10 ns.
2. The delay between the two clocks is a sensitive function of the amplitude of the input sine wave.
3. The duty cycle and the "shape" of the square wave is a function of the input sine wave amplitude.

3 Modifications done on the circuit

3.1 Phase shifter

The phase shifter used in the existing card is a RC lag network. We found that RC lead network (see Fig. 2) gives better performance than the lag network. The phase shift is varied by changing the 1K trim-pot. A 15 Ω resistor is added in series with the trim-pot to restrict the phase variation to 9.0 ns. This is because when the resistor value is small the circuit becomes more sensitive to the amplitude of the input sine wave.

The sensitivity of the phase to the input sine wave amplitude is measured with a Vector Voltmeter and is shown in Fig. 3. The plots are for three different resistor value setting (1K, 425 Ω, 0 Ω) of the trim-pot. It is clear from the plot that in the worst case (ie when the trim-pot value is 0 Ω) a $\pm$ 1 dB change about 4 dBm input power produces a phase shift of $\pm$ 10° . This corresponds to $\pm$ 1.0 ns at 32 MHz. **Thus we recommend to operate the clock distribution card with an input power level of +4 dBm.**

3.2 Comparator

The comparator circuit is realised using a ECL to TTL (10125) converter. This circuit has been modified. The inverting inputs is connected directly to the internal reference voltage (VBB) and a decoupling capacitor of 0.1 μf is also provided for the reference (see Fig. 3). A 100 Ω resistor is connected across the two inputs of the 10125 which forms the termination. The phase shifter output is ac coupled to the non-inverting input through a 39 Ω series resistor.

With these modifications we measured the sensitivity of the "shape" of the square wave to the input sine wave amplitude. There is no variation in either the duty cycle or the "shape" when the input is changed from +1 to +7 dBm for any trim-pot resistor value in the phase shifter.

4 Phase stability

The phase stability of the square wave relative to the input sine wave (ie between A & B or A & C in Fig. 1) and that between the two square wave outputs (ie between B & C in Fig. 1) are important in the present application. We have used the HP vector voltmeter (model 8508A) for measuring the phase stability. The 32 MHz input signal is fed from a Marconi signal generator (model 2031). The output of 10125 is series matched with a 50 Ω resistor for all the measurements. The lock range of the vector voltmeter is set to 25–50 MHz range so that the voltmeter locks to the fundamental frequency of the square wave.

Fig. 4a,b shows the output clock phase relative to the input signal (ie between A & B in Fig. 1) as a function of time for trim-pot value 1 K and 0 Ω respectively. The relative phase between the two outputs (ie between B & C in Fig. 1) as a function of time is shown in Fig 4c. In Fig 5a-d again the relative phase between A & B is shown. The data for these plots is collected by keeping the circuit powered "on" continuously for several days. However the data is acquired only when the measurement setup is free. It is clear from the Figs. 4 & 5 that the peak-to-peak phase variation is about 1° which corresponds to a time variation of 87 ps at 32 MHz.

5 Modifications for clock distribution card

1. Cut pin numbers 4 & 5 of the IC bases for U28 and U29 and solder them on the PCB at their respective places. Take 2 more similar IC bases, cut the pin numbers 4&5 and connect them together. Connect pin numbers 4&5 of U28 IC base to pin 1 of R47 (i.e. VEE1) and that of U29 IC base to pin 1 of R48 (i.e. VEE1).

2. Pin 1 (which is not connected to ground) of the capacitor C29 is to be connected to L1 i.e.VEE1.

3. Pin 1 (which is not connected to ground) of each of capacitors C36, C47 is to be connected to pin 1 of R48 i.e.VEE1.

4. Do not soldier the inductor L3. Connect pin 1 of L3 in the PCB (which is connected to pin 3 of U31) to VEE1.

5. Do not solder the components R37, C39, C38, R42, C44, C37, R47, R48.

6. Cut the track between R39 and R38. Connect pin 1 of R39 to 15E (R1) resistor. The other terminal of R1 should be connected to GND1.

7. Cut the track between pin 2 (middle pin of pot R39) and pin 2 of C53.

8. Instead of connecting pin 1 of C51 to GND1, it should be connected to the pin of R38 where the track is being cut.(track between R38 & R39) and the same should be connected to pin 2 of C53.

9. Cut the track between R44 and R43; connect the pin 1 of R44 to 15ω (R2) resistor. The other terminal of R2 should be connected to GND1.

10. Instead of connecting pin 1 of C52 to GND1; it should be connected to the pin of R43 where the track is being cut. (track between R44 & R43).

11. Connect 100 Ω resistor between pins 2 &3 of IC U32. Connect 100Ω resistor between pins 14 & 15 of IC U32 .

12. Connect pin 2 of U32 to pin 1(VBB) of U32. Connect pin 14 of U32 to pin 1(VBB) of U32.

13. Cut the track going to R35 from pin 6 of U28.

14. Cut the track between pin 2 &6 of U28; **do not remove the track from pin 6 to R34.**

15. Cut the track between pin 2&6 of U29.

16. Connect externally 390 Ω resistor between pin 2&6 of U28 and U29 also.

17. Connect pin 2 of U28 to pin1 (which is not connected to ground) of R35.

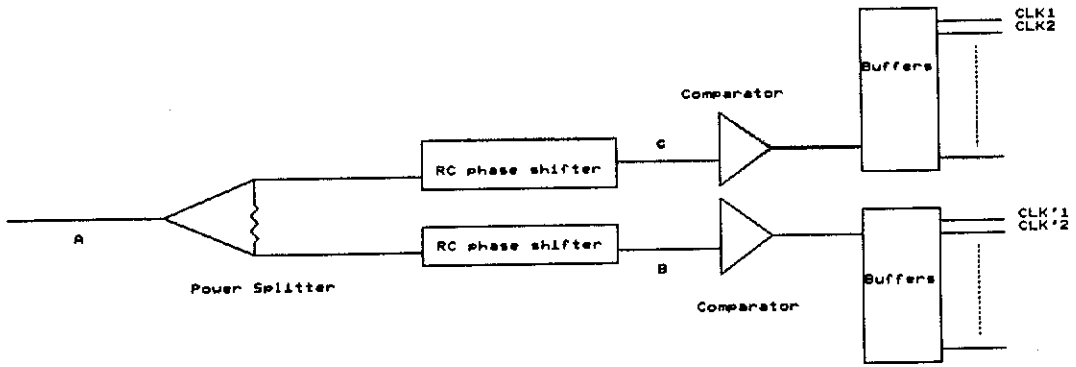


Fig. 1

NCRA-TIFR		
Title: Clk Distribution Card Block Diag.		
Size: B	Document Number: 1	REV
Date: July 31, 1997	Sheet 1 of 1	

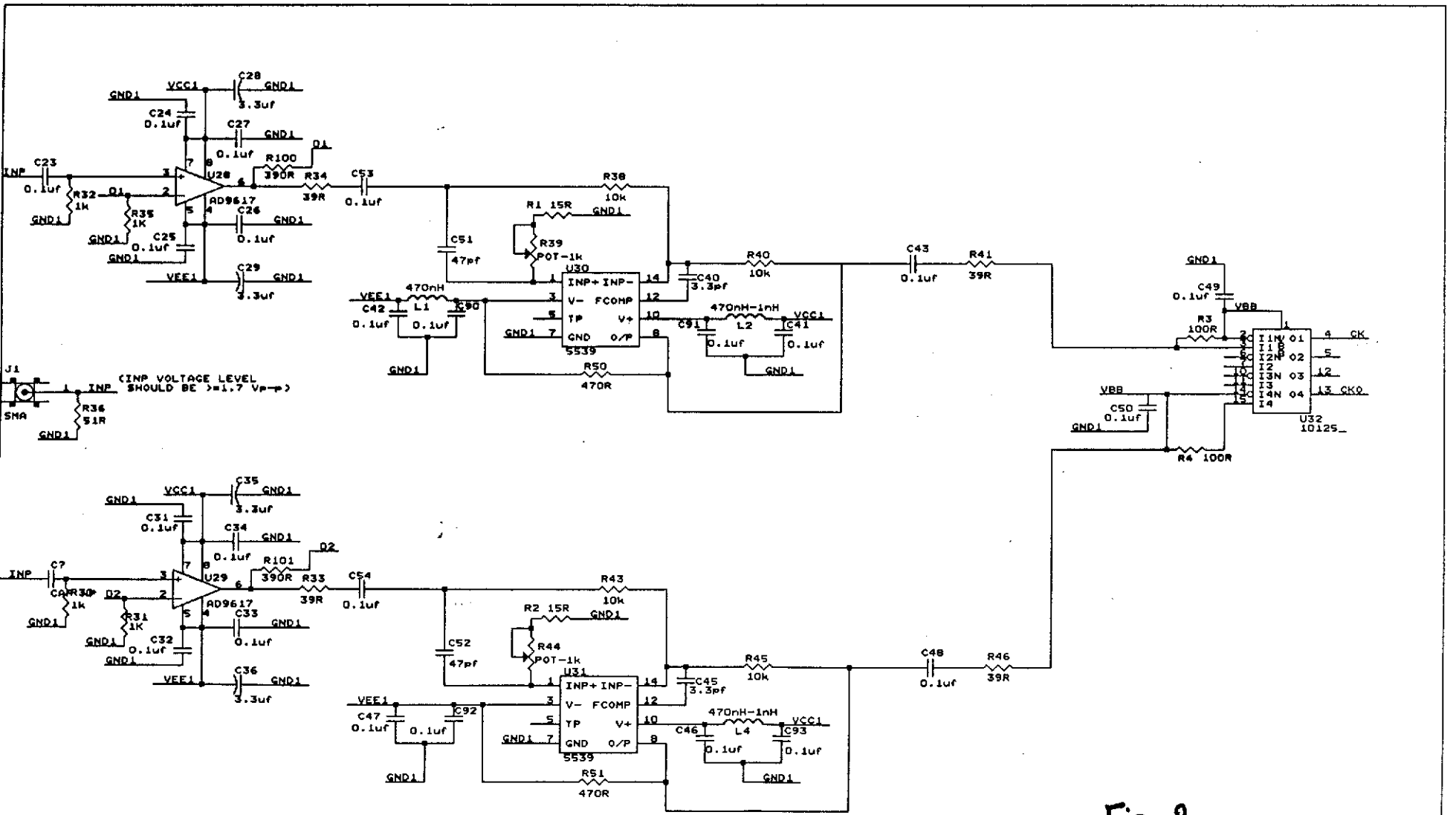
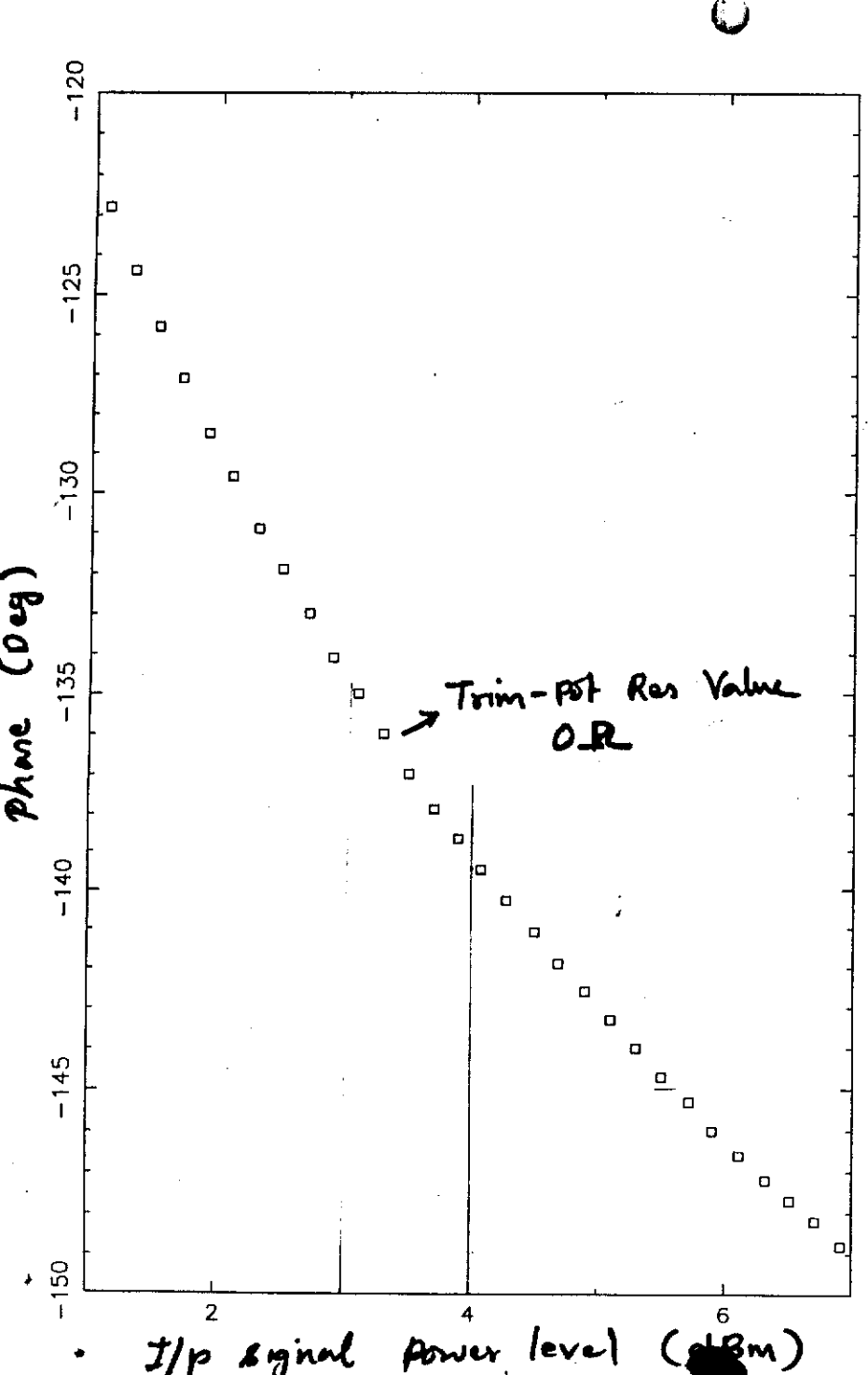


Fig. 2

TATA INSTT. OF FUND. RESEARCH		
Size B	Document Number D:\KIRAN\PHASE.SCH	REV
Date: July 31, 1997	Sheet of	


Phase (Deg)
-120
-125
-130
-135
-140
-145
-150
2
4
6
Trim-Pot Res Value
0Ω
I/p signal Power level (dBm)

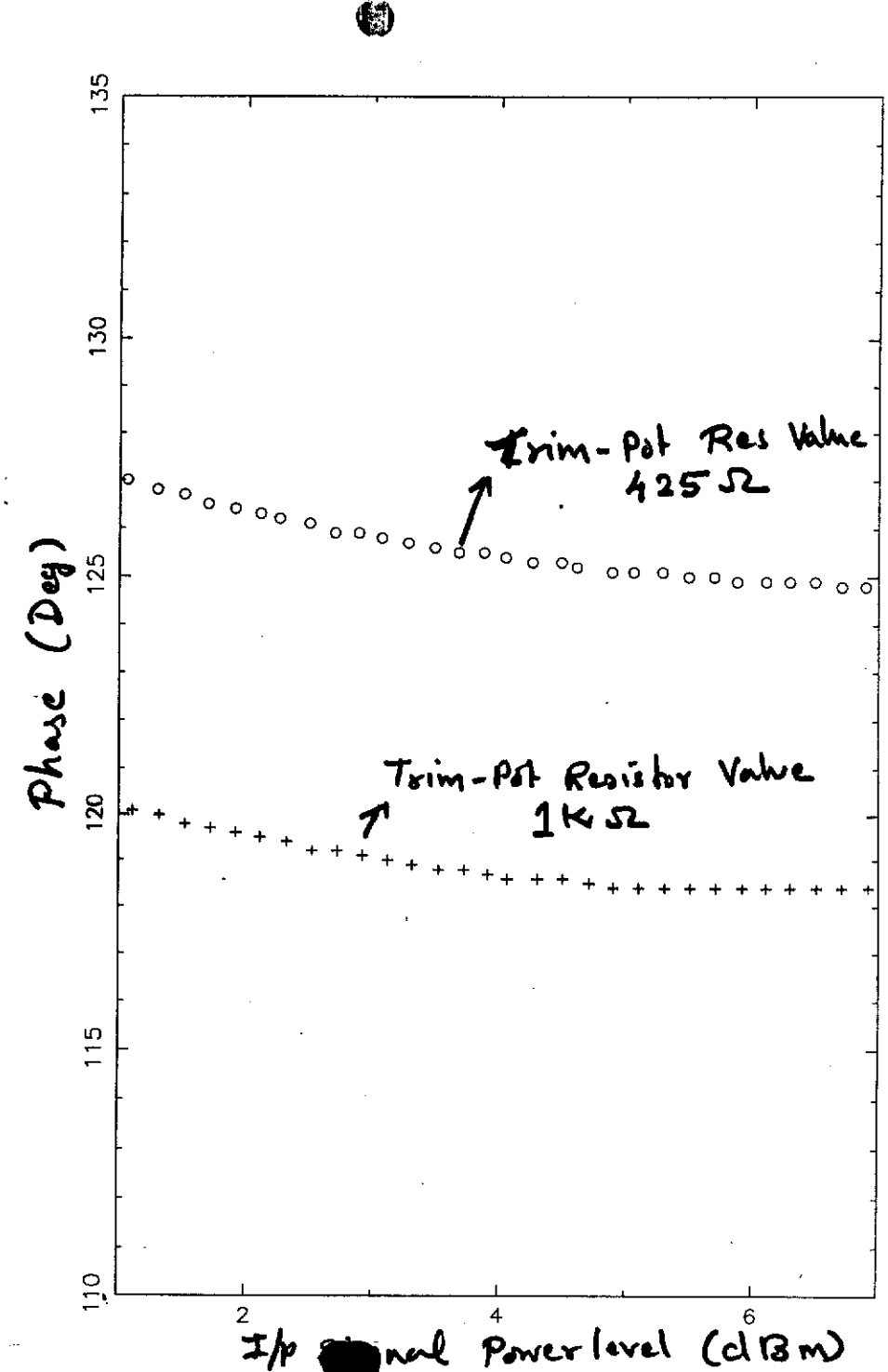
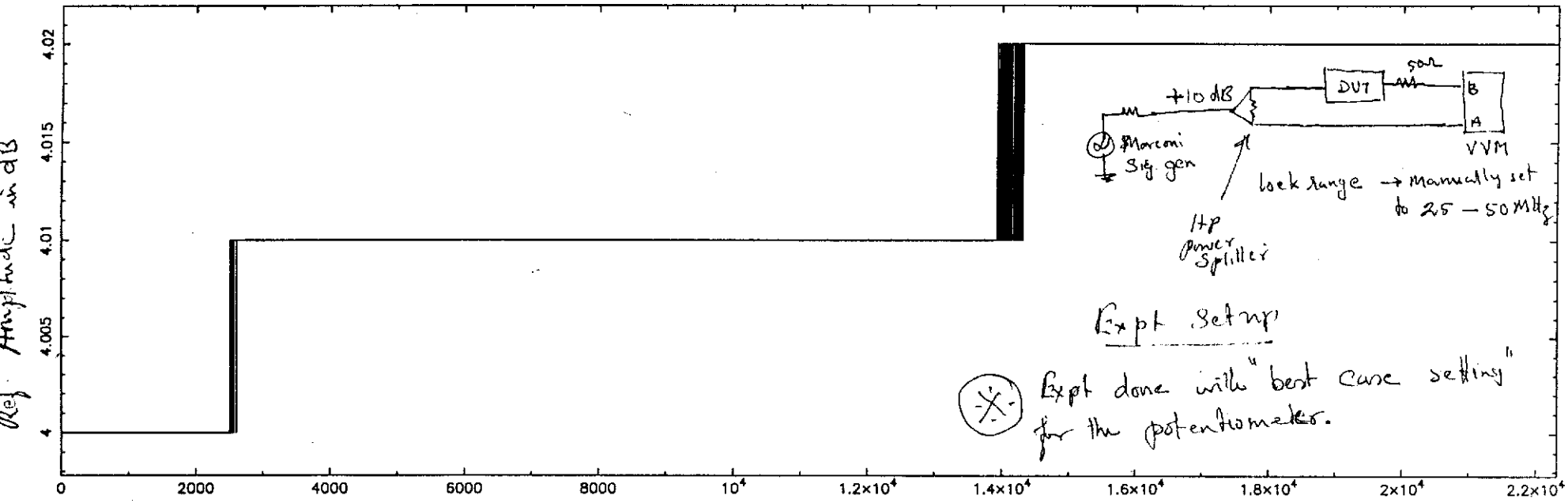

Phase (Deg)
135
130
125
120
115
110
2
4
6
Trim-Pot Res Value
425Ω
Trim-Pot Resistor Value
1KΩ
I/p signal Power level (dBm)

Fig. 3

Kiran / Anish



18:45 (24/6/97)

→ ~~time~~ Sample number

8:10 (25/6/97)

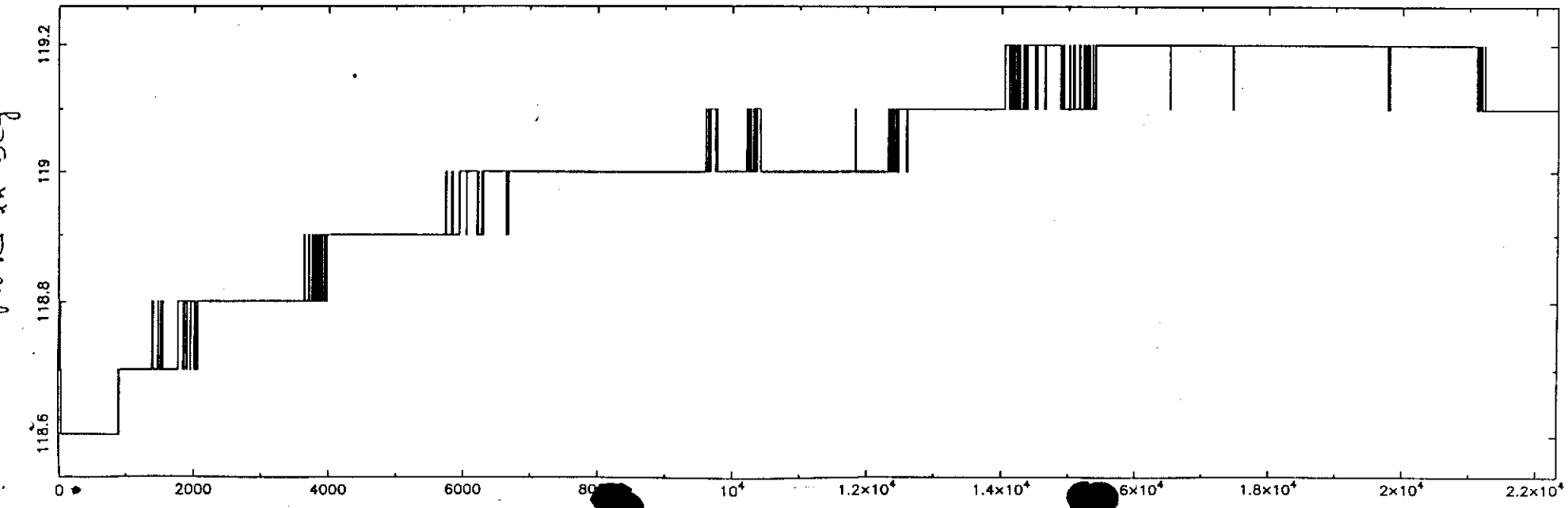
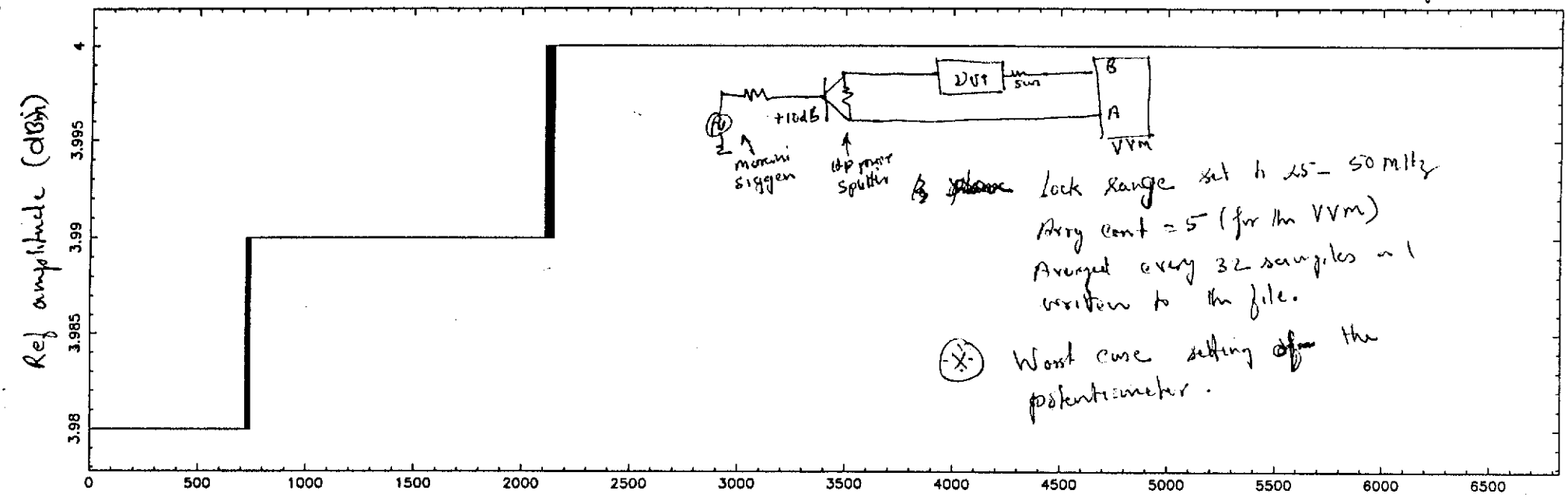


Fig 4a

Lisp on the [illegible]
Card for Correlator. (25/6/97)



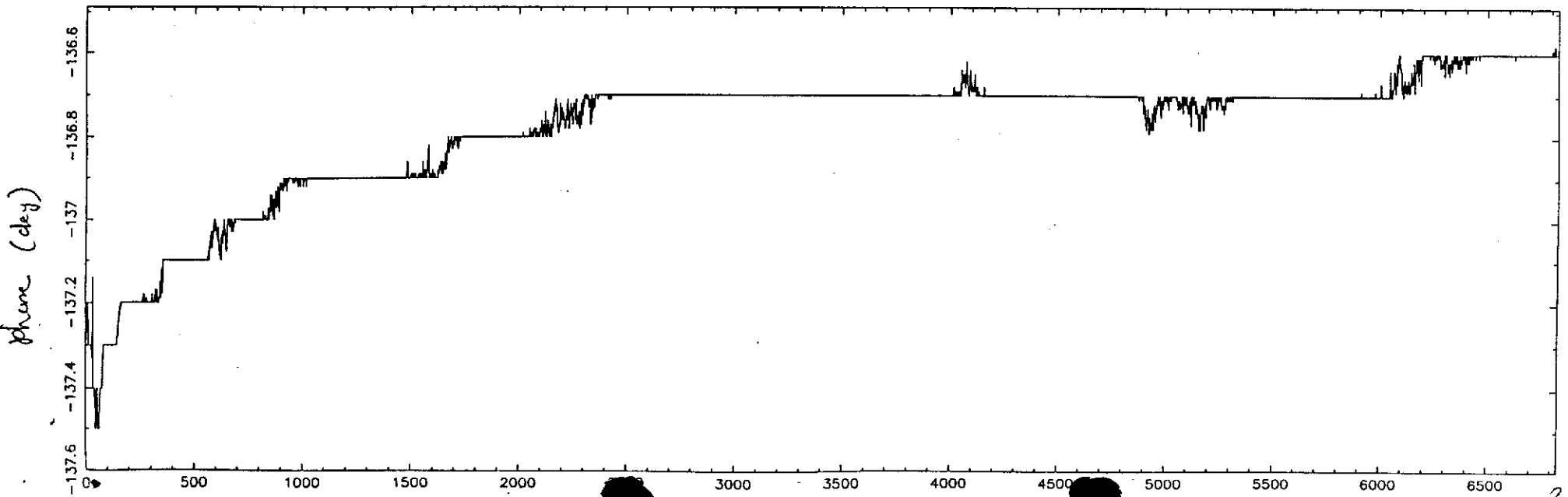
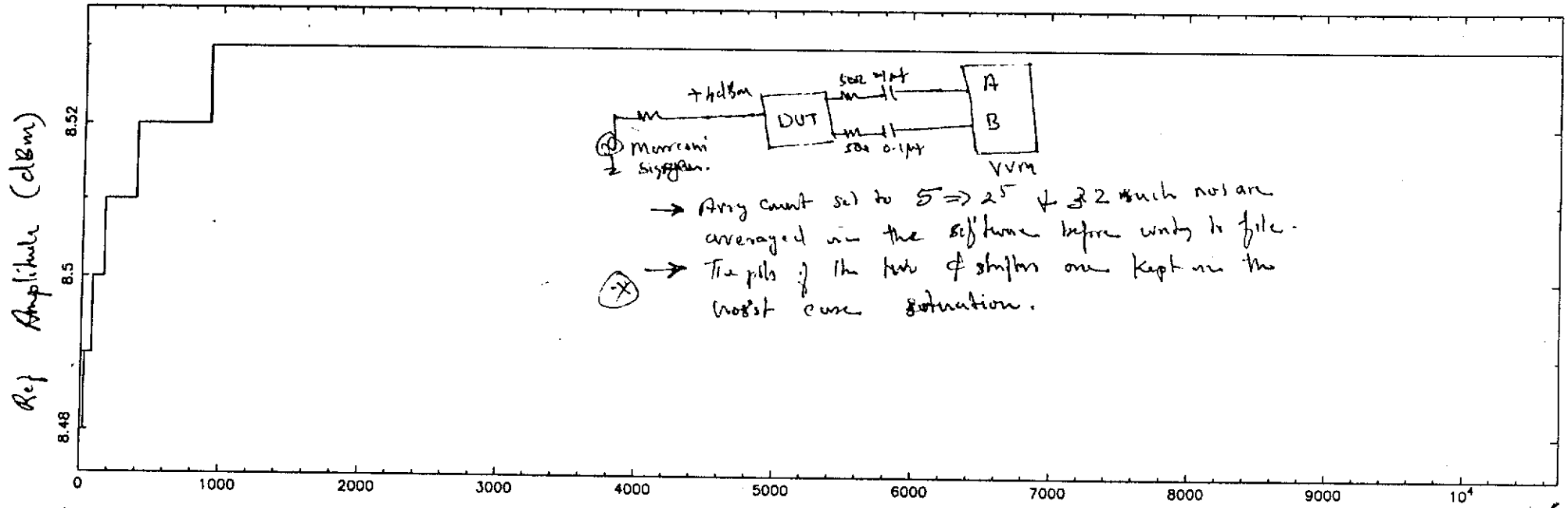


Fig 4b



→ Avg count set to $5 \Rightarrow 2^5 = 32$ which not are averaged in the software before writing to file.

→ The plots of the test of shifters are kept in the worst case situation.

16:30 (26/6/97)

4.15 (27/6/97)

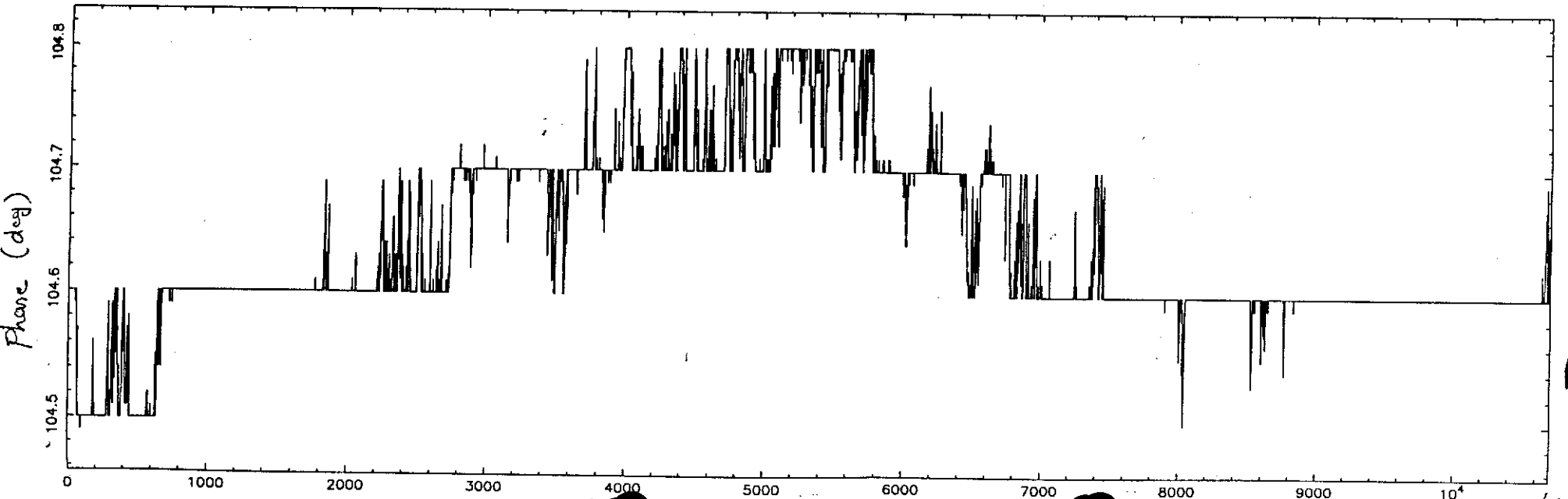
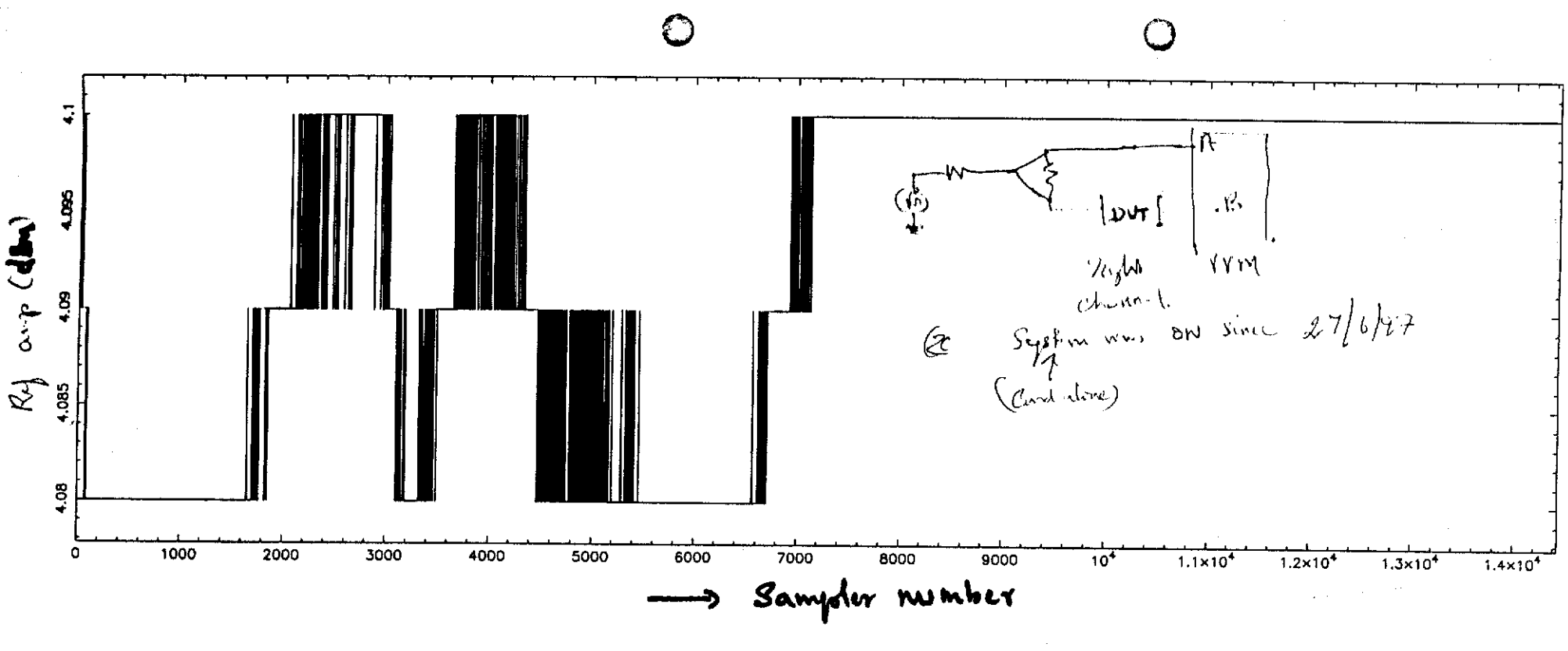


Fig 4.6

Phase Stability



1/7/97

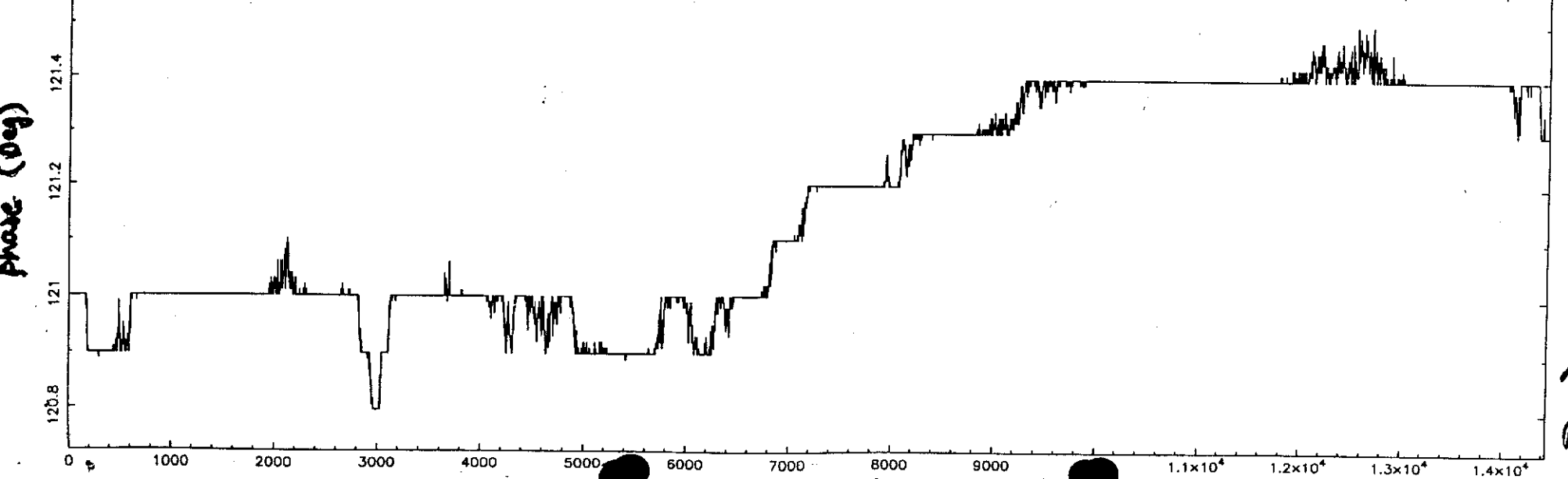
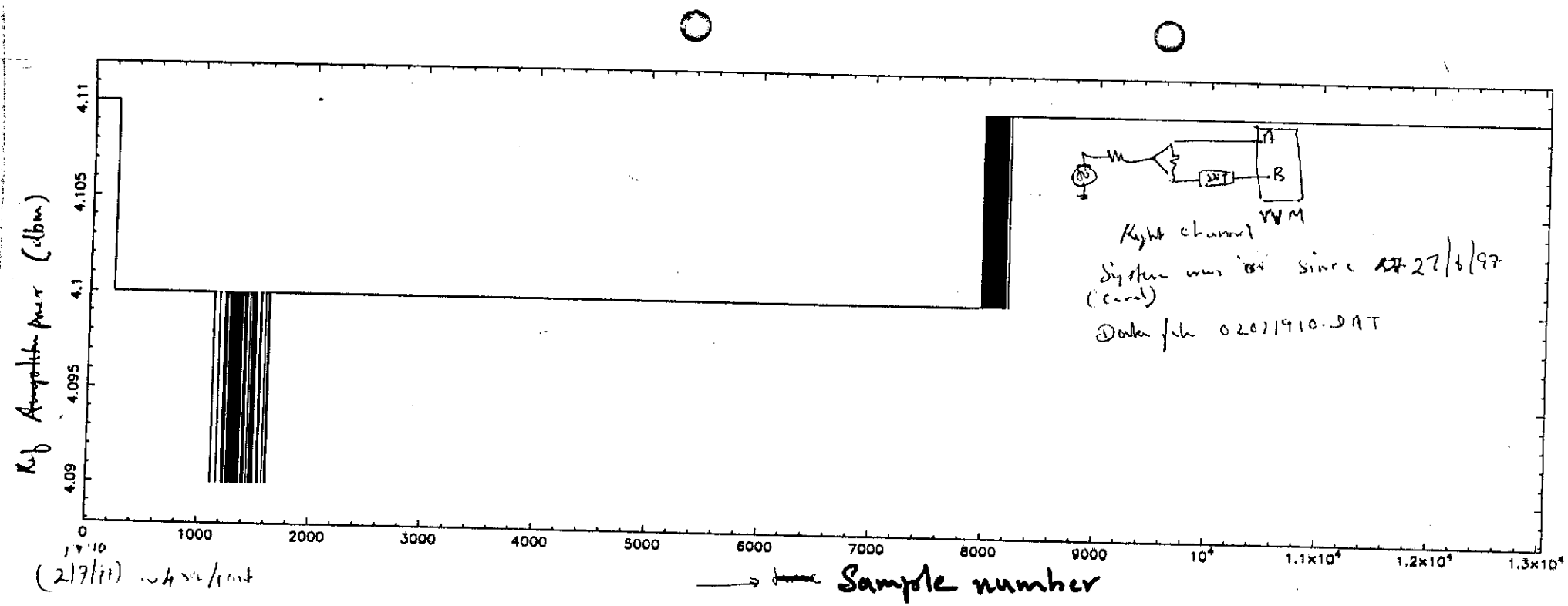


Fig 5a
Long term phase stabili


Rb Amplitude power (dBm)
4.11
4.105
4.1
4.095
4.09
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10⁴
1.1×10⁴
1.2×10⁴
1.3×10⁴
Sample number
Right channel
Data file 02071910.DAT
VVM
A
B

2/7/97

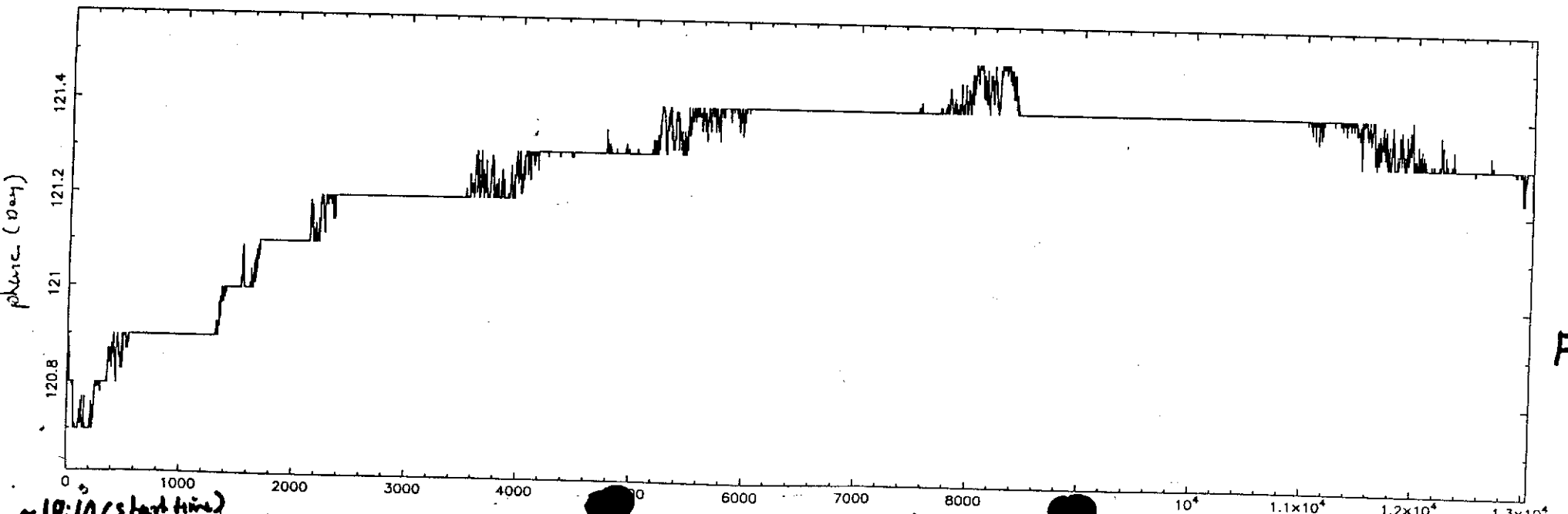
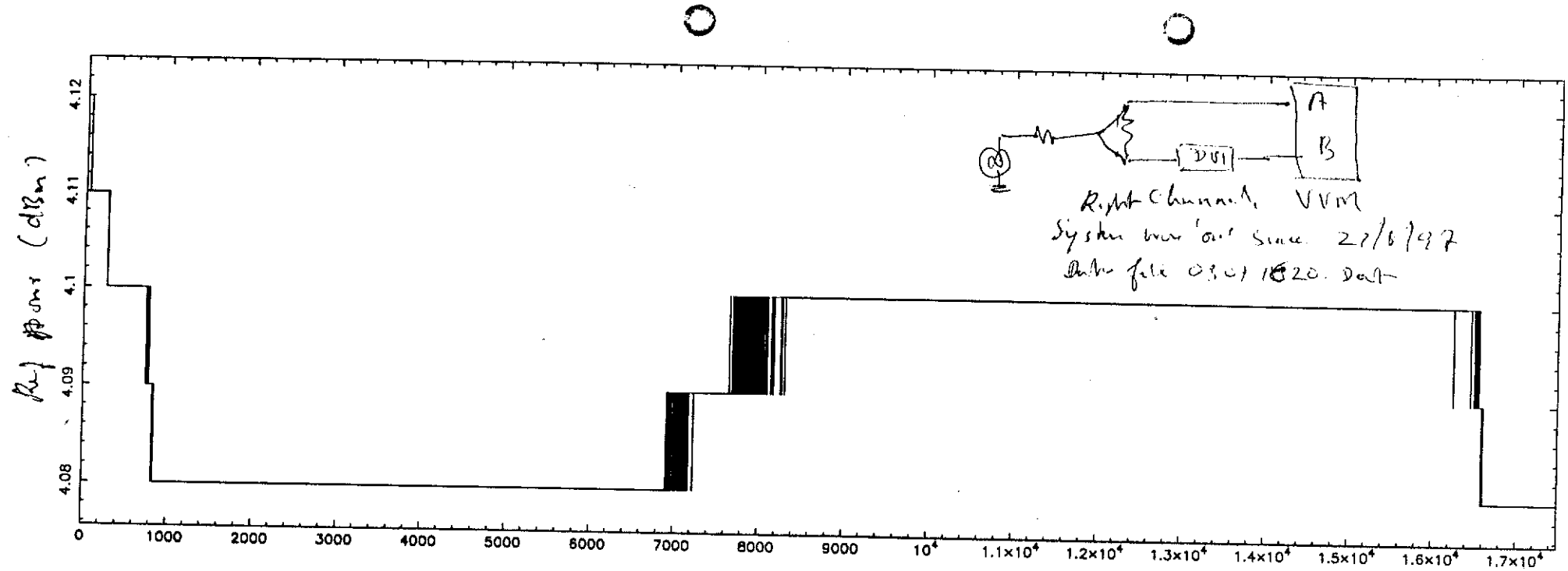

phase (deg)
121.4
121.2
121
120.8
0
1000
2000
3000
4000
6000
7000
8000
10⁴
1.1×10⁴
1.2×10⁴
1.3×10⁴

Fig 5b



3/7/97

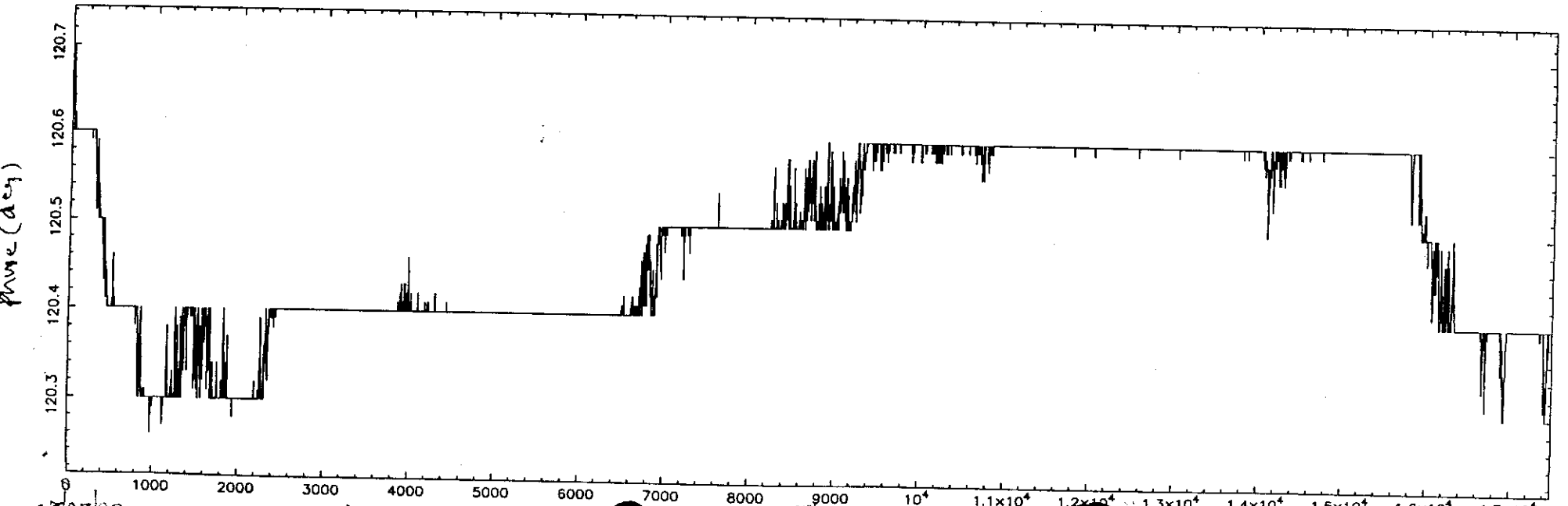
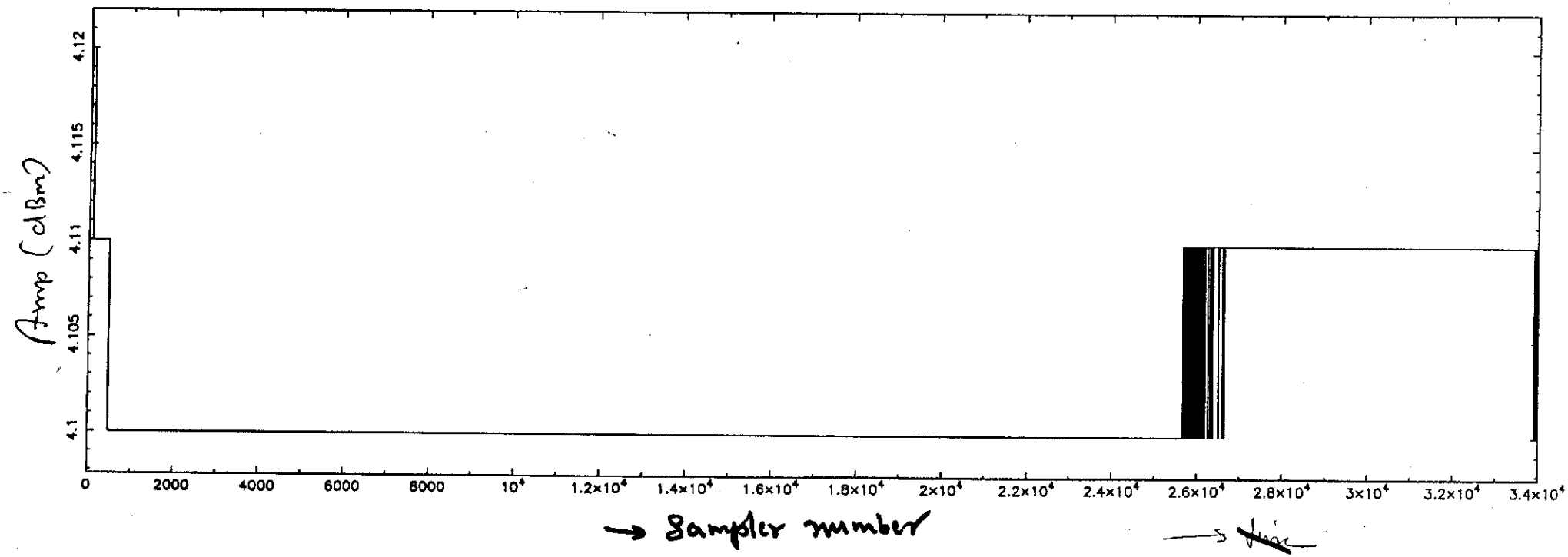


Fig 5c

05/03/97


Amp (dBm)
4.12
4.115
4.11
4.105
4.1
0
2000
4000
6000
8000
10^4
1.2×10^4
1.4×10^4
1.6×10^4
1.8×10^4
2×10^4
2.2×10^4
2.4×10^4
2.6×10^4
2.8×10^4
3×10^4
3.2×10^4
3.4×10^4
→ Sampler number

5/7/97

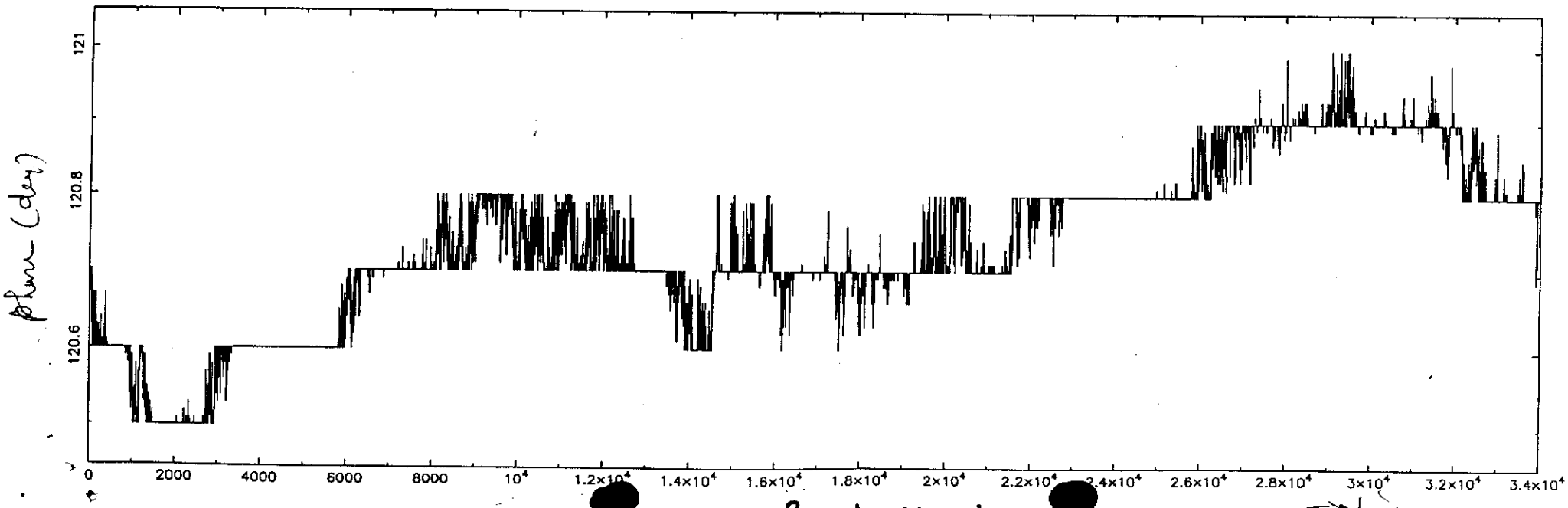
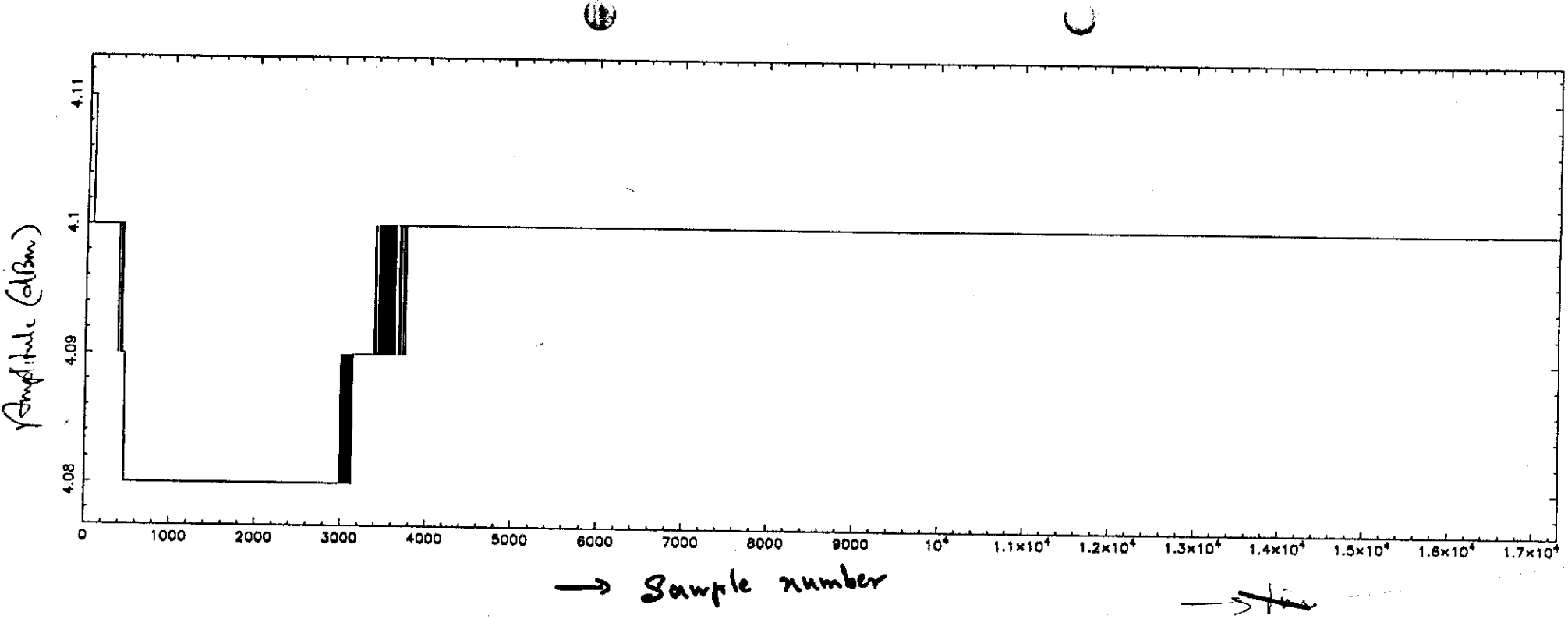

Phase (deg)
121
120.8
120.6
0
2000
4000
6000
8000
10^4
1.2×10^4
1.4×10^4
1.6×10^4
1.8×10^4
2×10^4
2.2×10^4
2.4×10^4
2.6×10^4
2.8×10^4
3×10^4
3.2×10^4
3.4×10^4

Fig 5d


Amplitude (dBm)
4.11
4.1
4.09
4.08
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10^4
1.1×10^4
1.2×10^4
1.3×10^4
1.4×10^4
1.5×10^4
1.6×10^4
1.7×10^4
Sample number

7/7/97

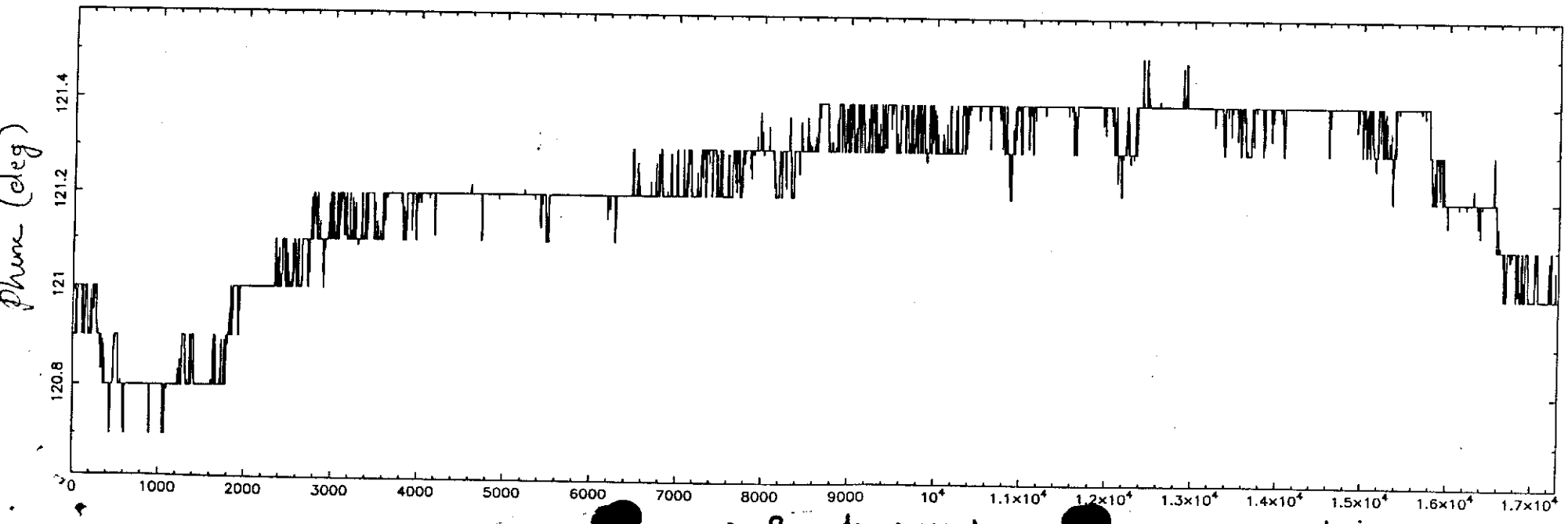

Phase (deg)
121.4
121.2
121
120.8
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10^4
1.1×10^4
1.2×10^4
1.3×10^4
1.4×10^4
1.5×10^4
1.6×10^4
1.7×10^4

Fig 5d

(4) metal-case TMO series, plug-in leads
(5) open construction TC series, surface-mount leadless

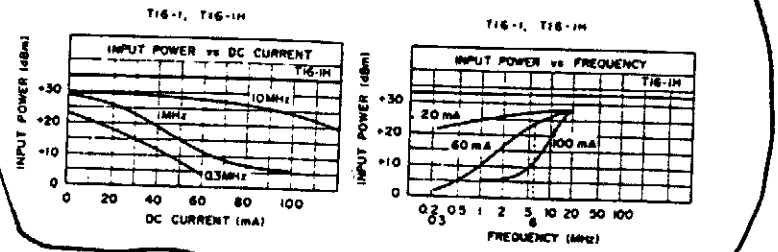
For these various types, the electrical configurations that are available are:

(A) DC isolated primary and secondary, center-tap secondary
(B) DC isolated primary and secondary, center-tap primary and secondary
(C) DC isolated primary and secondary
(D) unbalanced primary and secondary
(E) DC isolated primary and secondary, balanced primary and unbalanced secondary
(F) DC isolated, three open windings

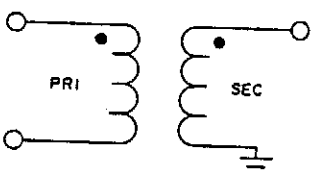
Coaxial connector models are available from 5 KHz to 500 MHz and are offered with 50 ohm and 75 ohm impedances; 75 ohm connectors are used at 75 ohm ports. The FT1.5-1, with unbalanced input and output is especially useful for 50 ohm to 75 ohm matching applications. The FTB series with unbalanced output and balanced input (connector ground insulated from the case) helps eliminate ground loop problems, especially when long cable runs are involved.

open package surface-mount requirements. Consult our Applications Department for your particular needs.

performance saturation curves T, TH series
(RF power & DC current at which signal saturation begins)



modern definition of terms



In some applications there is a need to pass a relatively high DC current through the primary winding. In this case, the transformer core may saturate resulting in reduced transformer bandwidth and power handling capability. Mini-Circuits TH series of transformers are designed to handle up to 100 mA in the primary winding without appreciable saturation and change in RF characteristics.

Transformer core saturation is influenced by (1) DC current through the winding, (2) RF input power, and (3) frequency of operation. These three variables interact to affect the point at which saturation occurs. See Figures 7 and 8 in which conventional transformer saturation is compared to the TH series.

Mini-Circuits has developed many special transformer impedance ratios and configurations where high DC current is passed through one winding of the transformer. Many of these designs have been for

amplitude balance
is a measure of the absolute difference in signal amplitude between each output of a center-tapped transformer relative to the center-tap.

phase balance
is a measure of the difference in signal phase between each output of a center-tapped transformer relative to the center-tap.

insertion loss
is the amount of power lost through the transformer under matched conditions.

balun
is a transformer that has a balanced input, where both ports are isolated from ground, to an unbalanced output where one side is connected to ground.

autotransformer
is a transformer where the secondary winding also comprises a portion of the primary winding.

1 dB bandwidth
is the frequency range over which insertion loss is less than 1dB referenced to the midband insertion loss.

From RF/IF Designer's Handbook, Mini-Circuits, 1992/93

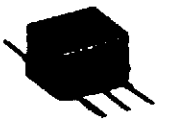
wideband

RF Transformers

3 KHz to 800 MHz

case style selection

outline drawings see Table of Contents



T, TH, TT

		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS▲ 3db MHz	INSERTION LOSS▲ 2db MHz	INSERTION LOSS▲ 1db MHz	PRICE $ Qty. (1-9)	DISTRIBUTOR FACTORY	DISTRIBUTOR LOCAL
A*	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45	•	•
	→	T1-6T	1	.015-300	.015-300	.021-150	.03-50	6.95	•	•
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95	•	•
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95	•	•
PRI SEC		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95	•	•
		T4-1	4	2-350	2-350	.35-300	2-100	3.25	•	•
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45	•	•
		T5-1T	5	.3-300	3-300	6-200	5-100	4.95	•	•
		T8-1T	8	.3-140	.3—140	.7—90	1-60	7.95	•	•
		T13-1T	13	3-120	3-120	.7-80	5-20	4.95	•	•
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65	•	•
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95	•	•
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	7.95	•	•
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45	•	•
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45	•	•
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95	•	•
		TMO4-1	4	2-350	.2-350	.35-300	2-100	6.25	•	•
		TMO5-1T	5	.3-300	3-300	.6-200	5-100	8.45	•	•
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45	•	•
B*	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95	•	•
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95	•	•
PRI SEC		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45	•	•
		TT4-1	3	.05-200	.05-200	.2-50	1-30	5.95	•	•
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95	•	•
		TT16-1	16	0.1-45	0.1-45	0.14-35	1-20	9.95	•	•
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95	•	•
	†TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95	•	•
	→	†TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45	•	•
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95	•	•
C	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25	•	•
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65	•	•
	→	T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65	•	•
PRI SEC		T1.5-1	1.5	1-300	1-300	.2-150	.5-80	4.45	•	•
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65	•	•
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45	•	•
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45	•	•
		T9-1	9	.15-200	.15-200	3-150	2-40	3.95	•	•
		T16-1	16	3-120	3-120	.7-80	5-20	4.45	•	•
		T36-1	36	.03-20	.03-20	.05-10	1-5	6.95	•	•
	TO	TO-75	1	10-500	—	10-500	40-250	6.95	•	•
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95	•	•
		T9-1H	9	2-90	2-90	3-75	6-50	6.45	•	•
		T16-1H	16	7-85	7-85	10-65	15-40	6.45	•	•
	TMO	■TMO1-02	1	1-800	1-800	2-500	—	9.45	•	•
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25	•	•
		TMO1.5-1	1.5	1-300	1-300	2-150	.5-8	8.45	•	•
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95	•	•
		†TMO4-6	4	.02-200	.02-200	.05-150	1-100	7.95	•	•
		TMO6-1	6	3-200	3-200	.5-150	5-50	7.95	•	•
		TMO9-1	9	15-200	15-200	.3-150	2-40	7.95	•	•
		TMO16-1	16	3-120	3-120	7-80	5-20	7.95	•	•

NOTES:

▲ Insertion loss referenced to mid-band loss.
TMO: Case A11 except
†TMO, TTMO: Case A03
■ Denotes 75 ohm models. For coax connectors, 75 ohm BNC is standard

1. For quality control procedures and environmental specifications, absolute maximum ratings see section 0 article. For T, TT, and TH series operating temperature, Temperature range is −20°C to +85°C.
2. Absolute maximum ratings: RF power 250 mW, DC current 30 mA.
3. For connector types and case mounting options, see case style outline drawing.
4. Prices and specifications subject to change without notice.

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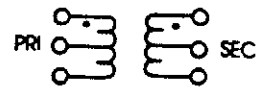
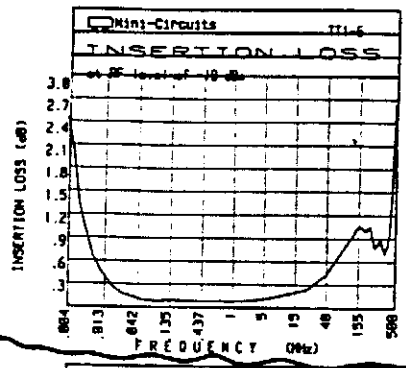
wideband

RF Transformers

Configuration B

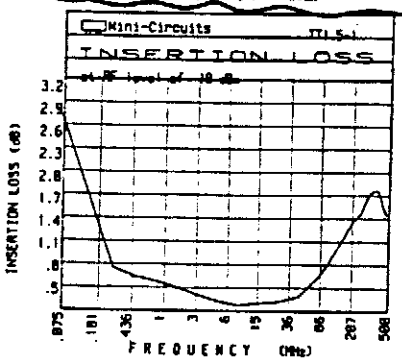




TT1-6

.004 to 500 MHz

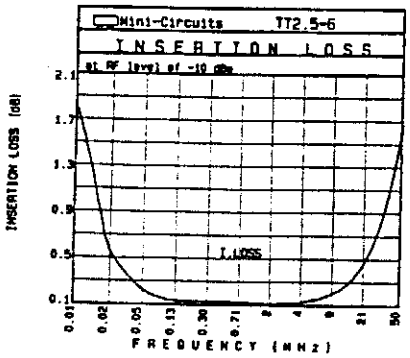
FREQ. (MHz)	I. LOSS (dB)	INPUT R. LOSS (dB)
.004	2.53	4.71
.020	.29	15.34
1.153	.10	37.84
100.858	.89	10.71
151.507	1.10	9.32
200.000	1.08	9.41
280.250	.87	12.74
350.000	.81	24.39
430.250	1.11	11.24
500.000	2.74	6.16



TT1.5-1

.075 to 500 MHz

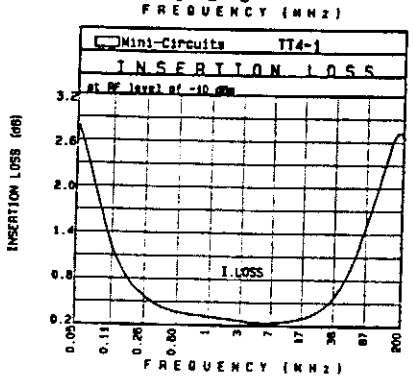
FREQ. (MHz)	I. LOSS (dB)	INPUT R. LOSS (dB)
.075	2.88	4.70
.913	.67	19.36
4.936	.41	23.51
19.837	.40	23.36
81.211	.75	16.19
201.509	1.47	8.72
297.468	1.80	5.38
351.506	1.89	4.13
439.125	1.70	2.79
500.000	1.57	2.35



TT2.5-6

.01 to 50 MHz

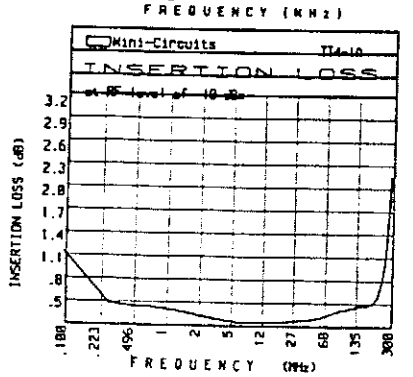
FREQ. (MHz)	I. LOSS (dB)	INPUT R. LOSS (dB)
0.010	1.85	2.83
0.020	0.74	6.20
0.025	0.52	7.77
0.050	0.22	12.98
0.100	0.15	19.05
10.000	0.26	14.59
25.000	0.67	8.03
25.890	0.71	7.73
48.062	1.65	3.91
50.000	1.74	3.73



TT4-1

.05 to 200 MHz

FREQ. (MHz)	I. LOSS (dB)	INPUT R. LOSS (dB)
0.050	2.88	1.46
0.100	1.29	4.13
0.200	0.58	8.81
0.501	0.39	15.77
1.000	0.36	19.03
30.000	0.51	11.31
50.000	0.91	7.28
100.860	1.96	3.92
195.150	2.78	3.87
200.000	2.76	4.08



TT4-1A

0.1 to 300 MHz

FREQ. (MHz)	I. LOSS (dB)	INPUT R. LOSS (dB)
.100	1.17	10.70
.846	.44	23.68
4.001	.29	30.12
18.929	.26	27.31
53.348	.32	17.29
99.339	.43	10.23
175.639	.49	3.69
223.677	.60	1.96
261.289	.99	1.36
300.000	2.21	1.09

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INTRODUCTION

The basic capacitor element is called a chip and consists of formulated ceramic dielectric materials in layers interspersed with metal electrode layers. The entire structure is fired together at high temperature, after which conductive terminations are applied on opposite ends to contact protruding electrode edges. Chips may be terminated with materials suitable for hybrid-circuit substrate assembly.

KEMET multilayer ceramic capacitors are produced in plants designed specifically for capacitor manufacture. The process features a high degree of mechanization as well as precise controls over raw materials and process conditions. Manufacturing is supplemented by extensive Technology, Engineering, and Quality Assurance programs. Extensive application in aerospace and military programs attests to the reliability of KEMET capacitors. No capacitors exceed the failure rate qualifications held by KEMET capacitors under military specification.

KEMET ceramic capacitors are offered in the three most popular temperature characteristics. These are designated by the Electronics Industry Association (EIA) as the ultra-stable C0G (known in the vernacular as NP0), the stable X7R (military BX or BR), and the general purpose Z5U. A wide range of sizes and lead arrangements are available to provide capacitance from 1 picofarad through 6.8 microfarads in 50, 100, and 200 volt ratings.

TEMPERATURE CHARACTERISTICS

Specified electrical limits for the three principal temperature characteristics are shown below. Electrical stability with respect to temperature and voltage is ranked inversely to the packaging efficiency (capacitance × voltage in a given case size). C0G is made from ceramic materials which are not ferroelectric, yielding superior stability but low packaging efficiency. Both X7R and Z5U capacitors are made from materials which are ferroelectric, principally barium titanate. This material changes crystalline form at its Curie point of approximately 120°C. The change in structure causes a radical change in the inherent dielectric constant, directly affecting the exhibited capacitance. Other materials in the ceramic formulations modify this effect to different degrees in producing the X7R and Z5U characteristics.

AGING

The change in dielectric constant above the Curie point is reversible but the reversal does not occur instantaneously. In the phenomenon called aging, capacitance declines progressively with time along a typical curve. The slope of this curve for X7R characteristic amounts to a loss of approximately 1.0% in capacitance for every decade of hours at 25°C following the last excursion above the Curie point. The typical slope for Z5U characteristic is approximately 3-5% per hour decade. C0G does not exhibit aging.

Aging rates are utilized in testing KEMET capacitors prior to shipment. Capacitance test limits are designed to bring capacitors within the specified tolerance at 1,000 hours, allowing a nominal six weeks for receipt and use by the customer. This is a matter of convenience for the customers' incoming inspection, for the capacitance will continue to decline with time.

VOLTAGE EFFECTS

Ferroelectric materials are also affected by applied voltage, both alternating and direct. Low values of voltage produce a slight increase in capacitance and dissipation factor. Higher voltages cause a decrease in capacitance which may become quite large. Typically, capacitors with BX or X7R characteristic decrease in capacitance by approximately 10% when rated DC voltage is applied. Other formulations with very high dielectric constants may exhibit a capacitance decrease of 50%.

This partial polarization of the ferroelectric formulations by DC voltage persists for some time after the voltage is removed. This residual effect can be removed by "de-aging," or raising the capacitors above the Curie point for a period of time. Two hours at 150°C is a satisfactory treatment. Upon returning to room temperature, the capacitors will once more age according to the previous discussion.

CUSTOMER TESTING

Because of the temperature and voltage effects, caution must be used in establishing a testing sequence. Dielectric strength and insulation resistance tests both apply high DC voltage and depress capacitance, so capacitance should be measured prior to these tests. Alternatively, the de-aging described above may be performed, followed by a stabilizing storage at room temperature, ambient conditions for about 24 hours.

SPECIFIED ELECTRICAL LIMITS

PARAMETER	TEMPERATURE CHARACTERISTICS		
	C0G	X7R	Z5U
Dissipation Factor: Measured at following conditions: C0G — 1 kHz and 1 vrms if capacitance > 1000 pF 1 MHz and 1 vrms if capacitance ≤ 1000 pF X7R — 1 kHz and 1 vrms if capacitance > 100 pF 1 MHz and 1 vrms if capacitance ≤ 100 pF Z5U — 1 kHz and 0.5 vrms	0.15%*	2.5%	4.0%
Dielectric Strength: At 2.5 times rated DC voltage.	Pass Subsequent IR Test		
Insulation Resistance (IR): At rated DC voltage, whichever of the two is smaller.	1,000 MΩ-μF or 100 GΩ	1,000 MΩ-μF or 100 GΩ	1,000 MΩ-μF or 10 GΩ
Temperature Characteristic: Range, °C Capacitance Change without DC voltage	−55 to 125 0 ±30 ppm/°C*	−55 to 125 ±15%	+10 to 85 +22%, −56%

±60 ppm/°C below 10pF nominal.
−53 ppm −30 ppm/°C from +25°C to −55°C comparable to MIL-C-20.
*0.10% for surface mounted chips.

Ref:- Kemet Solid tantalum & Multi layer Ceramic Capacitors, Kemet

Multilayer Ceramic Capacitor (Radial(s)
Ref:- Gujarat Poly-Avx Electronics Ltd.

POLY-AVX

X7R DIELECTRIC SIZE AND CAPACITANCE SPECIFICATIONS

EIA Characteristic — **Dimension : Inches (Millimeters)**

POLY-AVX Style		SR15		SR20		SR21		SR30	
Width (W)		.150 (3.81)		.200 (5.08)		.200 (5.08)		.300 (7.62)	
Height (H)		.150 (3.81)		.200 (5.08)		.200 (5.08)		.300 (7.62)	
Thickness (T)		.100 (2.54)		.125 (3.175)		.125 (3.175)		.150 (3.81)	
Lead Spacing (L.S.)		.100 (2.54)		.100 (2.54)		.200 (5.08)		.200 (5.08)	
Lead Diameter (L.D.)		.020 (.508)		.020 (.508)		.020 (.508)		.020 (.508)	
Cap. in. ★ pF	Typical POLY-AVX Part Nos.	WVDC 100	50	WVDC 100	50	WVDC 100	50	WVDC 100	50
470	SR.....C471KAA								
1000	SR155C102KAA								
1500	SR.....C152KAA								
2200	SR.....C222KAA								
3300	SR.....C332KAA								
4700	SR.....C472KAA								
6800	SR.....C682KAA								
10,000	SR215C103KAA								
15,000	SR.....C153KAA								
22,000	SR.....C223KAA								
33,000	SR.....C333KAA								
47,000	SR.....C473KAA								
68,000	SR.....C683KAA								
100,000	SR215C104KAA								
150,000	SR.....C154KAA								
220,000	SR215C224KAA								
330,000	SR.....C334KAA								
390,000	SR.....C394KAA								
470,000	SR305C474KAA								
1.0μF	SR305C105KAA								

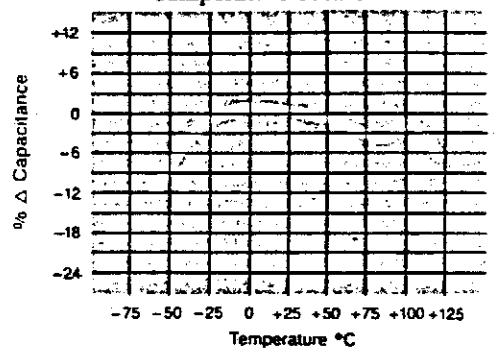
For other styles, voltages, tolerances and lead lengths see Part No. Codes or contact factory.

★ Other capacitance values available upon special request.

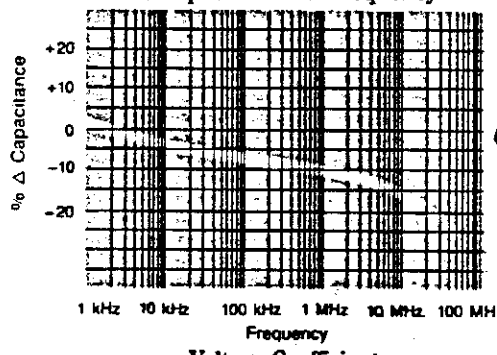
■ = Industry preferred values

Typical Characteristic Curves

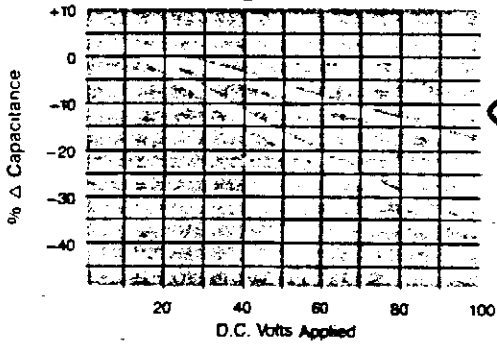
Temperature Coefficient



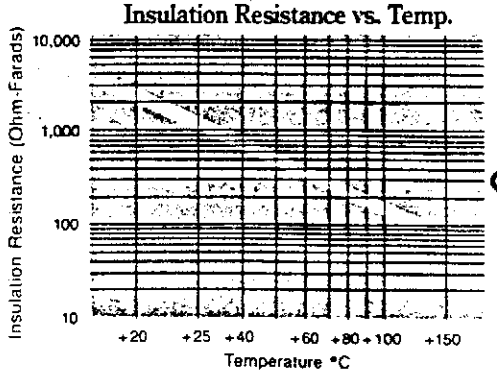
Δ Capacitance vs. Frequency



Voltage Coefficient



Insulation Resistance vs. Temp.



POLY-AVX

Z5U DIELECTRIC SIZE AND CAPACITANCE SPECIFICATIONS

EIA Characteristic

Dimensions : Inches (Millimeters)

POLY-AVX Style		SR15	SR20	SR21	SR30
Width (W)		.150 (3.81)	.200 (5.08)	.200 (5.08)	.300 (7.62)
Height (H)		.150 (3.81)	.200 (5.08)	.200 (5.08)	.300 (7.62)
Thickness (T)		.100 (2.54)	.125 (3.175)	.125 (3.175)	.150 (3.81)
Lead Spacing (L.S.)		.100 (2.54)	.100 (2.54)	.200 (5.08)	.200 (5.08)
Lead Diameter (L.D.)		.020 (.508)	.020 (.508)	.020 (.508)	.020 (.508)
Cap. in. ★ pF	Typical POLY-AVX Part Nos.	WVDC 100 50	WVDC 100 50	WVDC 100 50	WVDC 100 50
10,000	SR155E103ZAA	■	■	■	
47,000	SR.....E473ZAA	■	■	■	
100,000	SR215E104ZAA	■	■	■	
150,000	SR.....E154ZAA	■	■	■	
220,000	SR215E224ZAA	■	■	■	
330,000	SR215E334ZAA	■	■	■	
470,000	SR215E474ZAA	■	■	■	
680,000	SR.....E684ZAA	■	■	■	
1.0μF	SR305E105ZAA	■	■	■	
1.5μF	SR.....E155ZAA	■	■	■	
2.2μF	SR.....E225ZAA	■	■	■	
3.3μF	SR.....E335ZAA	■	■	■	

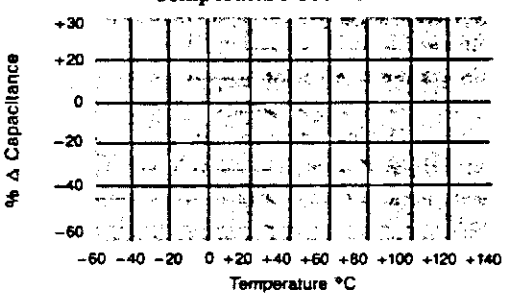
For other styles, voltages, tolerances and lead lengths see Part No. Codes or contact factory.

★ Other capacitance values available upon special request.

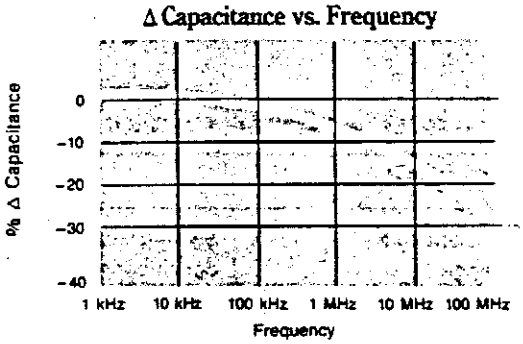
■ = Industry preferred values

Typical Characteristic Curves

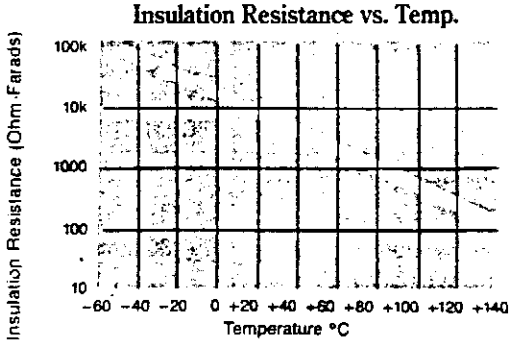
Temperature Coefficient



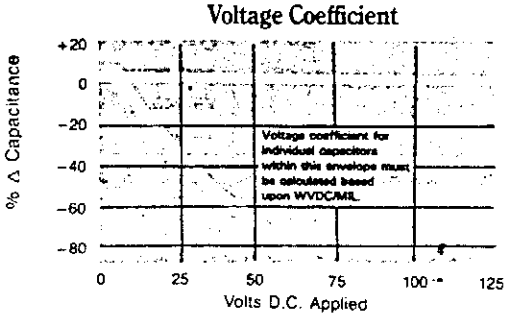
Δ Capacitance vs. Frequency



Insulation Resistance vs. Temp.



Voltage Coefficient



POLY-AVX

HOW TO ORDER

POLY-AVX Styles: SR15, SR20, SR21, SR30

Part Number Example

SR21 5 E 10 4 M A A

- SR21 — POLY-AVX Style
- 5 — Voltage
- E — Temperature Coefficient
- 10 — Sig. Figures of Capacitance
- 4 — Multiplier (Additional no. of zeros)
- M — Capacitance Tolerance
- A — Failure Rate Not Applicable
- A — Leads

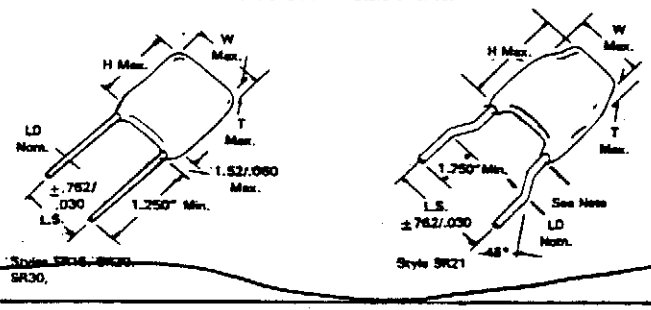
Part Number Codes

Voltages: 50V = 5, 100V = 1, 200V = 2

Temp. Coefficient: NPO = A, X7R = C, Z5U = E

Sig. Figures of Capacitance and Multiplier: First two digits are the significant figures of capacitance. Third digit indicates the additional number of zeros. For example, order 100,000 pF as 104. (For values below 10pF, use "R" in place of decimal point, e.g., 1R4 = 1.4 pF).

Dimensions : Millimeters (Inches)



GENERAL SPECIFICATIONS

Dielectric	NPO	X7R	Z5U
Capacitance Range	See Individual Parts Specifications	See Individual Parts Specifications	See Individual Parts Specifications
Capacitance Test at 25°C	Measured at 1 VRMS max at 1 KHZ (1MHZ for 100 pf or less)	Measured at 1 VRMS max at at 1KHZ	Measured at 0.5V RMS max at 1KHZ
Capacitance Tolerances	C = ±.25pF, D = ±.50pF F = ±1%, G = ±2% J = ±5%, K = ±10%, M = ±20% FOR VALUES LESS THAN 10PF TIGHTEST TOL IS ± 0.25 pF	J = ±5%, K = ±10%, M = ±20%	M = ±20%, Z = +80% −20%
Operating Temperature Range	−55°C to + 125°C	−55°C to + 125°C	+10°C to +85°C
Temperature characteristics	0 ± 30ppm/°C	±15% (DVdc)	+22%, −56%
Voltage Ratings	200, 100 and 50V dc	200, 100 and 50 Vdc	100 and 50 Vdc
Dissipation Factor	0.15% max (+25°C and +125°C) for values greater than 30 pF or Q = 20 × C + 400 for values of 30 pF and below. 1.0 VRMS, 1MHZ for values ≤ 100pF and 1KHZ for values > 100pF	2.5% max at 1KHZ, 1VRMS max	4.0% max at 1KHZ, 0.5 VRMS max
Insulation Resistance 25°C	100K megaohms or 1000megaohms − μF minimum whichever is less	100K megaohms or 1000 megaohms − μF minimum whichever is less	10K megaohms or 100 megaohms − μF minimum whichever is less
Dielectric Strength	250% of rated Vdc	250% of rated Vdc	200% of rated Vdc
Life Test (1000 hours)	200% rated Voltage at +125°C	200% rated Voltage at +125°C	150% rated Voltage at +85°C