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Alliot Sylvain

ESPEO 4

Giant Meter Radio Telescope

Fast Fourier Transform card

Test bench

Correlator group

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I am obliged to Dr. Yashwant Gupta responsible for the correlator group for giving me the opportunity to work on that project. I sincerely thank members of correlator lab for their help and co-operation.

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1. Introduction

My training period took place in India in the National Center for Radio Astrophysics(NCRA). This institute is similar to Nancay observatory in France, and is building a powerful radio telescope the Giant Meter Radio Telescope (GMRT). This telescope is a large array of 30 steerable very large antennas focused on the sky getting naturally produced radio waves reaching us.

I was involved in the realization of the Mark IV correlation system, collecting and processing every antenna signal. I worked particularly on a setup testing fully an electronic card before introduction in the whole system.

- The first part of the report gives a brief introduction to NCRA project and GMRT radio tool. We can then understand the reason and how GMRT has been built.
- The second part presents GMRT digital correlation. Why this real time system, will allow direct and multi base observations.
- The third part sets out the FFT test bench project schedule and the constraints that will explain hardware design.
- The forth part presents the project hardware and software realization.
- Finally, we will see the result of such a test bench and we will give some comments, about the FFT hardware processing.

2. NCRA/GMRT

2.1 NCRA

I was working for 5 month in Pune (India, Maharashtra), city situated 150 km from Bombay, in an Indian institute named (NCRA) National Center for Radio Astrophysics. NCRA is a part of the Tata Institute for Fundamental Research (TIFR) India's premier institution for research in basic sciences.

The institute is involving in setting up a powerful radio telescope, the Giant Meter Radio Telescope (GMRT) at Khodad 80 km north Pune. Designed to study many challenging astrophysical problems, GMRT will be the world's most powerful facility for radio astronomical research at meter wavelengths.

2.2 Radio Astronomy and Cosmos

Radio Astronomy is the study of the Universe through naturally produced radio waves reaching us from a variety of celestial objects. Like light waves, radio waves are also electromagnetic waves but with much longer wavelengths. Celestial objects usually radiate in different regions of the electromagnetic spectrum such as X-rays, ultra-violet, optical light, infra-red or radio waves depending upon their physical conditions such as temperature, magnetic field, etc.

With the use of the powerful radio telescopes, astronomers have discovered a series of remarkable objects and phenomena, such as radio galaxies, quasars, supernova, pulsars, interstellar molecules etc. The strongest waves generally arise from highly energetic relativistic electrons in the presence of magnetic fields created in aftermath of violent events occurring in stellar explosions and in the ultra-strong gravitational fields of the central regions of galaxies.

Apart from continuum radio waves (covering of a wide range of radio frequencies), atomic and molecular processes also give rise to line radiation confined to a relatively narrow frequency range. The most important of these lines occurs at 1420 MHz (wavelength of 21 cm) to hyperfine transition in the atoms of neutral Hydrogen - the most abundant consistent of universe. The study of this line radiation has not only provided a wealth of information on the structure of our own as well as of other nearby galaxies, but also the potential of revealing the state of the early Universe before the formation of galaxies.

2.3 Tools and techniques of radio astronomy

A radio telescope, the basic tool for exploring the radio universe, consists essentially of a reflector antenna, a feed and receiver system. The reflector focuses on the radio waves from a celestial object on the feed(usually a dipole or a horn) which collects the radio signals and feeds this weak signal to a sensitive low-noise amplifier to be further process by a sophisticated electronic receiver system. The two most important characteristics of a telescope are : high sensitivity to detect the weak radio waves from distant celestial objects and high angular resolution to distinguish features close together in the sky. The larger the size or 'collecting area' of a telescope is, the higher are its sensitivity and resolving power.

Because of the very long wave-lengths of radio waves(ranking between 1 cm and 10 meter) compared to less than a millionth of a meter for visible light, the resolution of even a large single radio telescope is relatively much poorer. At a wavelength of 1 meter for instance, a parabolic dish with a diameter of about 1 km would be required to obtain even the modest resolution of the human eye. By using an array of telescopes spread over tens of kilometers such interferometric techniques can be used to synthesize much larger telescopes with effective diameter equivalent to the maximum separation or 'baseline' between the most distant antennas in the array. This process is greatly aided by the rotation of the Earth that constantly changes the orientation and effective lengths of different interferometric baselines as seen from the radio source. Radio astronomers can in fact now obtain resolutions as high as thousandth of an arc second, much higher than possible with optical telescopes, by the technique of Very Long Baseline Interferometry (VLBI), in which radio signals are independently recorded by telescopes separates by thouthands of kilometers and subsequently correlated in a computer.

2.4 GMRT

GMRT is a large array of thirty fully steerable antennas, each 45 meters in diameter. The number and configuration of the dishes were optimized to meet the principal astrophysical objectives that require sensitivity at high angular resolution as well as ability to image radio emission from diffuse extended regions. 12 antennas are located in compact central array, about 1 km x 1 km in size. The remaining eighteen antennas are placed along the three arms of an approximately Y-shaped configuration with each arm extending to about 14 km from the array center. The multiplication or correlation of radio signals from all the 435 possible pairs of antennas or interferometers over several hours will thus enable radio images of celestial objects to be synthesized with a resolution equivalent to that obtainable with a single giant dish 25 kilometer in diameter. There are six operating frequency bands centered at 50, 153, 233, 327, 610 and 1420 MHz. The dual polarization operation is supported at all these bands. Optical fiber links are being used to distribute the local oscillator and control signals to the antennas from a central point and to bring back the IF signals. Then a spectral correlator and a Pulsar machine process the signal.

3. Correlator

3.1 Theory

A correlator system can be designed using two approaches:

- A XF (time multiplication) scheme where the signals from antennas are correlated (multiplied and accumulated) in hardware and then Fourier transformed in a computer doing a cross power spectrum.
- A FX (frequency multiplication) scheme where the signals from antennas are Fourier transformed in hardware and multiplied point by point to obtain a cross power spectrum.

$F1(f)*F2(f) \Leftrightarrow FT(f1(t)\otimes f2(t))$

GMRT is an FX correlator that crosses correlate polarized and not polarized signals of every antenna.

3.2 Application

The GMRT correlator System consists of 4 subsystems: sampler+delay subsystem, FFT subsystem, multiplier plus accumulator subsystem and long term accumulator. A control logic provides synchronisation for this fully pipeline system.

Correlator block diagramm

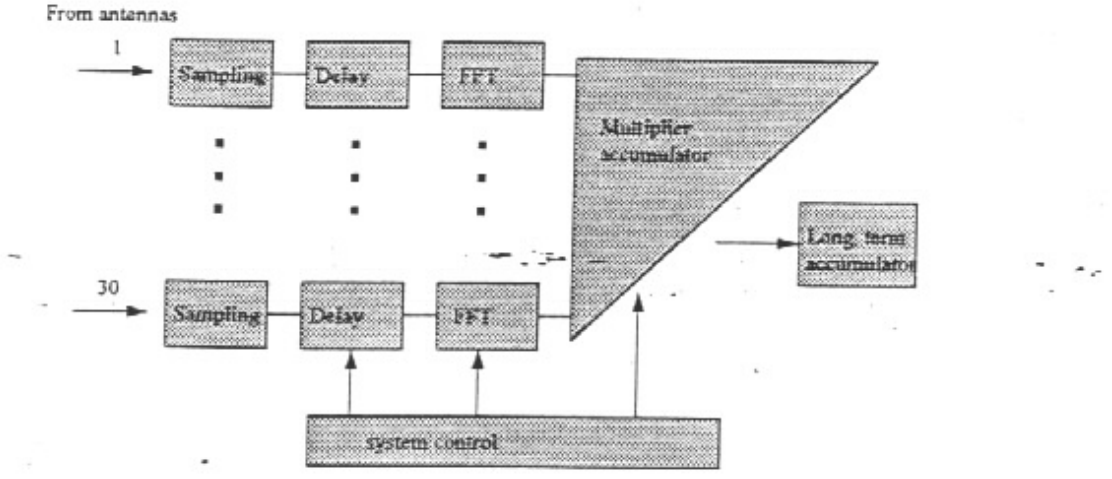


Figure 1

GMRT's correlator will work at 32 MHz to give 128 spectral channel output over the bandwidth ranging from 64 kHz to 16 MHz in the RR-LL polarisation mode. The sampler samples the analog signal at 32 MHz. The sampler has a 6 bit output witch is fed to the data preparation card and delay card. They can act on various options such

as input scaling, channel selection, walsh demodulation, gain calibration. Propagation and observation delays are compensated for every channel.

(Cross-correlating a pair of signals f1(t) and f2(t) is a function of relative time delay τ. When an interferometer observes a source, the instrumental delay τ_i is chosen to compensate the geometrical time delay τ_g for a phase center that is centered on the source.)

The FFT card computes the 512 point FFT using the basic radix 4 butterfly algorithm. An ASIC especially designed for the purpose of performing the radix 4 and radix 2 is being used in the FFT card. The MAC cards then multiplies and accumulates the FFT outputs on all 435 baselines. This is a short term integration for the maximum of 64 ms, the master control can then perform a long term accumulation. The large amount of possible cross correlation (435 for 30 antennas), makes the complexity of the system. At a same rate a large amount of data has to be exchanged and synchronized.

4. Schedule

4.1 Purpose

At present, the correlator group is involved in building 30 antenna correlator system. Basic correlator cards concepts are the same as cards already running on site but the correlator will connect 30 new FFT cards that have to be tested independently. The main purpose of the project is to realize an independent test bench for such a card. Data tests are sent and received by the system that moreover drive the real time FFT card process.

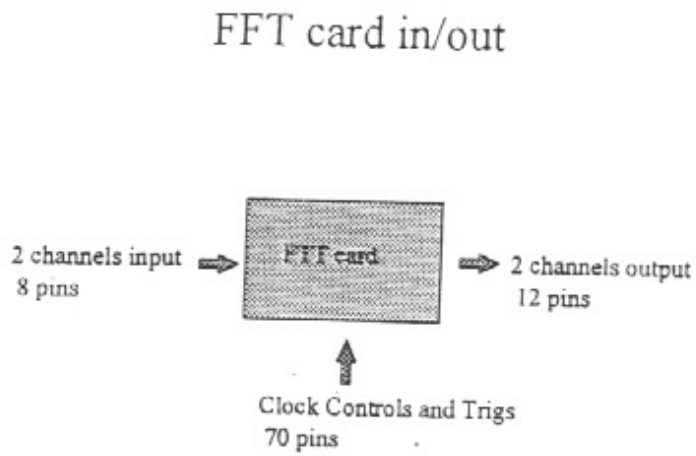


Figure 2

4.2 Functions

The system will load, send, drive, acquire and plot or analyze the result. That bench should validate a card according to new standards, but also enable an easier development on the card.

4.3 Constraints

An FFT card sends and receives a large number of signals at the same frequency. A universal bench with the same input and output number should be convenient but within 5 months a complete realization and design is difficult to achieve, especially because of the multilayer board realization delay. Therefore various boards already designed can be used for such an application. FFT is running at 32 MHz, consequently we have to synchronize input and output at the same rate. Two cards designed by the correlator group can send and receive at this rate 'delay control card' and 'acquisition card', they are linked by two extension cards to a single PC. The 'FFT control card' should select and drive stages of the FFT. Using such a board we will adapt to a convenient logic format and synchronize every signal.

The software driving the test bench should be clear and easily accessible by any user. Cards internal processor routines and communication process are available in C and assembly language. They should be adapted and collected in a common software.

5. Realization

5.1 Functional diagram

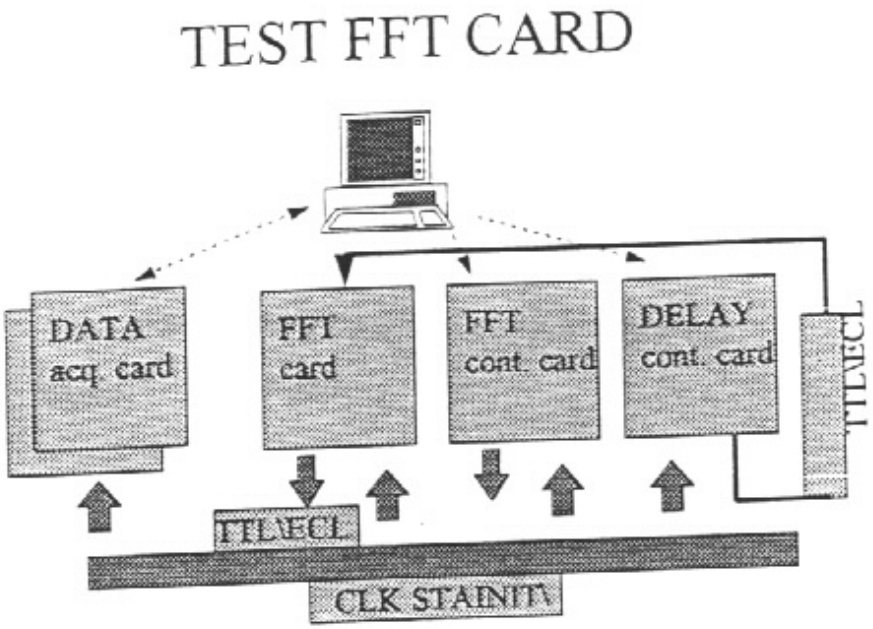


Figure 3

Mainly, the test bench manages a data flow from one stage to another, as shown above on the diagram. A main clock and a starting signal synchronize every stage of the pipeline.

FFT card data test and control input can be configured by software.

A PC sends serially a data file to the 'delay control card' used as a data delivering card. Consequently, patterns will run in a loop at the main frequency and after a logic format adaptation they will be the FFT card's inputs.

FFT card works with a master control called 'FFT control card'. This card works independently, running a sequence in a loop at the main clock frequency. A P.C. drives this control card through a serial link.

Once FFT is running two acquisition cards receive FFT outputs at the main frequency and acquire the signal in burst mode. Then the data can be acquired by the PC for analysis.

According to external constraints such as PCBs realization delays and high frequency interference, a specific 2 layer PCB backplane has been designed. 10 independent modules are necessary (described in the next sub section).

5.2 Hardware

5.2.1 Back-plane

The back-plane is two layers PCB designed, that connects 10 independent cards to one another:

1. Clock and STAINIT\ (main synchronization signal).
2. PC card interface for 4 INMOS 8 bits serial link.
3. PC card interface for 16 bit parallel acquisition.
4. Two ECL/TTL card converters for differential transmission at FFT input and output.
5. Delay control card for real time data test generation.
6. FFT control card drive FFT card.
7. Two acquisitions cards for real time data test acquisition.
8. FFT card test (to be tested).

Power is being supplied at -5V 0 +5V to every card.

FFT test bench back-plane is the only card designed for this application, with an independent ECL/TTL adaptation card. With only 2 layers, connection between FFT and control card were impossible. Consequently, wirewrapping is indispensable among the 2 connectors. Moreover we had to reduce distance from a connector to another to remove wirecoupling and interference possibilities.

5.2.2 FFT

The FFT card is a main board in the correlator system. It realizes a real time FFT algorithm. FFT card performs an FFT butterfly pipeline on 4 bit input and results in a 12 bit complex output data. Two FFT pipelines are processed in the same time and multiplexed in output every alternate cycle.

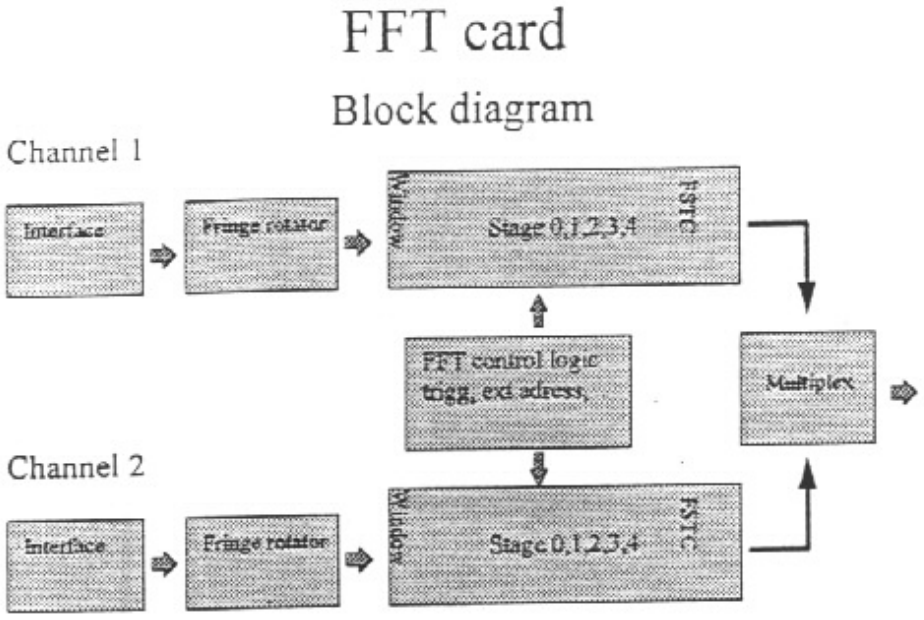


Figure 4

GMRT's correlator is based on the FFT card and especially on FFT ASIC. This ASIC has been developed for radiotelescope FFT processing. The GMRT's FFT cards connect and supply 2 FFT ASIC pipeline.

In GMRT, ASIC is running on Radix 4 and radix 2 configuration. 5 VLSI[1] custom ASIC[2] in cascade perform 5 stages FFT butterfly on 512 samples.

Each butterfly ASIC has an internal RAM for dynamic storage and multiplication but in FFT stages 1,2,3,4 it receives external Fourier twiddles factors. Meanwhile coefficients are automatically addressed in external RAM. These coefficients are periodically externally configurable. Moreover, stages 0, 1, 2, 3, 4 are being externally synchronized.

Various provisions such as fringe stopping, input window and automatic phase adaptation (FSTC) available on the card should be use in the next correlator version. Such options are also externally configurable. As a result, FFT control card provides most of the butterfly ASIC functions.

[1] VLSI

[2] ASIC

5.2.3 FFT control card

FFT control card is the interface between a PC and FFT card.

As explained earlier, FFT control card loads FFTs' control signals from a PC and sends them at a master clock rate in FFT cards. A DSP[3] drives a shared bus to load at any time Trigs and sequencer files. DSP can also drive FFT rack but in this project such a possibility is not being used. Once downloaded trigs and sequencer are running independently, because a counter addresses independent Rams at master clock rate.

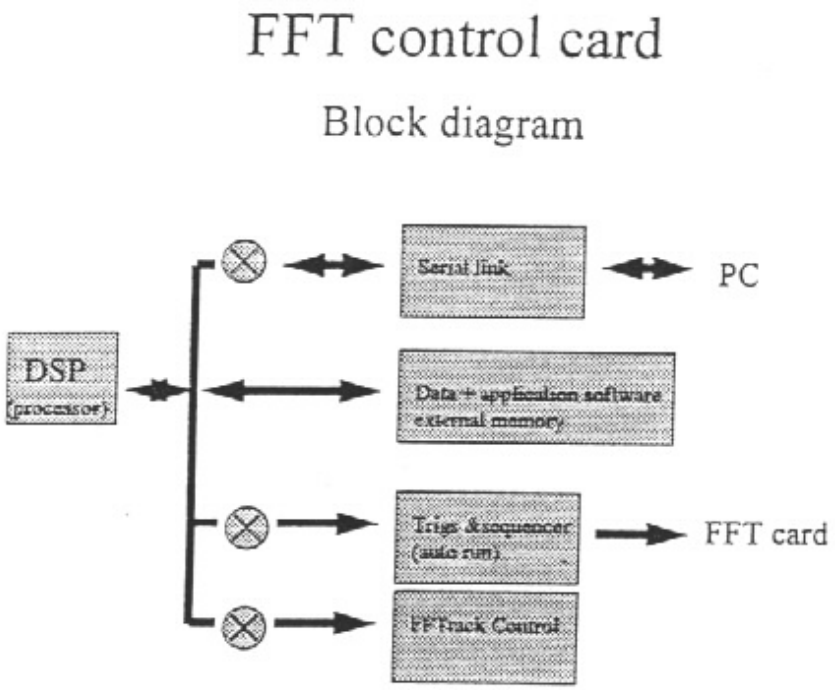


Figure 5

5.2.4 Delay control card

The Delay control card is the interface between a PC and delay cards in the main correlator system. For this particular project, the delay control card is the interface between a PC and FFT data input. 2*4 bit output drive 2 channels FFT input. The control card and the software have been modified for an external synchronization (STAINIT\). This synchronization has to be the same for both FFT control and Acquisition. A small ECL/TTL conversion board designed for this bench plugged between the test bench backplane and delay control card connector adapts TTL signal in a ECL differential format for FFT input.

The delay control card block diagram is approximately the same as FFT control card diagram (figure 5). Data comes serially from a PC and then is sent at a master clock rate in FFT cards. A DSP drives a shared bus to load at any time some new data files. Once downloaded data patterns are running independently (figure 6).

[3] Analog device ADSP2105

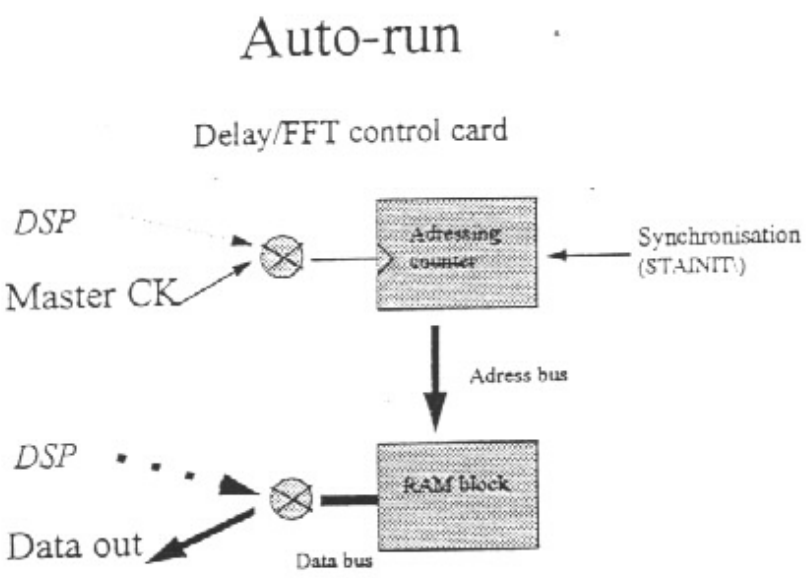


Figure 6

Both FFT card and Delay control card are using a same inMOS 8 bit in/out serial link. Working in an interrupt mode, the link can interrupt the DSP software and access the card at any time, to download software or data test. PC can also reset the card externally. In this particular project a specific PC 4 serial links card drives FFT control card and Delay control card.

5.2.5 Acquisition

Acquisition cards were used earlier for GMRT sampler output calibration. With some more time this card could be modified to improve from 8 bit to more than 12 bit simultaneous acquisition. In this project we require a 12 bit input, as a matter of fact we are using 2 acquisition cards in parallel. A specific PC interface can connect both acquisition cards to the PC bus. A software can then release an automatic acquisition in a memory and later on address the memory for a reception. Automatic acquisition is the same as 'auto-run' system used in control cards (figure 6), PC is then accessing RAM instead of writing. The 2 acquisition cards have been modified to get an external clock and top synchronization using previous chips.

5.3 Software

5.3.1 Overview

FFT test bench application software has been written in TURBO C and is available on every PC with 2 bus slot extensions, a graphic pilot and 1 Mb. RAM.

In a first time, every card used on the FFT test bench have been repaired and debugged one by one with the actual independent C softwares applied in the correlator lab. (C Protocol exchanges, DSP boots and running softwares are same). Secondly, necessary adaptation to delay control card DSP running software and acquisition card C protocol exchanges have been achieved. Finally C interface modules are running in an independent software. Some graphic and system TURBO C libraries have been written and are now available on the lab.

5.3.2 Possibilities

TSTFFT is accessible and can be used easily with the on-line help and rolling menu presentation. FFT input is configurable on both channels with squarewave sinewave, pulse or bin selection at any amplitude frequency or size. While loading FFT and delay control card TSTFFT plots a report on the exchange. Various types of acquisition representation are already available: real, imaginary, exponent part, spectrum or phase in many different formats and other options : long term acquisition, hardcopy, NCO configuration...

5.3.3 Structure

TSTFFT is a structured application software. Others libraries and functions used are included in appendix.

5.3.4 Delay control card DSP software

The delay control card has an external synchronization reset (STAINIT\) that has to be removed during a PC loading sequence (Ref. hardware application notes in appendix). A bit provision latched, controls the external reset. Otherwise, new Assembly language DSP software, TSTDATA1.DSP, is the same as the previous one.

5.3.5 New Acquisition protocol

For a complete bench synchronization, the acquisition card reset is only available at a synchronization signal. P.C. reset was the addressing counter reset signal, it is now only selected after an external synchronization.

Acquisition protocol is the following on figure 7:

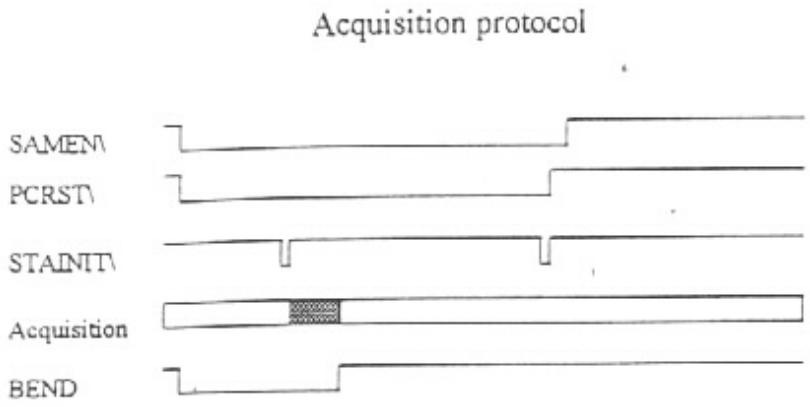


Figure 7

5.3.6 Pipeline alignment

Every card on the bench receives the same main clock. Meanwhile, phase of master clock will be tuned according to FFT card main frequency. Delay control card, FFT control card, acquisition cards have tunable delay provision to align latch data at every stage. We can tune delay control card's delay, sending a dirac in FFT card. Output spectrum has to be a constant. Once this phase is correctly tune and stable, we can adjust FFT control card's delay, sending a constant in input, a dirac should be the output. If there is no FFT output in that case, possibility is an extra clock delay at acquisition. This phase is card dependent, you can press left or right arrow to tune eventually one or two clock acquisition offsets. This offset is based on a reference acquisition card, the other acquisition card is then automatically aligned.

6. Results and comments

6.1 Results

The test bench has been tested on various FFT cards and on the actual FFT bench. Results in both cases are same. FFT numerical result is constant, nevertheless after some time especially at higher temperature computation noise appears distributed on every FFT channel. This can be tested switching off fans after few minutes and whatever the card. A real long time run is only possible at a constant low temperature.

The bench can be tested without any external data generator. Earlier a sine wave was computed in the input fringe PROM, delivering a 7 bit sine wave output depending on an addressing counter (NCO). We select a specific FFT channel (bin) sending a sine wave at a particular frequency (number of bin / Period). At NCO 1, spectrum is given on bin 10. The result is the following:

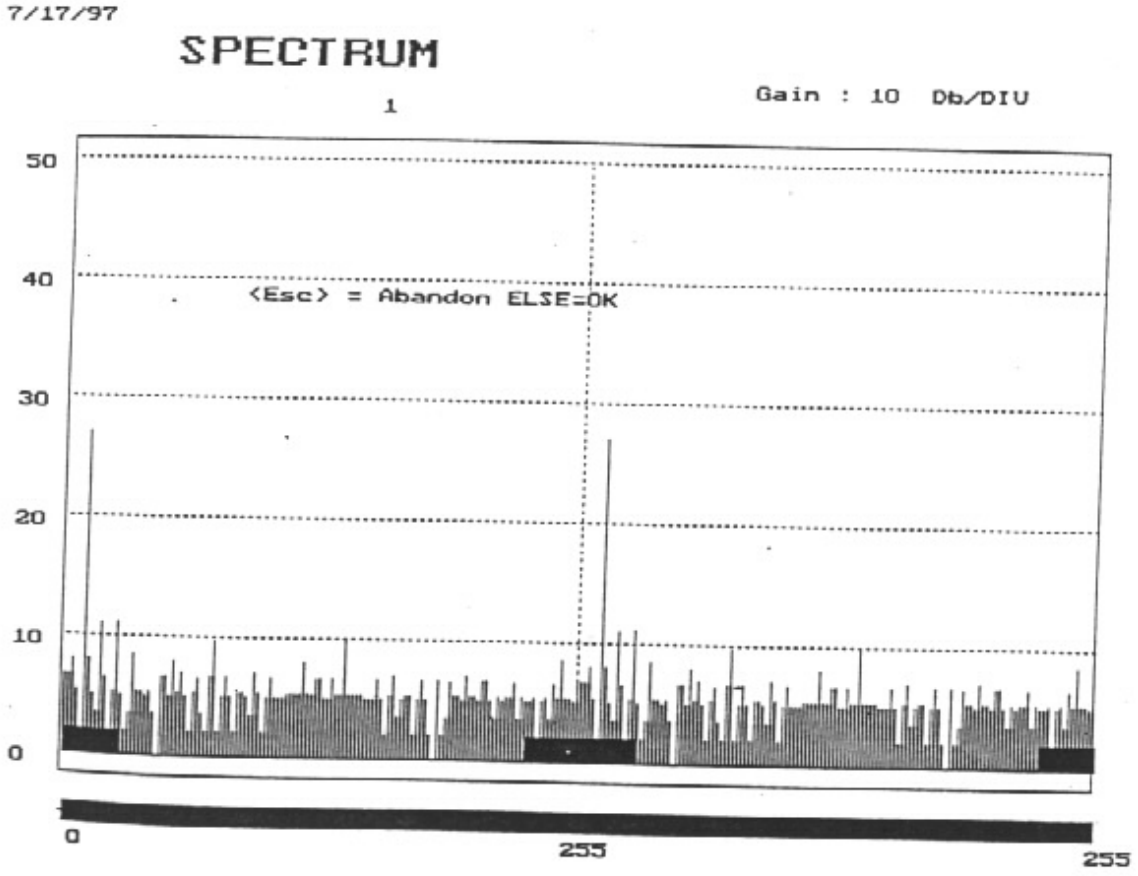


Figure 8

Spectrum scale is a 10log10 amplitude, this sine wave test is efficient for testing the FFT pipeline without the input stage.

Using the complete setup, a 4 bit to 7 bit look up table is used for FFT input. For a visual comparison, with a 4 bit sine wave input sent by delay control card, the result is the following:

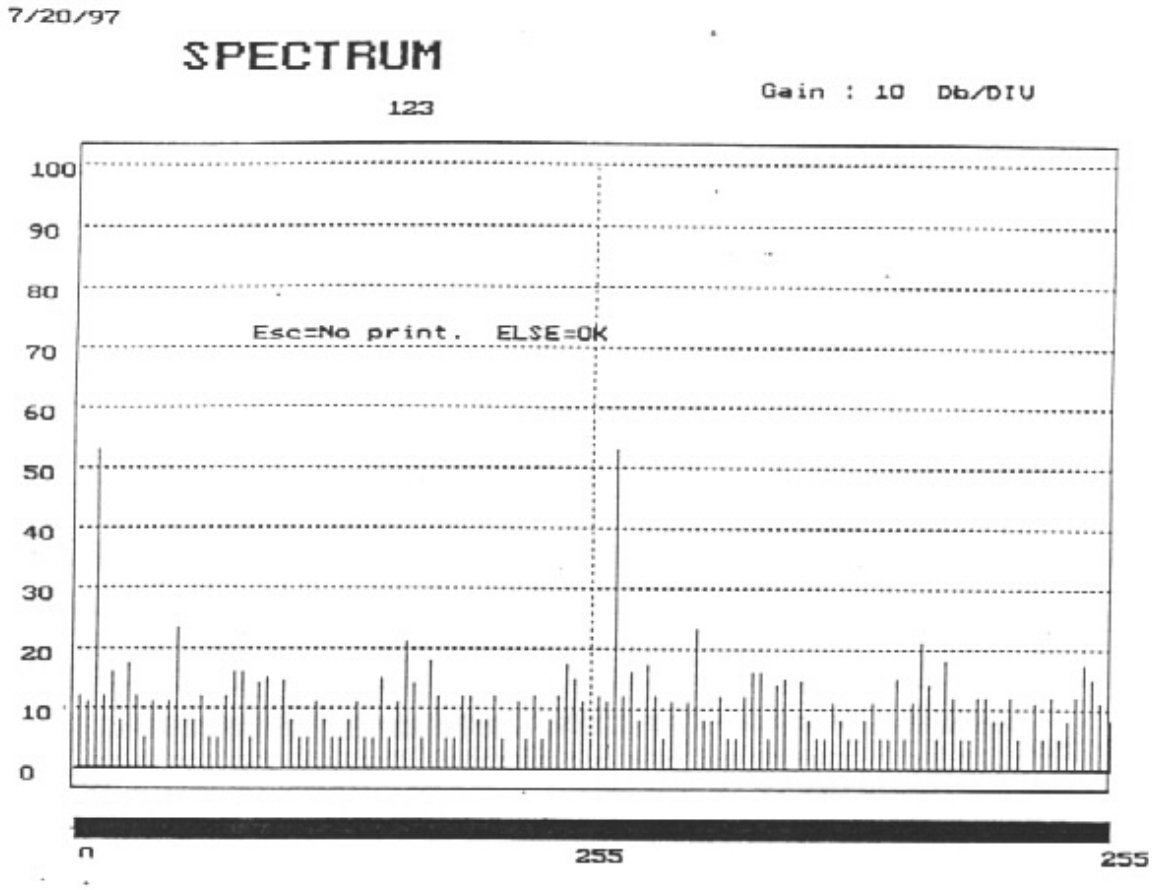


Figure 9

(Spectrum scale is a 20log10 amplitude).

For a particular bin and in both cases higher harmonic is 30 dB less than the main frequency. This is a constant processing noise due to truncations on the 4 bit sampling input but also due to twiddles factors truncation on 3 FFT butterflies' stages. ASIC internal truncation is 7,7,4 format and output truncation is 4,4,4 format. Various effects of truncation can be shown using a basic simulation.

The FFT test bench has already been used to develop the input FFT fringe PROM for fringe stopping. Fringe stopping demodulates the input signal at a particular bin according to observation parameters. For fringe stopping command, a counter addresses a reference sine wave multiplied by the input signal. The counter speed determines the sine wave frequency. If FFT input is DC, after fringe stopping it becomes a 7 bit sine wave combination sent to the FFT pipeline. On figure 10, we can see the result after and before debugging the fringe PROM on channel 10.

(On the graph, result with new fringe PROM is channel 1, with older fringe PROM result is channel 2.)

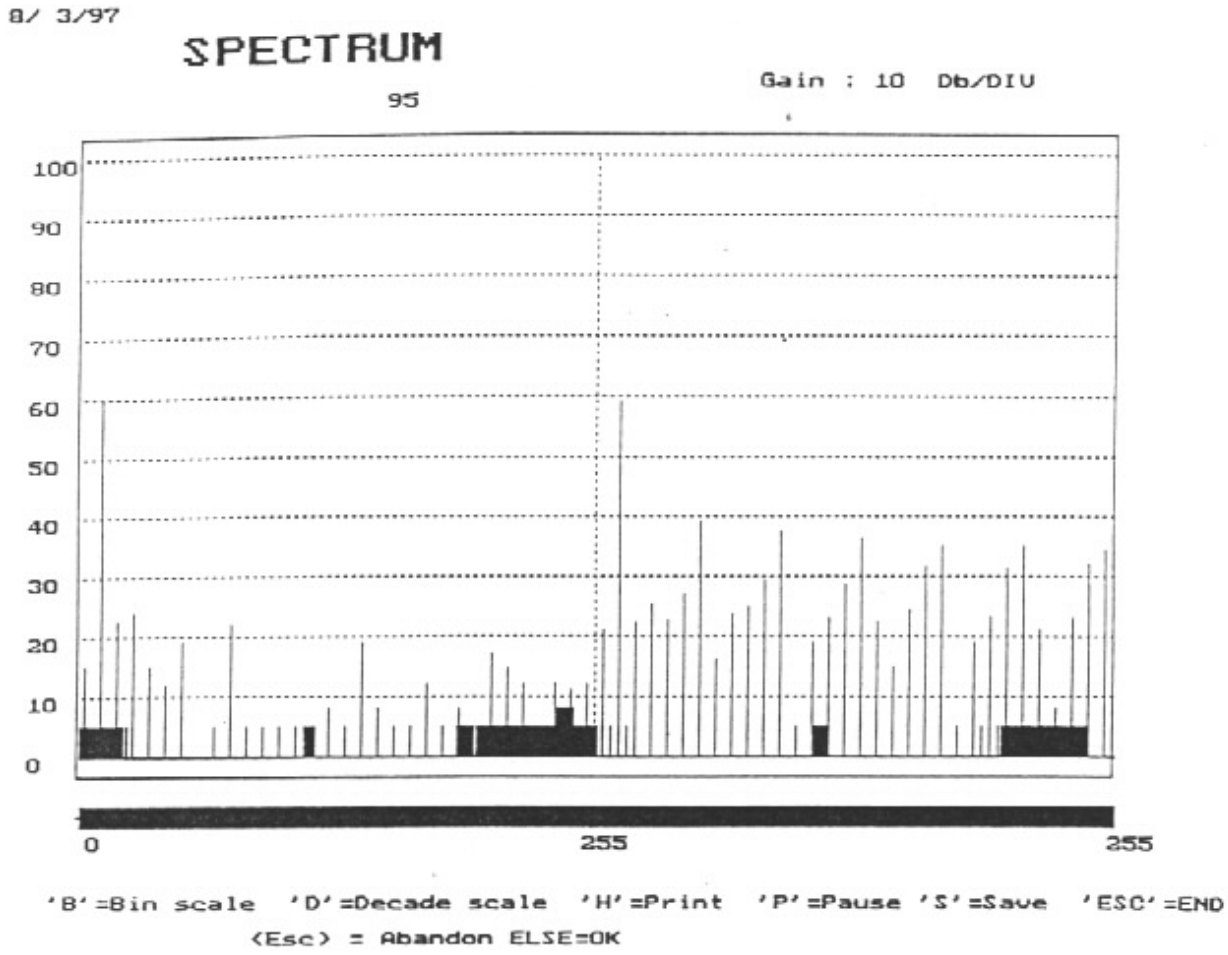


Figure 10

6.2 Comments

6.2.1 general

This bench seems useful especially for a better and much easier debugging operation. Moreover as long as fringe stopping and automatic phase adaptation are not running completely, the FFT control card test bench will be used for FFT card development. Therefore, at a basic debugging stage this bench is not required, existing tools and DSP FFT control card software can test data inits and commands on FFT mother board.

6.2.2 performance

The FFT card generates a processing noise that can not be removed directly by average. Consequently, even if an astronomer studies a single particular FFT channel, a correlation noise can be due to other channels computation. After accumulation this noise is added and subtracted on every channel in such a way that it is finally not drastically high. To measure this level of noise a test on the 'FFT test bench' consists in sending and recording FFT output on every channel. In this particular case input 4 bit truncation noise and twiddles factors computation noise are taken into account. In fact the first 4 bit truncation effect can be removed using a noise generator (result from

simulation) and average. Figure 11 represents an acquisition and accumulation after sending a sine wave in every FFT channel.

1. Amplitude_cumul[i]=$\sum_{k=0,255}$ Amplitude[i,k]
2. Amplitude_erreur[i]= Amplitude_cumul[i]-Amplitude[i,i]

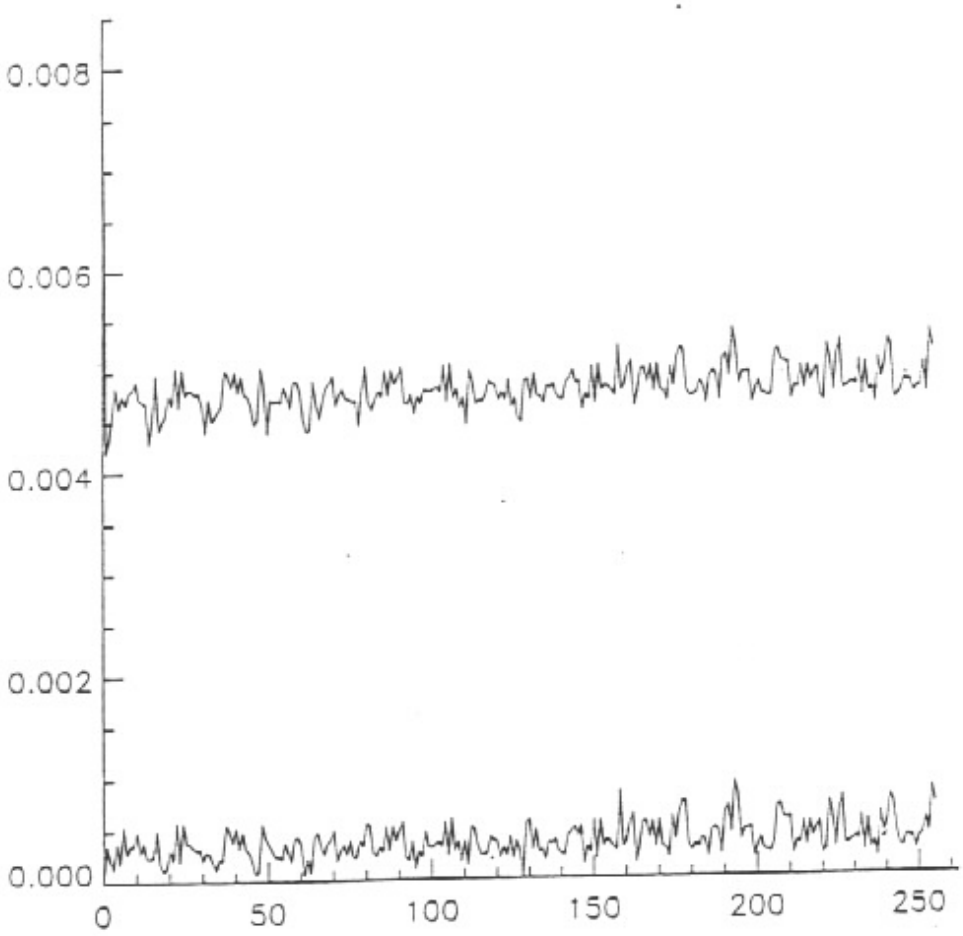


Figure 11

Error due to other channels in a main bin amplitude is 7.5% average and 3% variance.

Figure 12 gives the relative error amplitude. It is interesting to notice the truncation effect of the FFT on a particular channel. Because of the FFT symmetry channel 128 is not affected by the others.

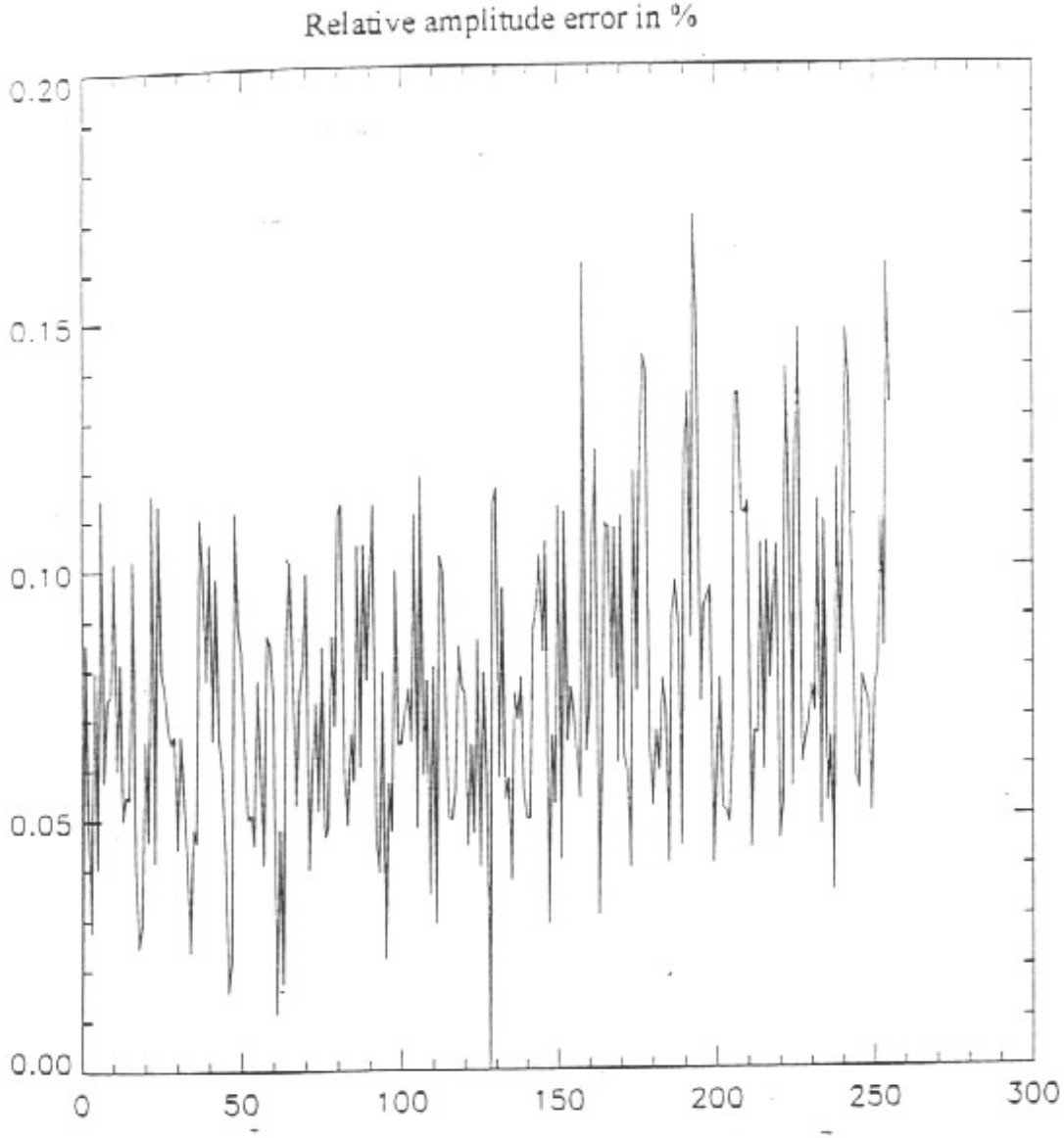


Figure 12

The same type of relative error can be given too for the phase, average error is then 1.46 degree with a 1.5 degree variance.

1. Figure 13, Phase[i]=atan($\Sigma_{k=0,255}$ A[i,k])

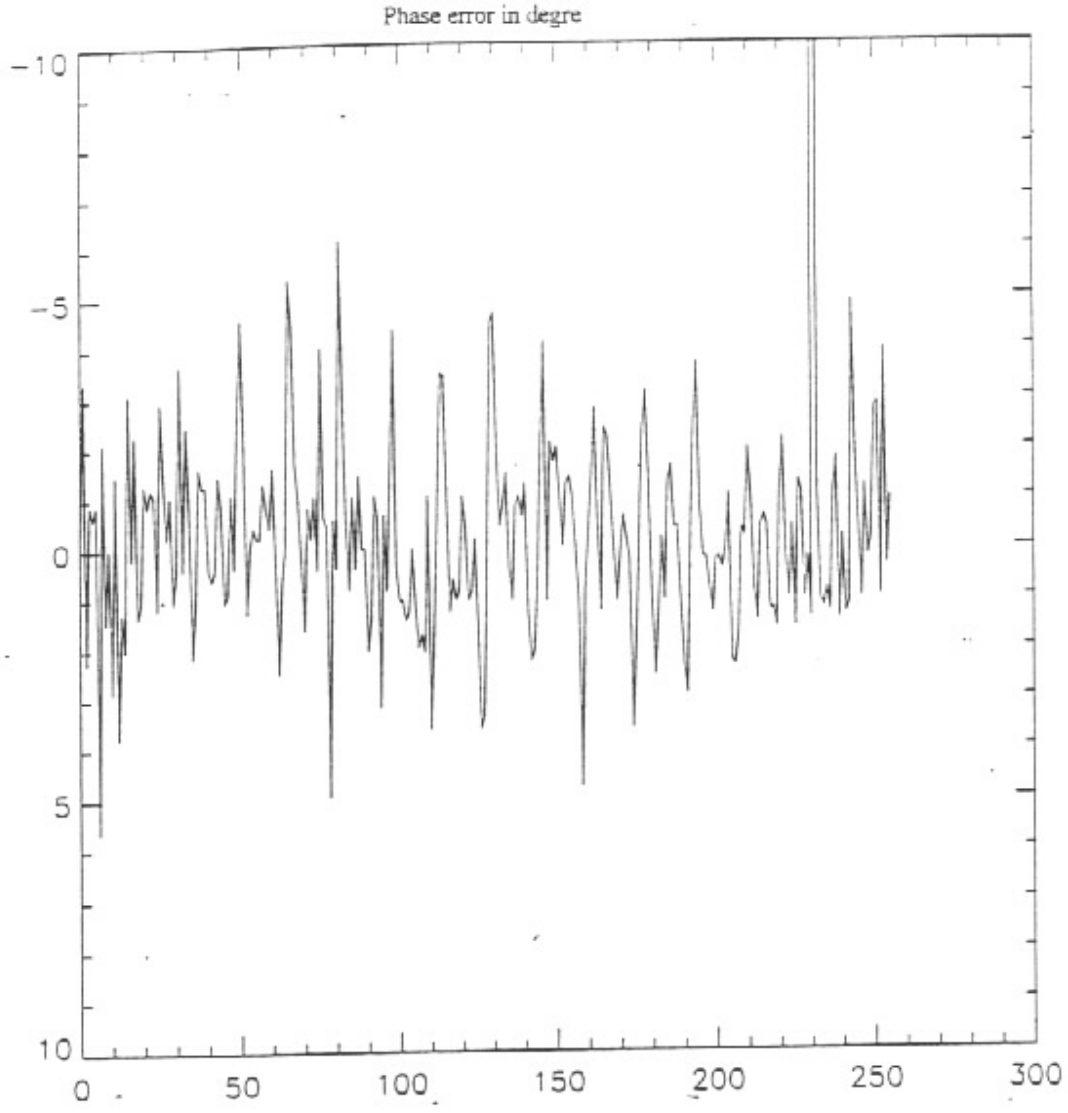


Figure 13

6.2.3 Simulation

With a basic Fourier transform software simulation at a particular bin, we can see an important similarity with the hardware result. This simulation takes the various truncations into account. On figure 14, 3 graphics show the 4 bit input truncation, the twiddles factors 5 bits and 4,4,4 output effect on channel 10.

Without averaging, 4 bit input truncate is the most important effect, maximum noise is at --30dB after computation by an accurate FFT function. Twiddles factors maximum noise effect is measured at -35dB.

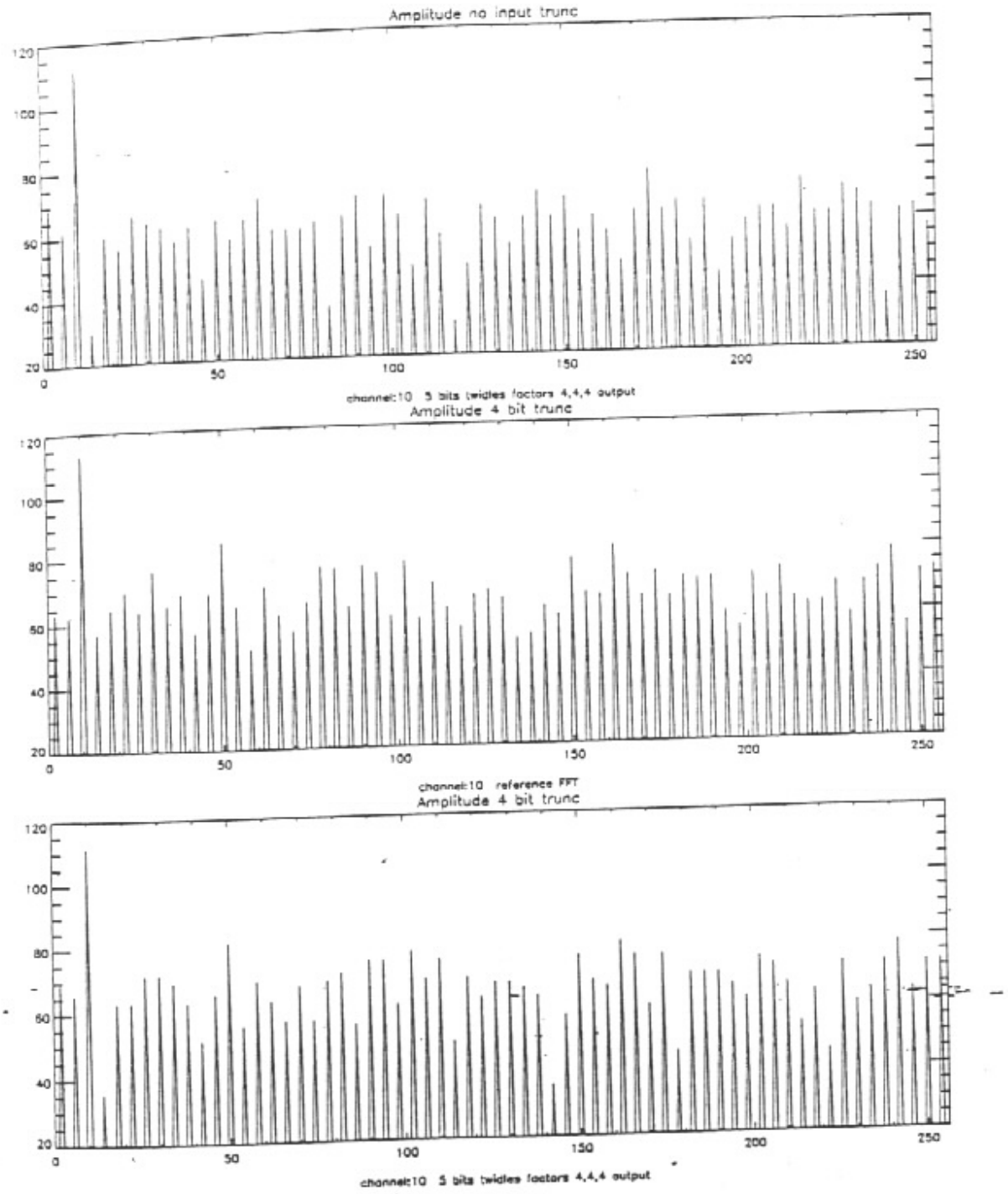


Figure 14

Sine/Cos truncation effect is the most important systematic processing error in the actual system. The FFT control card that sends twiddles factors is used with only one specific table. To improve the accuracy, FFTs twiddle factors can be truncated differently and loaded in a 32 ko provision memory (64 other twiddle factors tables). After a simulation we can see that truncate effect can be then reduced after an average.

6.2.4 Swept-frequency test signal

The swept frequency test consists in taking the transforms of ten test signals at equal intervals between channels 10 and 11. The frequency step is 0.1. Figure 15 show the FFT amplitude in channels 10 and 11 for both real FX FFT and a reference FFT.

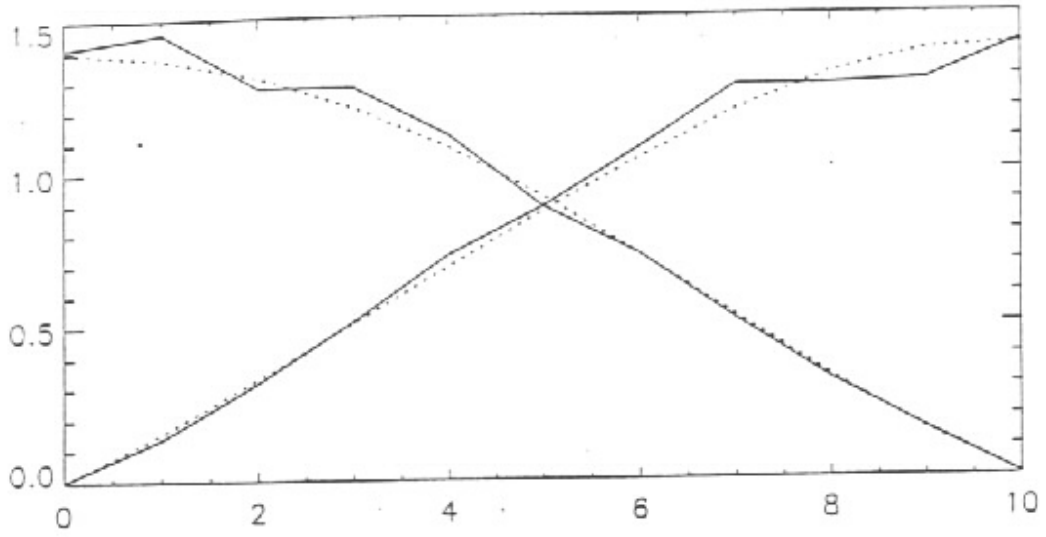
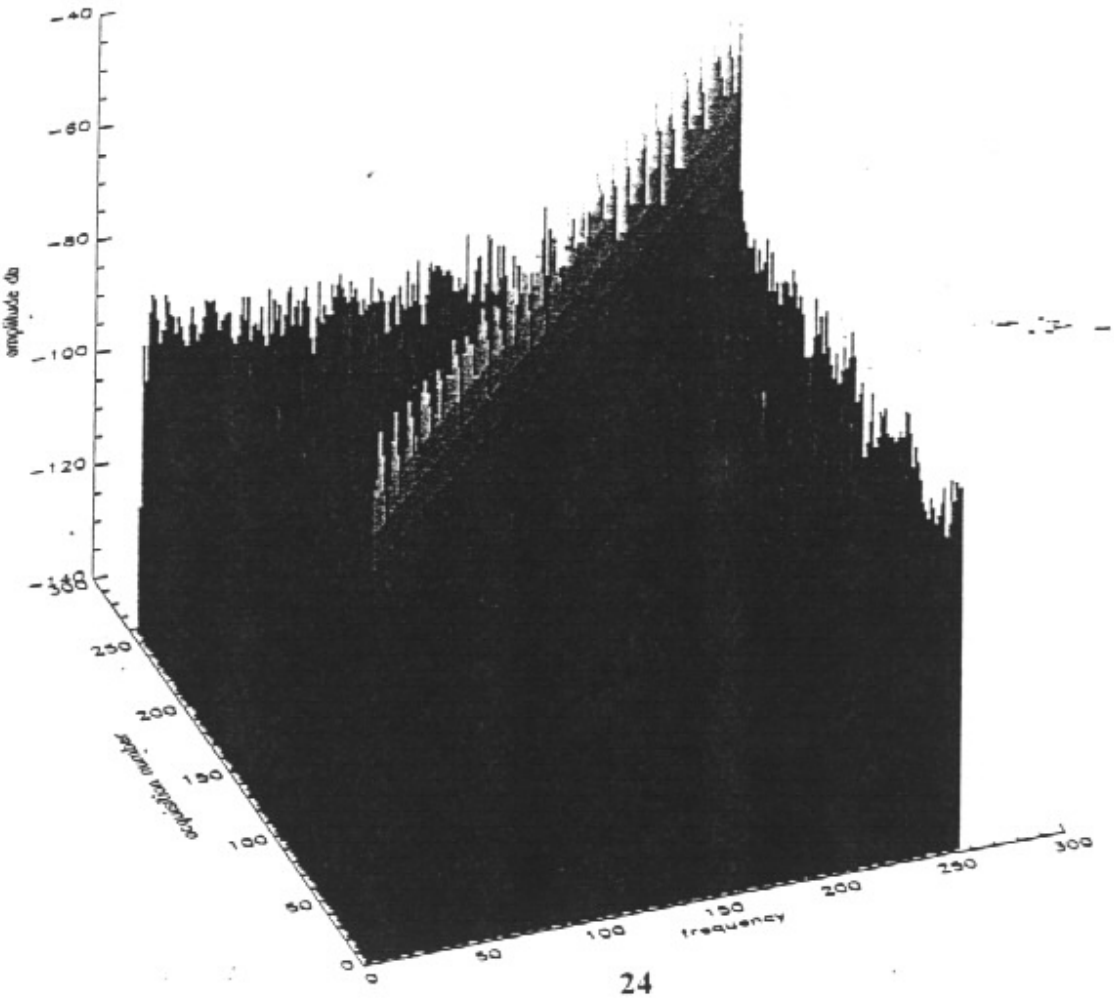


Figure 15

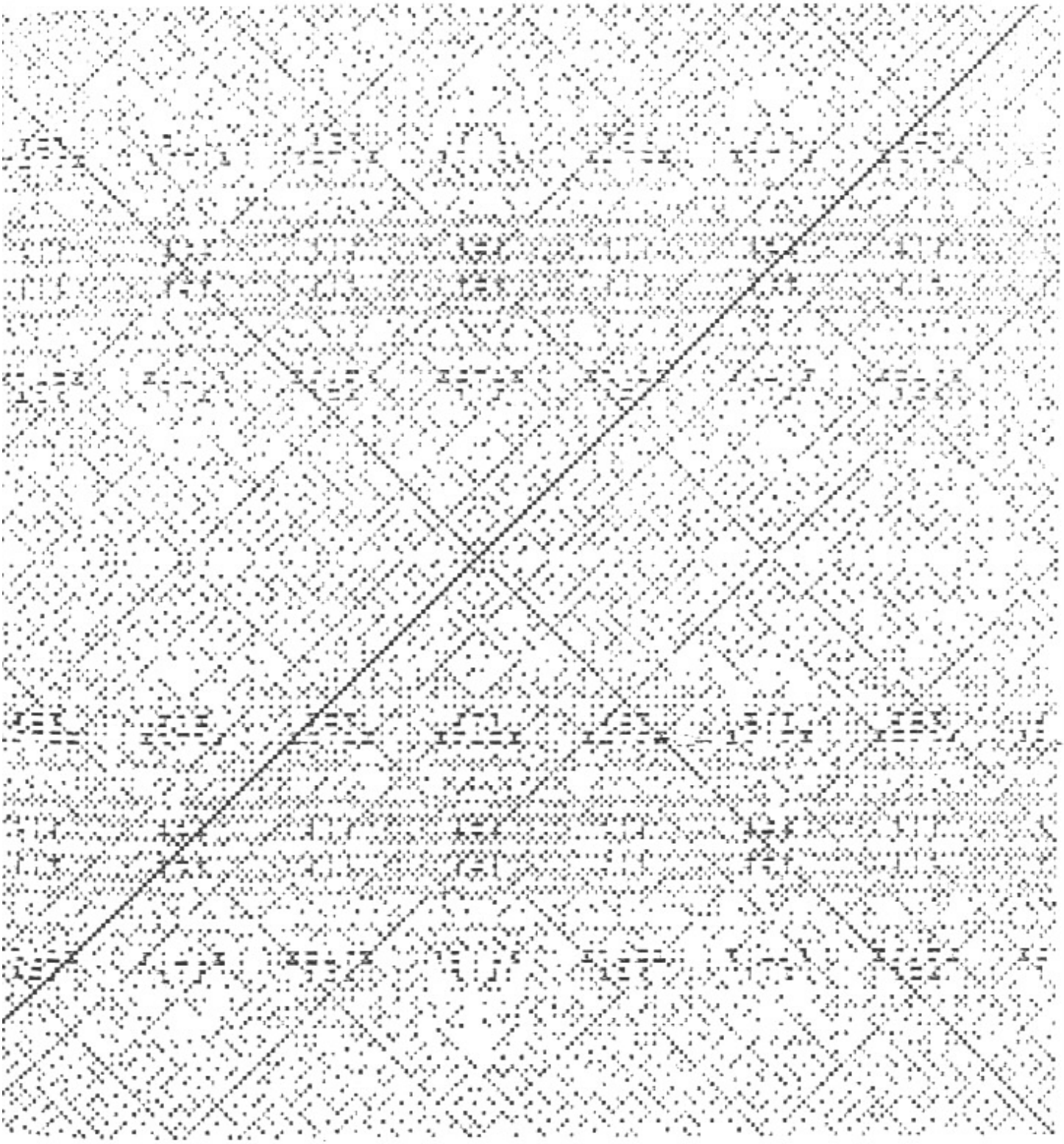
6.2.5 3D FFT map

We can have a better idea of the FFT output, plotting the result of 256 acquisitions by 256 channels on a 3 dimensional representation.



This contour representation shows the FFT distribution and especially textures symmetry.

1. Amplitude for 256 channels by 256 acquisitions (horizontal) at 256 frequencies (vertical).



7. Conclusion

I joined for my final year engineering training period, an important Indian institute working on a huge and long term radio telescope project. In Pune, I had the opportunity to join the correlator group working out a large digital real time system.

At the present stage correlator group prepares the 30 antenna correlator system. A much larger amount of data transfer and multiplication of electronic cards will increase complexity and failure risks. Card's conception is the same as cards already running on site but the correlator will connect 30 new FFT cards that have to be tested independently.

The main purpose of the project was to realize an independent test bench for such a card. Data tests are sent and received by the system that moreover drives the real time FFT card process. That bench validates a card according to new standards, but also enable an easier development on the card. The interactive access to FFT output gives a direct visualization after processing and truncates effects. Some useful FFT specifications can already be apprehended on the bench.

Appendix gives technical details on the bench hardware and software realization with schematics of every card combined in the setup.

Bibliography

An overview of the VLBA correlator, Ray Escoffier,Sept., 1987

Simulation results for the VLBA correlator, John Benson, Chuk Broadwell, oct., 1987

Test on the VLBA FX-style FFT, John Benson, Jan., 1987

Correlator system for GMRT preliminary report, S.Vijayanarasimha, Feb., 1988

An introduction to Radio Astronomy, B. Burke, F. Graham-Smith, Cambridge university press, 1997

Appendix

Hardware application Notes

Presentation

The main purpose of the project is to test FFT card, thanks to a PC and check its work. The test is realized with boards already used in the correlator lab.
PC leads patterns in the 1k*2 bytes memory from the delay control card. Then patterns are thrown at 32 MHz in the 2 inputs' channels of the FFT card. FFT results go to the 64k bytes RAM of 2 sampler acquisition boards. At the same time, the FFT control card selects and drives stages of the FFT card.
The flow is synchronized externally with a period of 66.048 ms (4096*516*32 MHz clock period).

Realization notes

Delay control card

A conversion board changes the TESTD[0..7] into ECL thanks to a conversion card plugged on the backplane. STAINIT, ECLCK32 and the power supply are also taken from the backplane. On the backplane, a 13x2 map connects the bus output to the FFT input. Modifications are necessary to synchronize the CLR\ with STAINIT in order to reset the counter addressing the RAM. This can be realized with 3 gates unused U18C, U29,U19.

FFT control card

The FFT control card generates every inits and trigs necessary for the FFT. A DSP software synchronized by STAINIT\ is charged apart from a PC serial link.

FFT card

The FFT card is selected by CARDSEL\ corresponding to CARDSEL\0.

Sampler acquisition board

2 sampler acquisition boards are necessary for the 4x3 bit FFT multiplexed output. They are synchronized by STAINIT and an external 32Mhz clock. Those signals are transmitted in ECL and converted in the DAC section. A strap is necessary between U20 5 and U11 1 for CK32. An OR gate (U15 D) between STAINIT\ and PCRST\ reset the address counters and BEND. STAINIT\ is taken from U20 4 (J5.1) and PCRST\ is taken from the connector.
The backplane connects the PC acquisition board to the 2 sampler acquisition boards.

Backplane

The backplane is a 2 layers' board. Meanwhile the 4 rows FFT and FFT control cards cannot be connected properly. S3TRG[0..9] and NCSRCKP-N on the same row are external connections. Connect also BR\ and IRQ0\ to VCC.
Every Clock and STAINIT\ is wrapped on jumpers next to connectors. Every clock phase can be adjusted on each board. On the actual bench power distribution is given by a VCC and GND copper bar. Effectively, FFT card is 5 Amp maximum input current that can not be safely supplied by the actual routing wire wide.

If another backplane has to be done, I propose not to solder FFT card connector inside but reversed, on the reverse side. In the present system a connector is wire wrapped and reversed. The first reason is the connection problem due to the FFT connector reversed on every FFT card. It was not noticed on the schematic consequently this was not taken into account for the design. The FFT connector is rigid enough to maintain a card by itself. Nevertheless another guide can be added reverse also. This mistake is finally an advantage in the sense that once connected to the other side, this bench can also be used for FFT debugging even easier than in the present bench. When designed this bench was not supposed to be used that way because backplane is a 2 layer PCB only. It was impossible to extent the width between the FFT and FFT card connection because of interferences and wire coupling. The only complication will be the remaining trigs wire wrapping. A convenient solution is to wire wrap before soldering FFT connector. For power distribution a large wire can be added between pin 1 and 2 for VCC and 31, 32 for GND and then solder on the backside (this has to be done before soldering the FFT connector).

Software application notes

```
*********************************************************
      6/7/97
      Alliot Sylvain
      Manual for TSTFFT project
      install.TXT
*********************************************************
```

1 sources :

Create a subdirectory for the project

```
C:\ <Enter>
MD TSTFFT <Enter>
CD TSTFFT
UNZIP TSTFFT.ZIP
.....
..\TSTFFT\*
..\TSTFFT\FFT\*
..\TSTFFT\DLYDPC\*
.....
```

2 Configuration of Turbo C:

---

open the project:

---

files are colected in a common project called TSTFFT.PRJ

- 'Projet' (Alt P)
- 'Open project'
- press *.PRJ and select TSTFFT.PRJ
- load one file on the screen.

compilation:

Option large 'LARGE':

- menu Options (Alt O)
- 'Compiler'
- 'Code generation'
- 'Model Large'

Compilation and link editor:

- Ask for menu 'Compile' (Alt C)
- take second ligne:
  MAKE EXE File: TSTFFT.EXE
- enter .....

****

6/7/97
Alliot Sylvain
Manual for TSTFFT project
ARCHITEC.TXT

****

DIRECTORY :

I. ..\TSTFFT
files used for FFT test bench only

II. ..\TSTFFT\FFT
files used for FFT control card independently
including the original software for manual operations

III. ..\TSTFFT\DLYDPC
files used for DLY control card independently
including the original software for manual operations

TSTFFT.PRJ main file. files of TSTFFT.exe:

---

tool1.c
samacq.c
cntrl.c
programm.c
windows.c
diagno.c
printer.c
submenu.c
submenu2.c
genedata.c

TOOL1.C
usefull subroutines sound and system fonctions

```
void sound1();
void sound2();
void sound3();
void sound4();
void date_system();
void shift_right(int,int);
```

SAMACQ.C
Plot the sampler acquisition board result
FOR FFT TEST BENCH ONLY another software is written
in C for a single acquisition card and a real time FFT computation
Channel A,B,C :
-> 4096 * 4 bits

-> FFT 512 * 2 * 4 bits
Store on "back.bat" in the main directory a 4096 sequence

```
        // init external variables
    void init();
        // clean the screen
    void clean();
        // clean the plot area
    void clean_plot();
        // get date with a text standard format
    void date_text_format();
        // first screen with title, menu, rectangle, divisions
    void title_time();
        // frequency screen with title, menu, rectangle
    void title_frequency();
        // phase screen with title, menu, rectangle
    void division();
        // Plot FFT decades
    void decade();
        // save channel A & B on ..\back.bat
    void PauseSave();
        // select the menu      end,pause,reverse,fft_on,scale
    void menu_selection();
        // direct plot after acquisition
    void plot_graph();
        // plot in fix point format
    double fix_point_format(char);
        // plot spectrum
    void spectrum();
    void error_message();
    void acquisition();
    void reception();
        // reception from the sampler acquisition of 64ko memory
        // initialisation of '..\acq.dat' for channel A and B
    void reception_full();
    void samacq(int);
        // test stability substract acquisitions
    int test_stable_n(int,int*,int*,int*);
        // test stability substract 2 acquisitions  NTEST times
    void test_stability();
```

CNTRLFFT.C
to be used with the 'PC4LINK' addon card.
Use link0 at @ 0x300

```
    reset_control_card()
    void reset_link(void)
    int check_link0_in()
```

```
        // The following procedure reads bytes from the opened file and sends
        // them on the inmos link.
    send_bytes()
    reset_link1()
        // The following procedure check if a word is received
        // on the inmos link1.
    int check_link1_in()
        // The following procedure reads bytes from the opened file and sends
        // them on the inmos link.
    send_bytes_link1()
        // FFT control card load and execute TCNRAM.EXE
        // result in information window
    void cfft()
        // Delay control card load and execute TSTDATA1.EXE
        // result in information window
    void cdlydpc()
        // Delay control card + FFT control card
        // test communication result in information window
    void test_link()
```

PROGRAMM.C
main software for FFTTST.PRJ project
main menu

```
    void message_module_missing()
    void message_simple()
    void message_menu_principal()
    void up_button_main_menu()
    void arrow_cursor_principal()
    int decode_keyboard()
    int decode_specific_key()
    int wait_keypressed()
    void manage_main_menu()
    int init_software()
    void main()
```

WINDOWS.C
fonction library managing C windows

```
    void    create_dial_window();
    void    create_information_window();
    void    clean_information_windows();
    void    block_title();
    void    first_screen();
    void    draw_button(int,int,int,int,int,int,unsigned char*);
    void    clean_dial_window();
    void    main_menu_button();
```

```
        void    get_main_menu();
        void    clean_data_window();
        void    get_initial_info();

-------------------------------------------------
DIAGNO.C
System informations and diagnostic
-------------------------------------------------
        void mem_free()

-------------------------------------------------
PRINTER.C
Print fonctions for LASERJET and compatibles on LPT1
-------------------------------------------------
                // End hardcopy
        int message_end_print()
                // Screen copy to laserjet
        void copy_screen_laserjet2(x1,y1,x2,y2,resolution)
        int prepare_printer()
        void print_screen()

-------------------------------------------------
SUBMENU.C
Subroutines to manage a submenu
init submenu for test data generation
-------------------------------------------------
        void messages_menu_subject()
        void submenu_subject()
        void up_buton_subject()
        void action_arrow()
        int menu_choice_subject()

-------------------------------------------------
SUBMENU2.C
Subroutines to manage a submenu
init submenu for plot
-------------------------------------------------
        void messages_menu_acquisition();
        void submenu_acquisition();
        void action2_arrow();
        int menu_choice_acquisition();

-------------------------------------------------
GENEDATA.C
Generate test patterns for delay control card
according to the FFT card input format
The output is written to tstdata.out
-------------------------------------------------
                // adapt y to FFT format
```

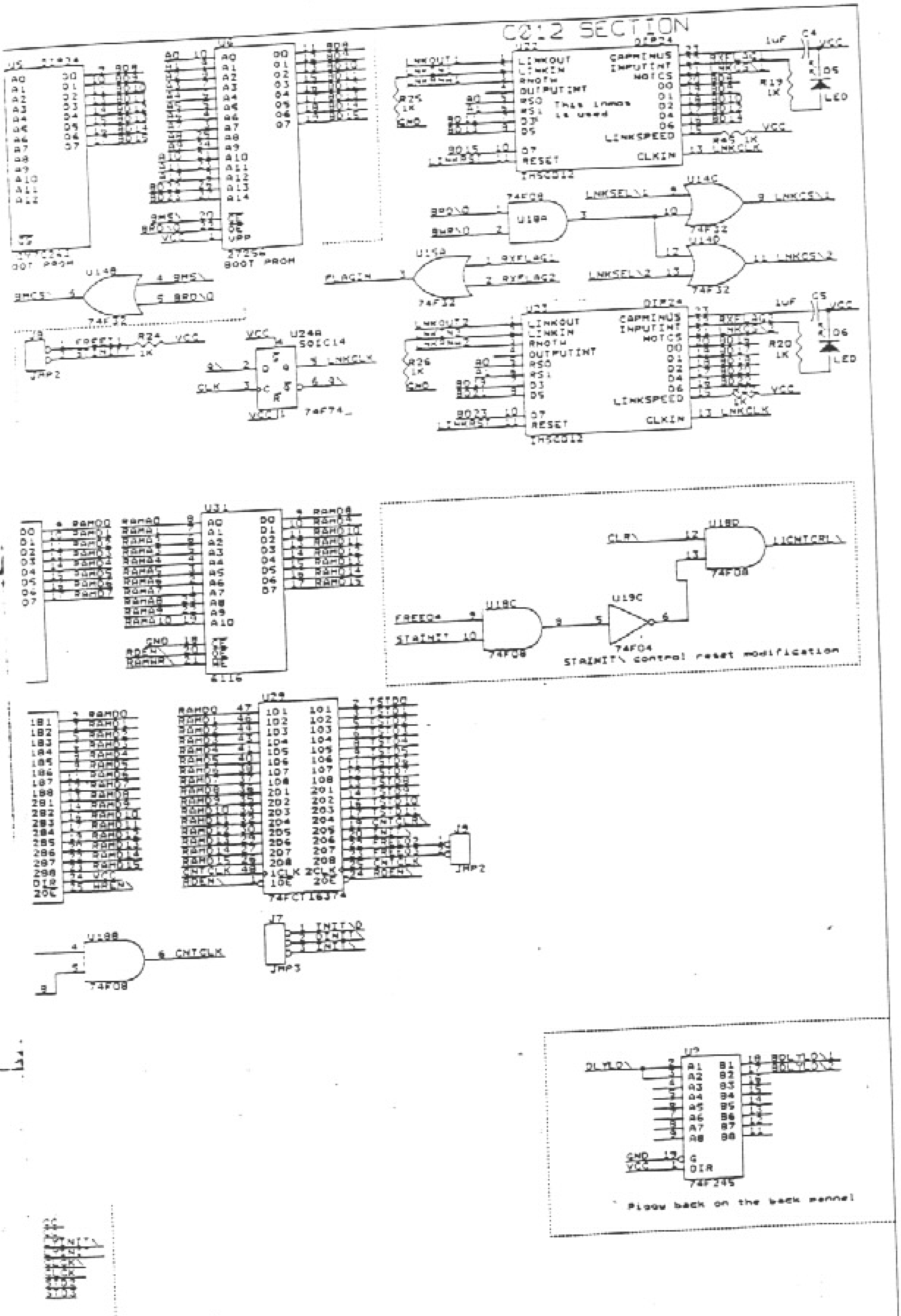
```
        // FFT input format X3 X2 X1 X0 |-> X3=signe, X2,X1,X0 value
    unsigned int format_fft(double y, unsigned int ampl, int ch)
        // send a sine wave in a particular bin of the FFT
    void signal_bin(unsigned int amp, unsigned int nfreq )
        // send a sine wave according to a periode
    void signal_sine(unsigned int amp, unsigned int nperiod )
        // send a square wave according to a periode
    void signal_square(unsigned int amp, unsigned int nperiod)
        // send a pulse according to a size
    void signal_pulse(unsigned int amp, unsigned int size)
        // interface for sinewave generation
    void genesine()
        // interface for square wave generation
    void genesquare()
        // interface for pulse generation
    void genepulse()
        // interface for generating a sine wave at a bin frequency
    void genebin()
```

../TSTFFT/FFT/*.*

- IMSPAK.OUT
contains the FFT control card application software
already compiled and at DSP format.
- IMSPAK.C
Is used to change the DSP FFT control card apllication
software. (not used directly by the application).
- FC4LNK.C
Basic application software testing FFT control card.
(not used directly by the application).
! can modify IMSPAK.OUT

../TSTFFT/DLYDPC/*.*

- IMSPAK1.OUT
contains the Delay control card application software
already compiled and at DSP format.
- IMSPAK1.C
Is used to change the DSP Delay control card application
software. (not used directly by the application).
- FC2105B.C
Basic application software testing Delay control card.
(not used directly by the application).
! can modify IMSPAK1.OUT
- TSTDATA.OUT
File that TSTFFT download to delay control card



R1–R44

C1–C5 = TANATALUM CAPS.

JMP2 = J5,J8,J9

JMP3 = J3,J4,J7,J10

HEADER 5X2 = J1,J2,J6

The following modifications have been made in the dly cntrl card:

(1) SINIT\ is not captured in the cntrl card.

(2) DACINIT\2 is produced using the FREE01 buffer.

(3) DLYLD\ is buffered to get 2 o/ps (piggy back).

MCRA–TIFR	
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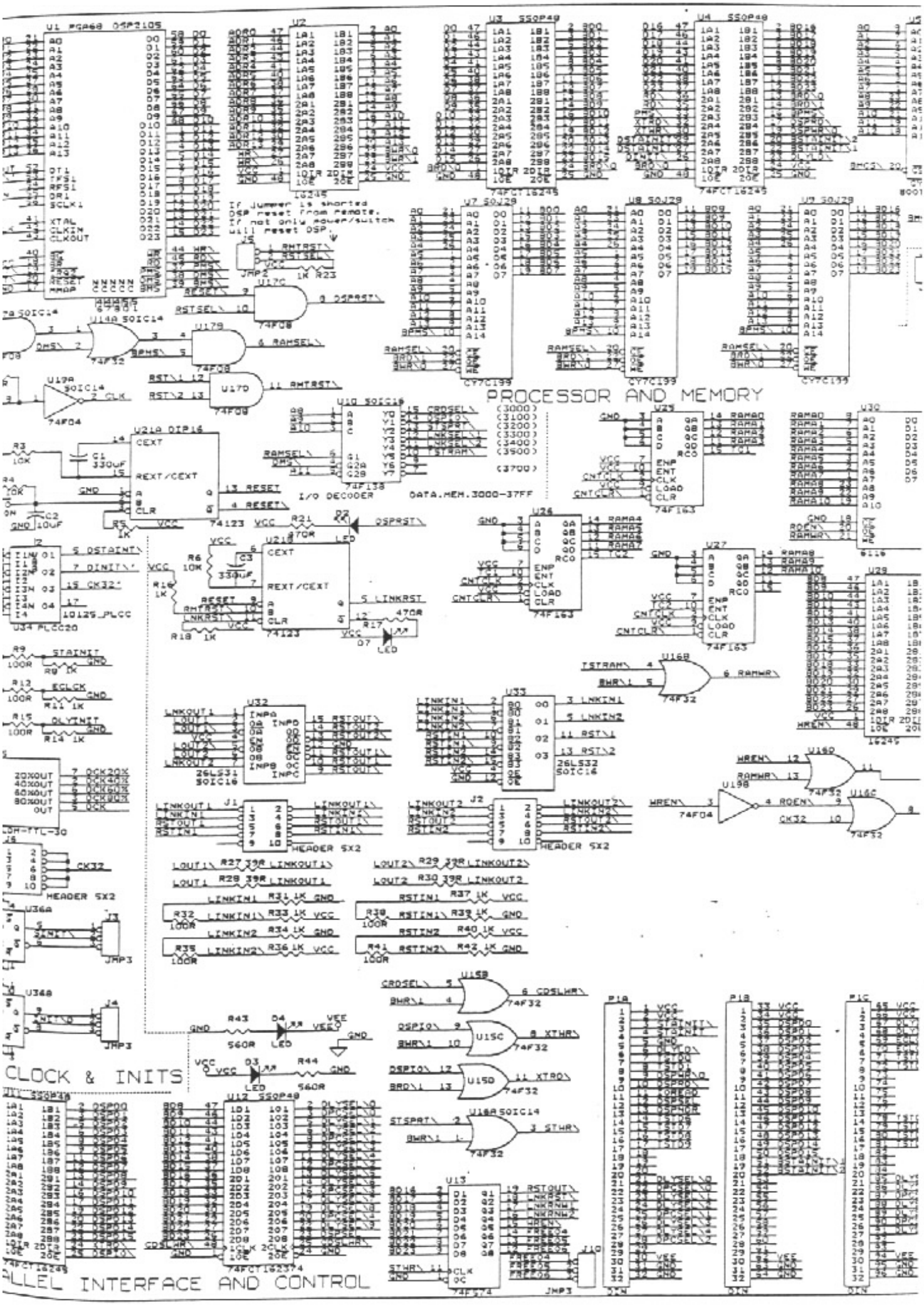
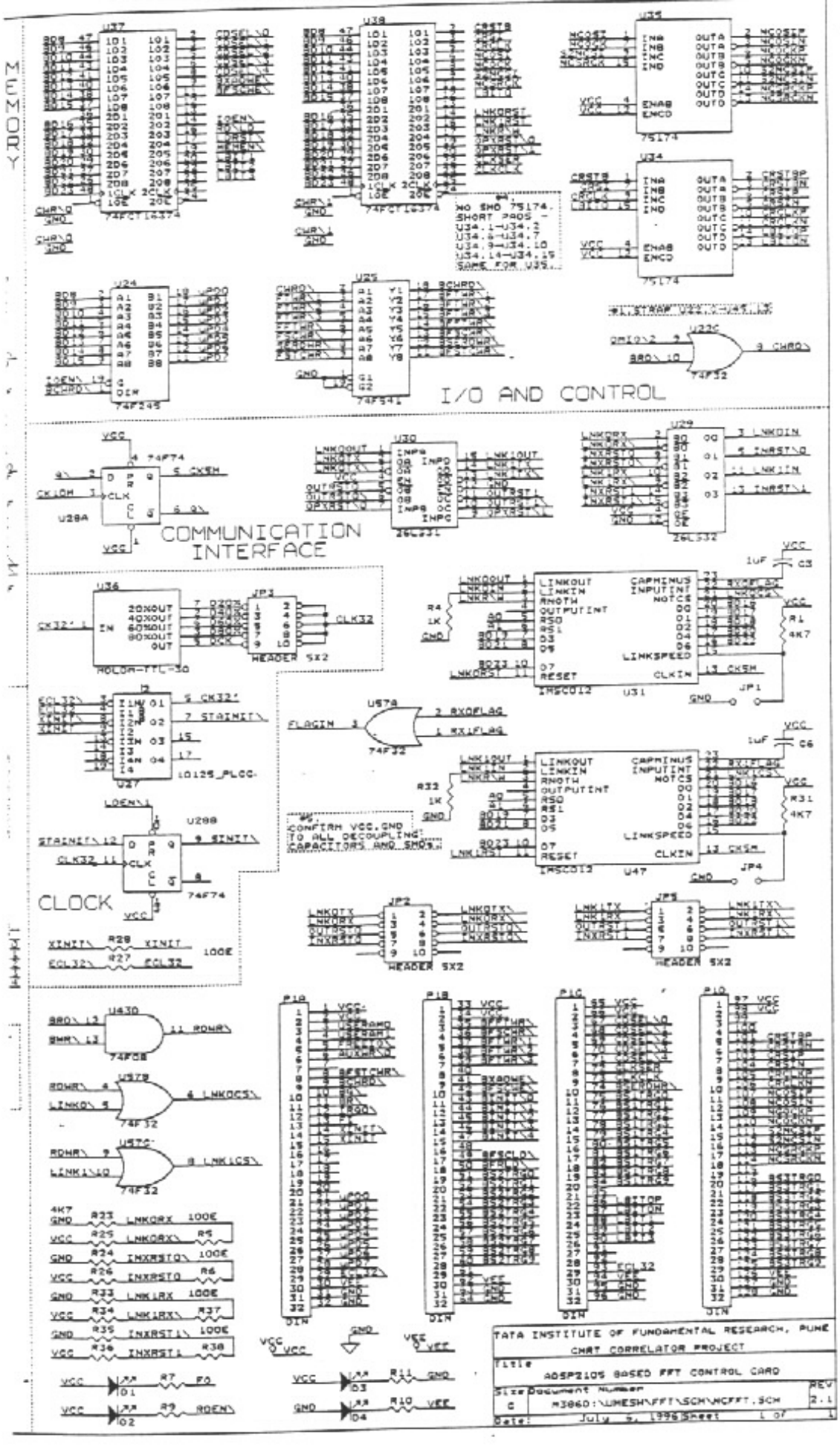
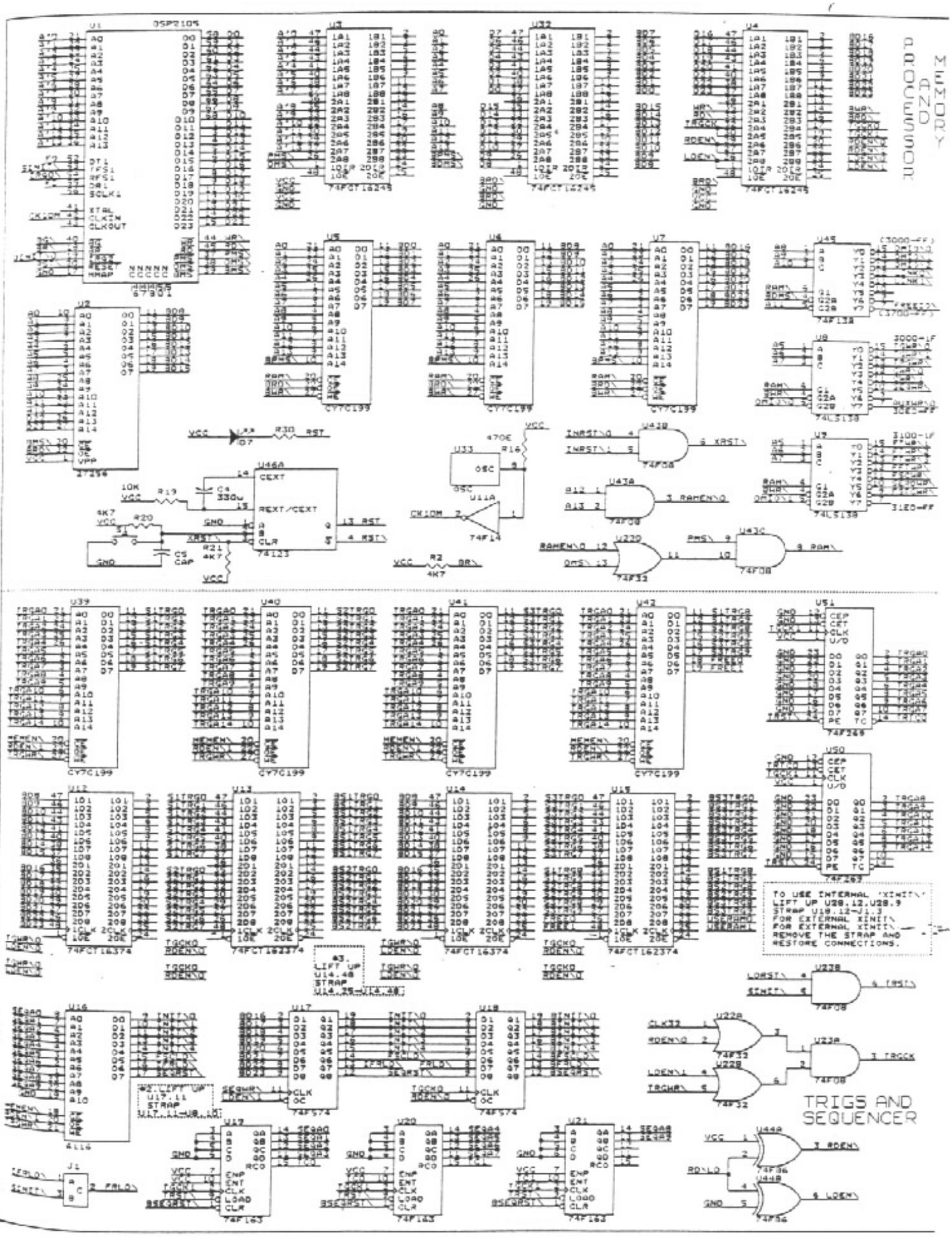
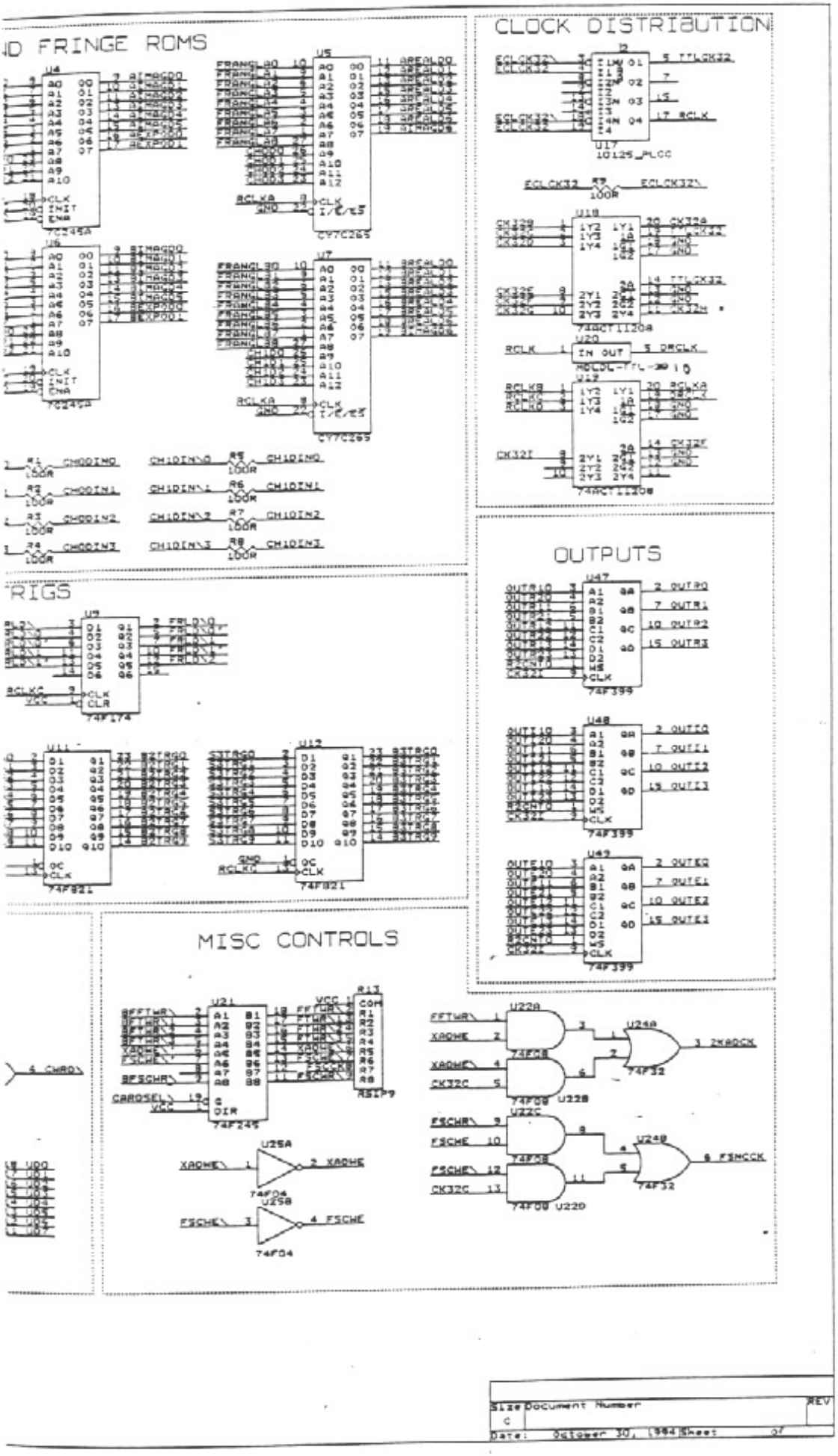
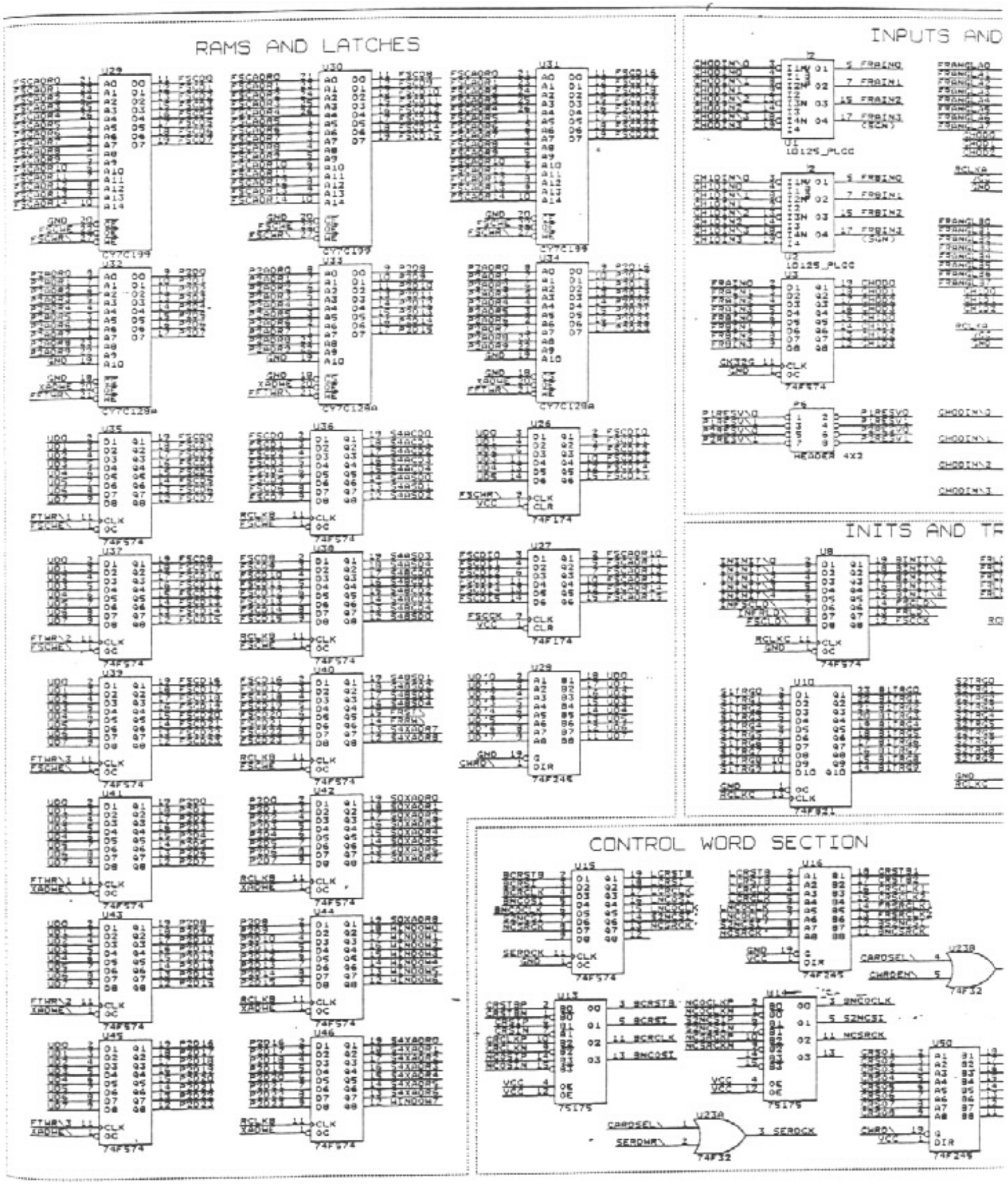
Size: C	Document Number: DLYCF.SCH	REV: 2
Date: July 29, 1997	Sheet 1 of 1

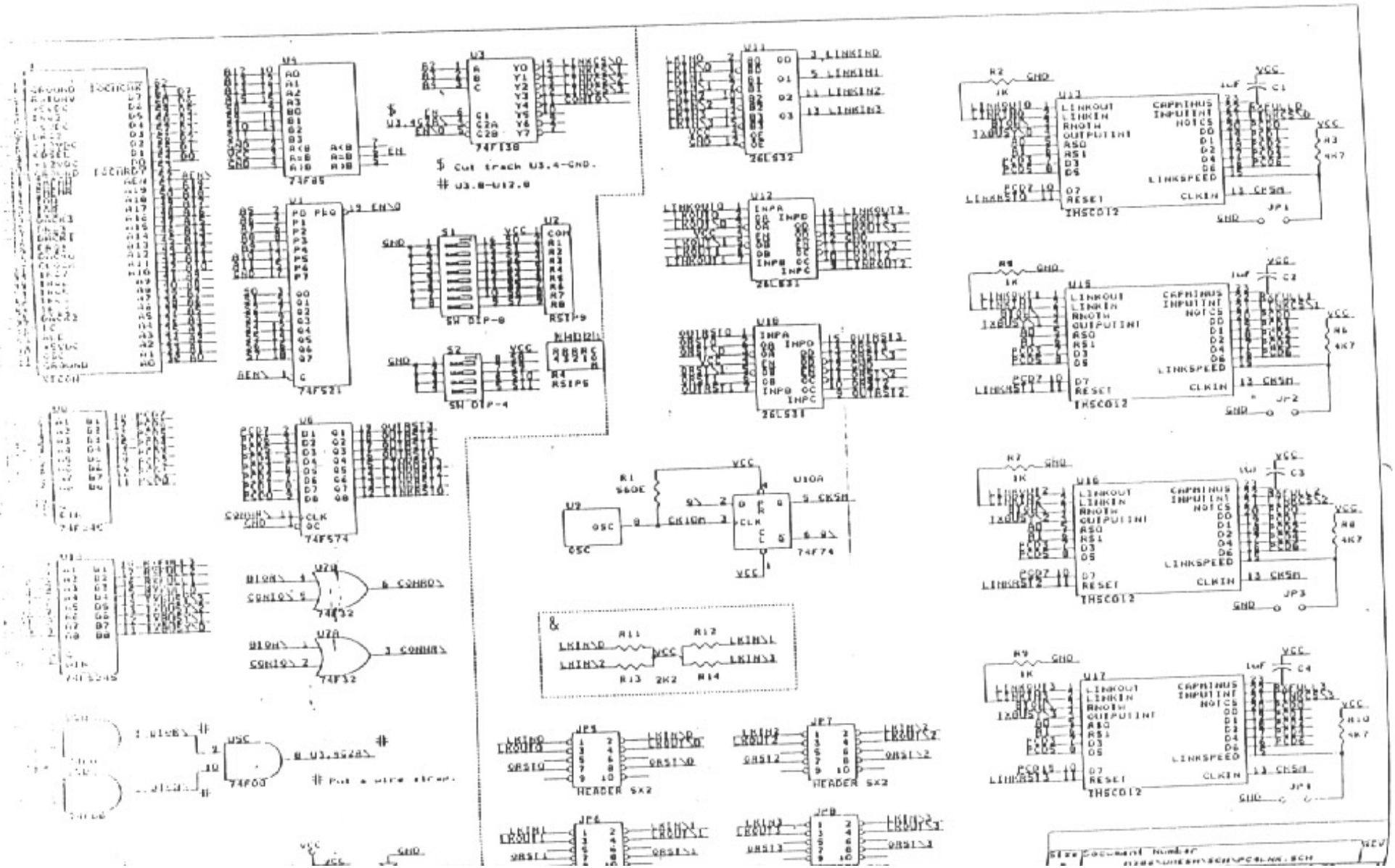

PROCESSOR AND MEMORY
CLOCK & INITS
PARALLEL INTERFACE AND CONTROL


I/O AND CONTROL
COMMUNICATION INTERFACE
CLOCK
TATA INSTITUTE OF FUNDAMENTAL RESEARCH, PUNE
CHAT CORRELATOR PROJECT
ADSP2105 BASED FFT CONTROL CARD


TRIGS AND SEQUENCER
TO USE INTERNAL 'XINIT\'
LIFT UP U28.12,U28.9
STRAP U18.12-U1.3
FOR EXTERNAL XINIT\
FOR EXTERNAL XINIT\
REMOVE THE STRAP AND
RESTORE CONNECTIONS.

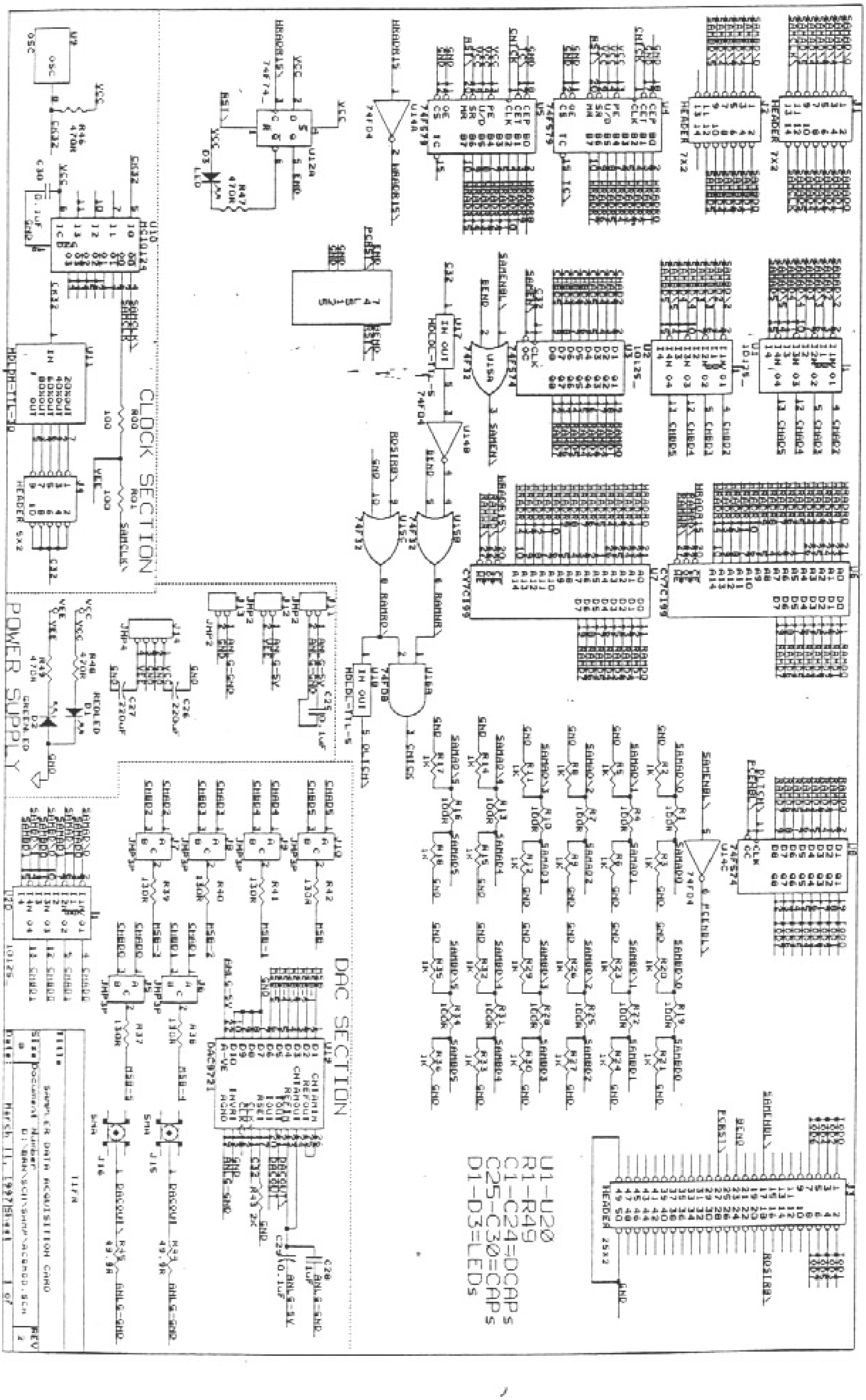

D FRINGE ROMS
CLOCK DISTRIBUTION
OUTPUTS
RIGS
MISC CONTROLS
Size Document Number REV
C
Date: October 30, 1994 Sheet of

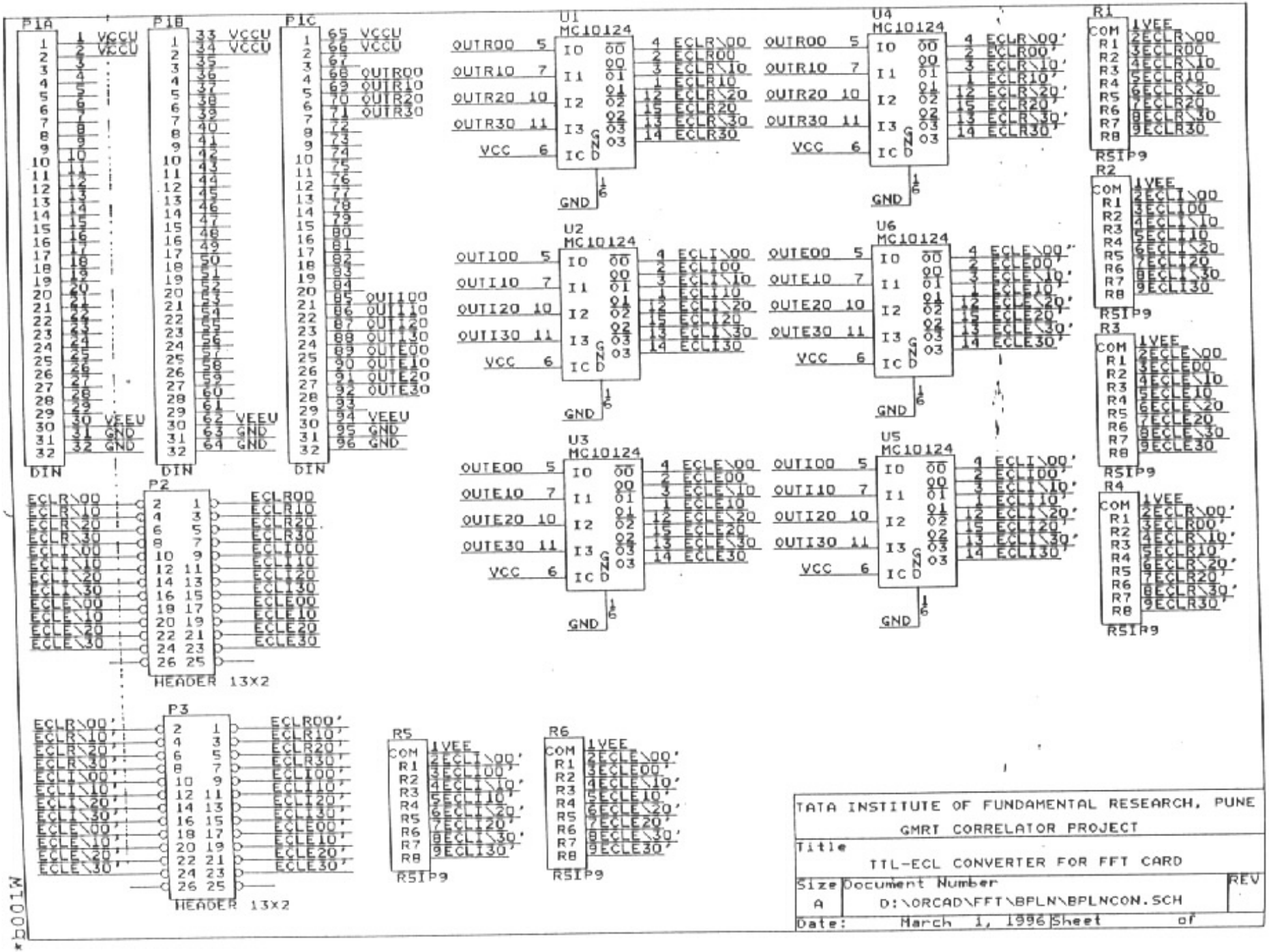

RAMS AND LATCHES
INPUTS AND
INITS AND TR
CONTROL WORD SECTION


74F138
74F85
74F521
74F574
74F32
74F00
74F74
SW DIP-8
SW DIP-4
RSIP9
RSIP8
26C32
26C31
THSC012
HEADER 5X2
$ Cut track U3.4-GND.
# U3.8-U12.8

program romRam

PARAMETER (LOG2N=10, n_mx=2**LOG2N, m2=9)




P1A
P1B
P1C
DIN
U1
U2
U3
U4
U5
U6
MC10124
OUTR00
OUTR10
OUTR20
OUTR30
OUTI00
OUTI10
OUTI20
OUTI30
OUTE00
OUTE10
OUTE20
OUTE30
VCC
GND
VEEU
P2
P3
HEADER 13X2
R1
R2
R3
R4
R5
R6
RSIP9
TATA INSTITUTE OF FUNDAMENTAL RESEARCH, PUNE
GMRT CORRELATOR PROJECT
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TTL-ECL CONVERTER FOR FFT CARD
Size
A
Document Number
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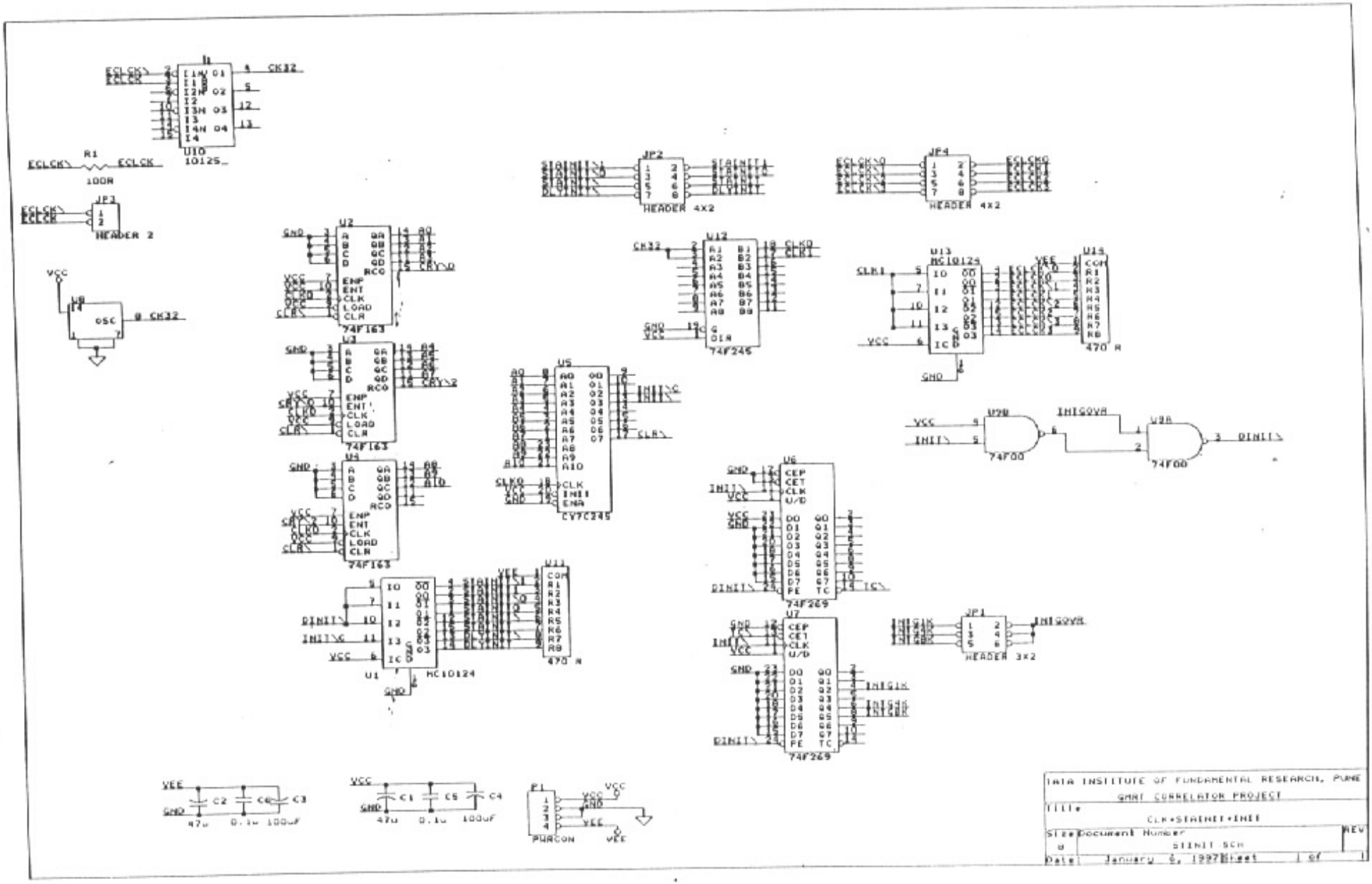
REV
Date: March 1, 1996
Sheet of



TATA INSTITUTE OF FUNDAMENTAL RESEARCH, PUNE		
GMRT CORRELATOR PROJECT		
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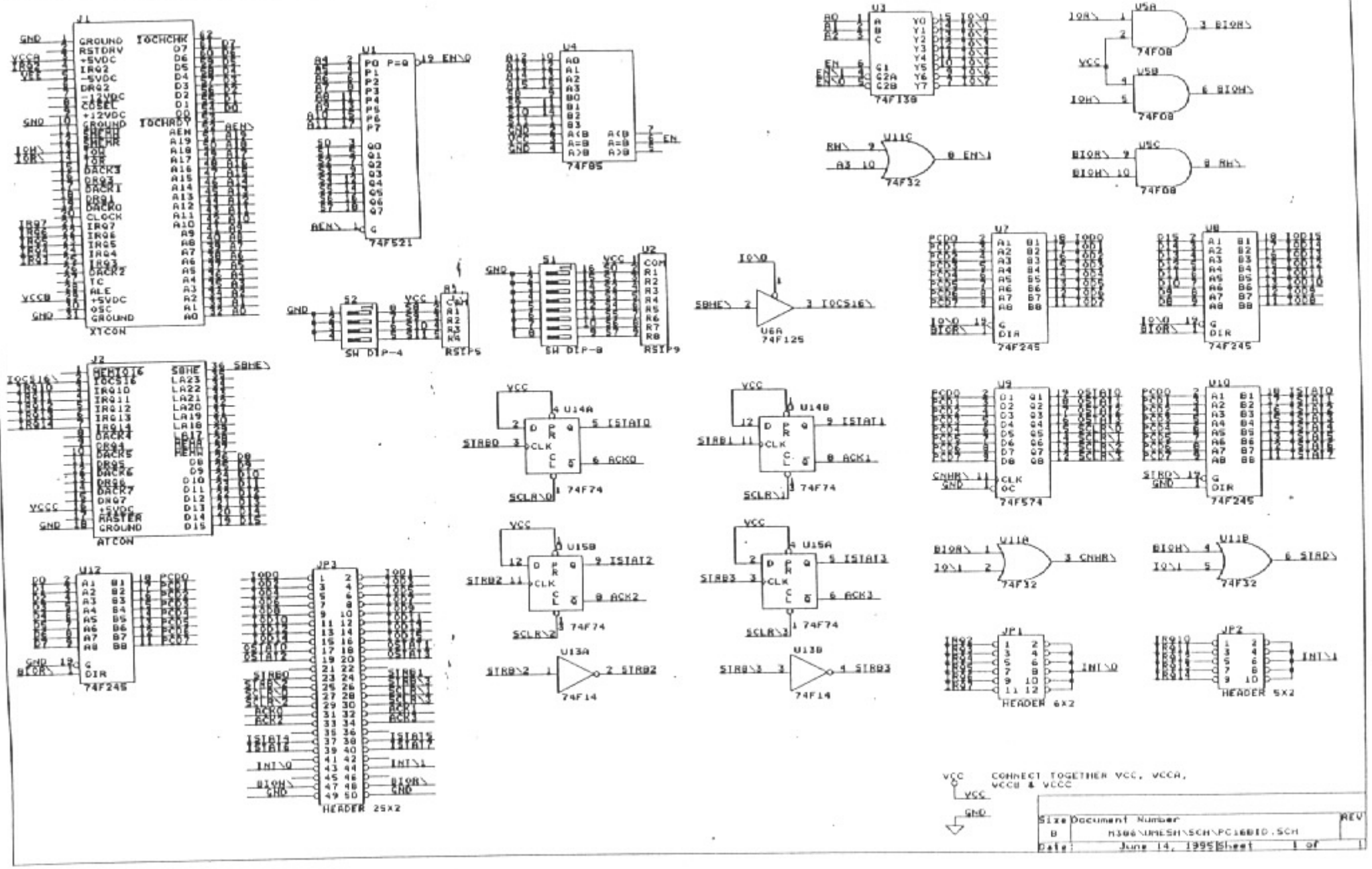
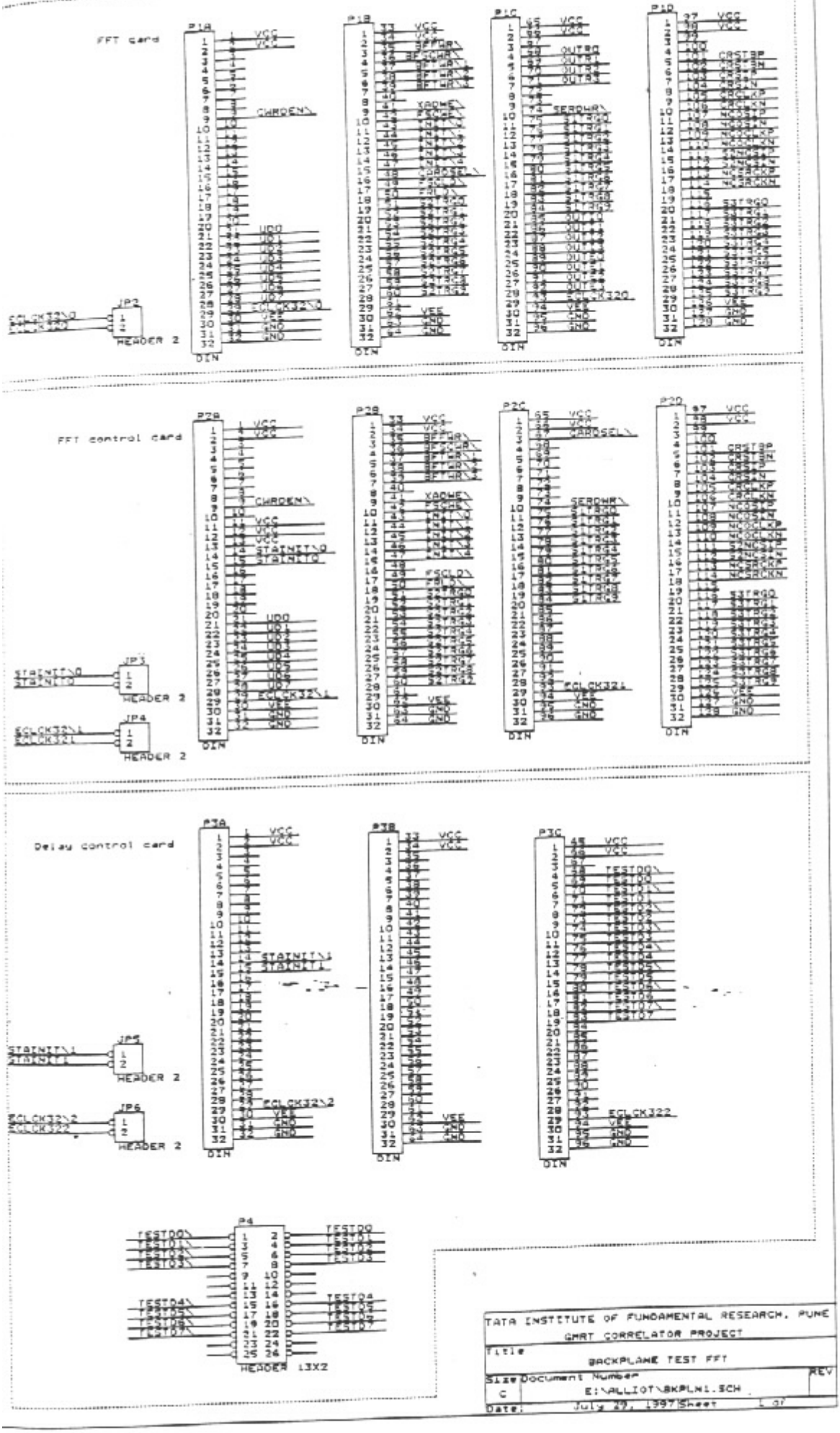
Size: B	Document Number: DINIT.SCH	REV:
Date: January 6, 1997	Sheet 1 of 1	


J1
XTCON
U1
74F521
U4
74F85
U3
74F138
U5A
74F08
U5B
74F08
U11C
74F32
U5C
74F08
S1
SW DIP-8
S2
SW DIP-4
U2
RSIP9
RSIP5
U6A
74F125
U7
74F245
U8
74F245
J2
ATCON
U14A
74F74
U14B
74F74
U15B
74F74
U15A
74F74
U13A
74F14
U13B
74F14
U9
74F574
U10
74F245
U12
74F245
JP3
HEADER 25X2
U11A
74F32
U11B
74F32
JP1
HEADER 6X2
JP2
HEADER 5X2
VCC CONNECT TOGETHER VCC, VCCA, VCCB & VCCC
Size B
Document Number M386\UMESH\SCH\PC16BID.SCH
REV
Date: June 14, 1995 Sheet 1 of 1



TATA INSTITUTE OF FUNDAMENTAL RESEARCH, PUNE		
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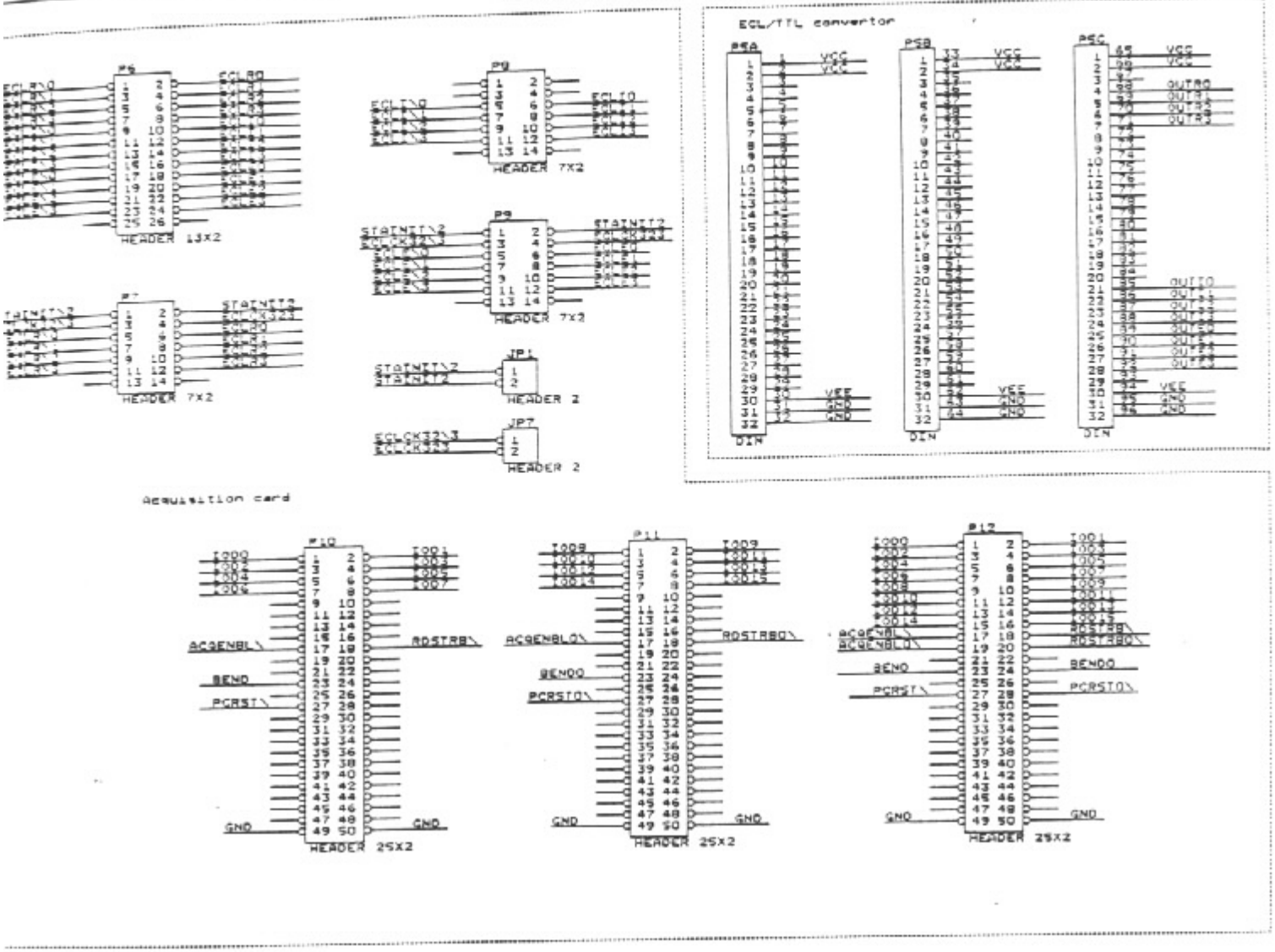
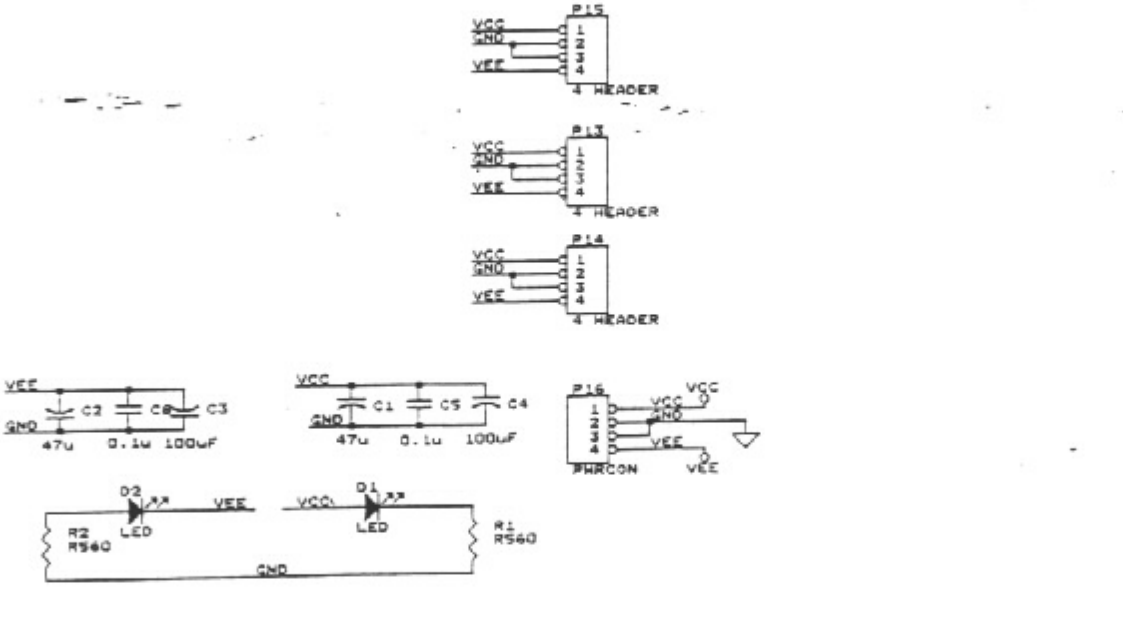
Date: July 29, 1997	Sheet	1 of


ECL/TTL convertor
P8
HEADER 13X2
P9
HEADER 7X2
P3
HEADER 7X2
P7
HEADER 7X2
JP1
HEADER 2
JP7
HEADER 2
P5A
P5B
P5C
DIN
Acquisition card
P10
HEADER 25X2
P11
HEADER 25X2
P12
HEADER 25X2
ACQENBL\
BEND
PCRST\
RDSTRB\
GND
BENDO
PCRSTO\
RDSTRBO\


P15
P13
P14
4 HEADER
VCC
GND
VEE
C2
C6
C3
47u
0.1u
100uF
C1
C5
C4
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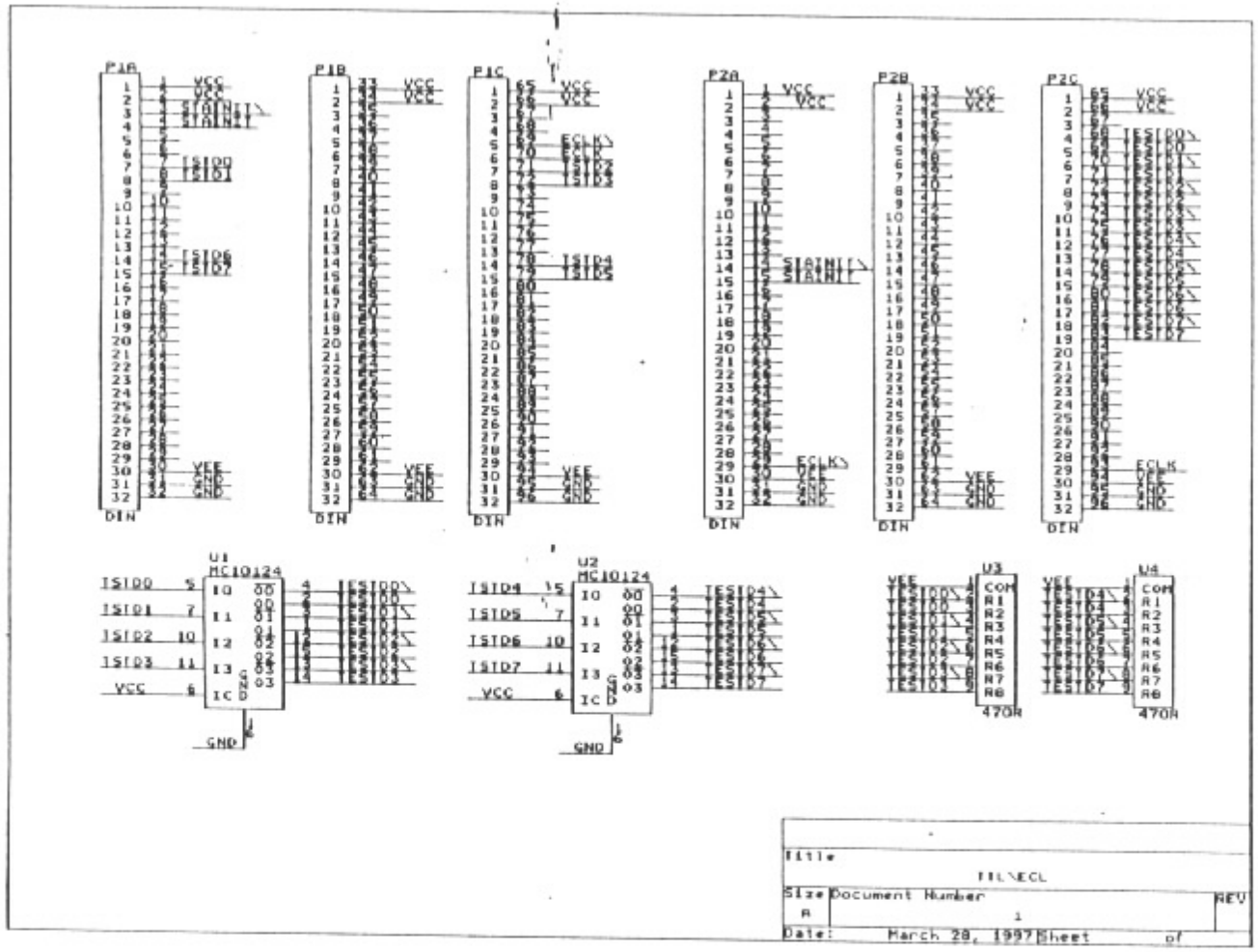
PWRCON
D2
D1
LED
R2
R560
R1
R560


P1A
P1B
P1C
P2A
P2B
P2C
DIN
VCC
VEE
GND
ECLK
U1
MC10124
U2
MC10124
U3
U4
470R
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ECL
Size
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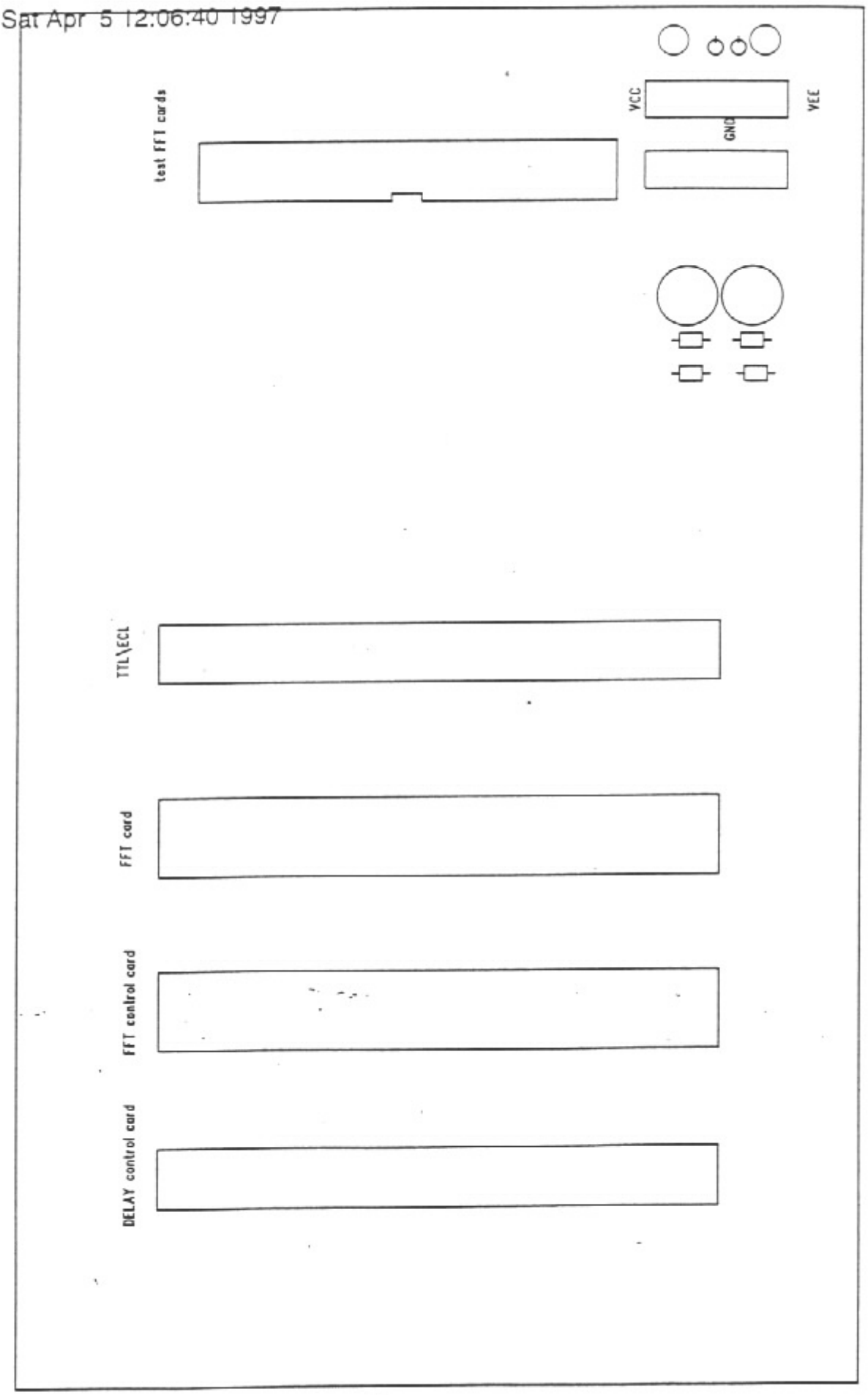
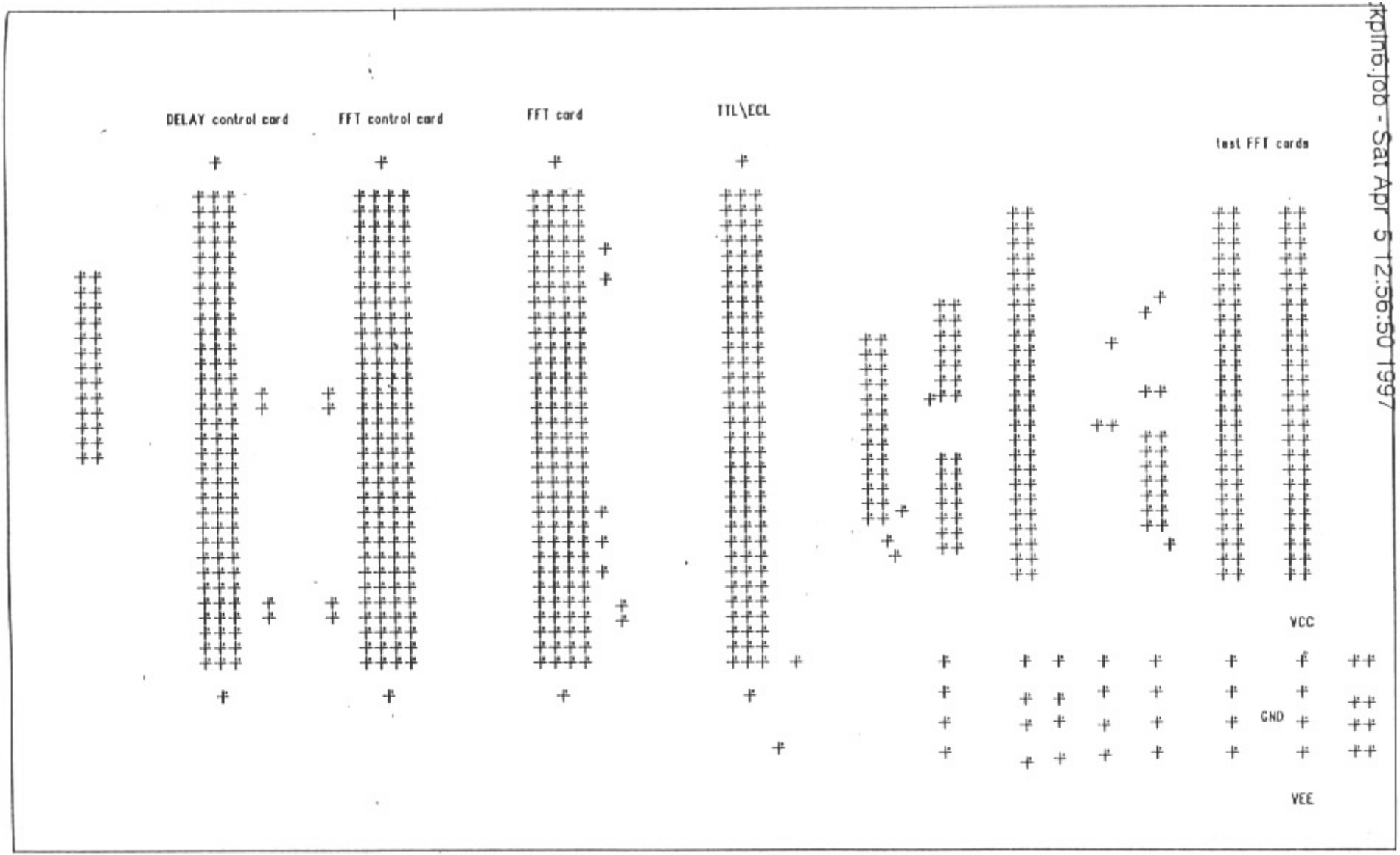
Document Number
1
REV
Date:
March 28, 1997
Sheet
of

bkpln6.job - Sat Apr 5 12:06:40 1997





SIZE	QTY	SYM
75	16	V
28	4	W
37	289	X
110	8	Y

BKPLN7.JOB - Mon Apr 7 17:47:57 1997