INTERNAL REPORT

DELAY DPC SYSTEM FOR THE MARK III CORRELATOR

(Prepared by Anish Roshi. D, Dt: 31-10-1996)

Preface

This report is prepared based on the work I have done on the DELAY:DPC system for the Mark III correlator from 1st August 1996 to 31st October 1996. The system was designed by Alka Dikshith and Abhijit Datta. My work was to debug the system and make it stable. In this report I have also included the informations received from Markandaylu about the system.

The schematics of the DPC and Delay circuit attached here should be taken as the closest approximation to the implemented circuit. This is because we have found that at least at two places in the DPCard the old schematic do not match with the implemented circuit. These schematics are also not completely free of ERC errors.

The Mark III correlator is an eight antenna, single side band, dual polarization correlator It requires 4 DPCards and 8 delay cards for compensating the delay suffered by the signal coming from different antennas due to geometric path difference. Since 5 DPCards and 10 delay cards form a "bin" we decided to integrated one such "bin". The 2 channels of each delay cards are used for the two polarization.

About DSTAINIT\ and DINIT\ control signals :

The system described here operates with a single clock of frequency 32 MHz. There are two important control signals for the entire correlator system for synchronizing various parts. They, as referred to the delay system, are (1) DSTAINIT\ with a peiord of 66.048 ms ($\equiv 4096 \times 516 \times$ 32 MHz clock period) and width 1 clk period; (2) DINIT\ with a period of 16.125 μs (516 $\times$ 32 MHz clock period) and width of 1 clk period. (**Note:** In the final system only the sampler, DPC and the write section of the delay card operates at 32 MHz and the rest of the system works at 32.25 MHz. The control signals are generated in the final system from 32.25 MHz and hence the periodicity of DSTAINIT\ and DINIT\ will be 64 ms and 16 μs respectively.) The labels representing these two control signals are used extensively in this report. For understanding the significance of other labels used here please refer to the schematics.

Present Status of the system :

Both channels of 9 delay cards are functioning. The test done by switching the delay between two values every DSTAINIT\ period, which is monitored for nearly 15 hours, is found to be stable. We have found that there are pick-ups in the data lines of the cards far (in position in the bin) from the control card when the test data is in logic state 0. A test conducted by connecting a dc motor to the same power supply to which the system is connected shows that there can be spurious interrupts generated in the control card DSP.

The following tests have been done on the DLYDPC systems :

(1) A test pattern is loaded into the 2048 location of the test data RAM (This RAM is in the delay control card.) such that a pattern of the form 1,2,4,f and zeros elsewhere appears at the output of the delay card (4 bits). The application program, dlyapp.dsp, is executed in the 2105 DSP. This software updates the read address counter in the delay card by incrementing by 258 (516/2) every DINIT\ intrrupt (ISR – DLYFFT.DSP). This ensures a continuous read out of the data from the DPRAM. At the DSTAINIT\ interrupt (ISR – DLYSTA.DSP) a new set of delay values is loaded. In this test delay values are toggled between zero delay and a gradient of 0 to 18 32 MHz clock period. The output of four delay cards has been monitored using Lecroy DSO in persistence mode. The delays are found to be togging between the expected values (monitored for nearly 15 hrs). However we found that there are pickups in some of the delay card outputs.

(2) The above test has been repeated with a square wave test pattern (1010, 0101, 1010, ...) of period 2 μs. This test pattern brings out the coupling between the bits. We found that the output pattern is toggling between the expected delay values (monitored for more than 15 hrs).

(3) While conducting test 1 & 2 we have changed the electrical environment like switching on tube lights, PC etc. to see their effect on the system. We haven't measure any change in the

output of the system within the trigger time of the oscilloscope.

The following tests should be done before shifting the system to Khodad :

Connect data (pattern with different rate of bit toggling) at the "normal" DPC input and check the pick-ups at the delay card output. This has to be done because the data passes through the ECL-to-TTL converters, which can produce high ground bounces.

Reliablity of delay loading (every $\sim$ 16 μs) from the DSP and how bad is the noise pick-up in the interrupt lines of DSP. The noise pick-up in interrupt lines can interrupt the DSP because the interrupts are edge sensitive. The clock dor DSP is generated from an independent source and therefore in the present system the interrupting cannot be made width sensitive.

Features supported by the present system :

(All the features are not been tested completely.)
The write address counter is cleared every DSTAINIT\ cycle. The 16 MHz clock (ADRINC & ODDCLK), used for incrementing the address counter and the latching the data, is also "phased" every DSTAINIT\ cycle (see timing diag 3).

The 16 MHz read clock (CNTLSB) used for loading the delay value is "phased" every DINIT\ cycle.

The design of the clearing of the write address counter every DSTAINIT\ cycle is such that it clears for lower frequency operation also (.i.e for 16, 8, 4 etc MHz, which is used when the bandwidth is less than 16 MHz). (*Tested only in one set of cards.*)

The power reading circuit in the DPCard 01 has been modified to get a stable reading. Right now power values from channel 0 is only available because of the shortage of free latches in the card. (*More tests have to be done.*)

The Walsh bits are wired to the back panel. Before connecting the walsh bits externally one should lift the latch IC pins, to which it is presently connected, from the base. (*Tested only in one set of cards.*)

The mode bit is also connected to the back panel. This can be used for masking the data by suitabling modify the 6to4 bit look-up EPROM. (*Tested only in one set of cards.*)

Synchronization of the system :

(Please refer to the timing diagram)

1. Adjust the phase of the SEQCLK to capture the DSTAINIT\ in the clock generation card.
2. Adjust the phase of 32 MHz clock to capture the DINIT\ in the delay control card.
3. Adjust the phase of the 32 MHz DPC clock to capture the test data in the DPCard.
4. Adjust the delay of DSTAINIT\ so that it is captured in the DPC card.
5. Adjust the 32 MHz delay "read" clock to capture the DINIT\ ($\equiv$ DLYLD\ ) in the delay card.
6. Adjust the 32 MHz sampler clock delay such that the data is captured at the input of the DPCard.

DSP software for delay loading :

There are three DSP routines used for delay loading — DLYAPP.DSP, DLYFFT.DSP, DLYSTA.DSP. The software requirements are (1) Update the read address offsets every DINIT\ period for all the 10 delay cards. (2) Load the new delay values every DSTAINIT\ period. For testing we have used a dual memory bank which are preseted with a set of delay values. The ISR, DLYSTA.DSP, switches between these two banks when the DSTAINIT\ interrupt occurs. The second ISR, DLYFFT.DSP, increments the offset value by 258 (258 because the read clk is 32 MHz and FFT requires 516 clocks) every DINIT\ interrupt. The dlyapp.dsp is the main routine which initializes the memory banks and waits for the interrupts.

The delay loading software should be modified, even for testing, such that the memory banks are initialized every DSTAINIT\ period, rather than just switching the banks. This is because, as described before, the interrupt lines are prone to noise pick-ups.

Interrupt priorities and timing of STAINIT\ & INIT\ for other parts of the correlator :

Presently the DINIT\ is connected to the highest priority interrupt (IRQ2) of the DSP. This means that after switching the memory bank in the DSTAINIT\ ISR the new delay values get loaded in the read counter only in the second DINIT\ from DSTAINIT\ signal (see timing diag). This should be taken into account in the generation of the control signal for other parts of the correlator.

Requirement on the control signals (DSTAINIT\ & DINIT\ ) when the write and read section of the DELAY:DPC system are operated at 32 & 32.25 MHz respectively :

In the final system the control signals, DSTAINIT\ & DINIT\ , are generated using the 32.25 MHz clock. But these signals are captures in the delay control card and DPCard with 32 MHz clock. This means that the two signals should be generated when the rising edges of the two clocks are synchronized with in a tolerable time. This should be taken into account in the design of the master control card of the final system.

Summary of the corrections made on the system

Changes made in the clock generation card :

The DSTAINIT\ (labeled as STINIT\ ), which is captured in the clock gen. card, is passed through a delay module and send to the delay control card (*astainit*). (U20 IC base has been used for introducing the delay module.) This is to adjust the propagation delay of the signal such that it is captured by the 32 MHz clock of the DPCard.

Changes made in the delay control card :

The capturing of the DSTAINIT\ in the delay control card have been bypassed. This is because it is captured in the DPCard by adjusting its propagation delay in the clock generation card.

The DSTAINIT\ is buffered using two buffers. The outputs of the buffers, BSTAINIT\ 1 & BSTAINIT\ 2 are connected to DPCards 1 & 2 and 3 to 5 respectively. This is take care of the transmission problem of the signal through the back panel.

The captured DINIT\ (≡ DLYLD\ ) is also buffered using two buffers. The outputs of the buffers, BDLYLD\ 1 & BDLYLD\ 2, are connected to Delay cards 1 to 6 and 6 to 10 respectively. The buffer used is 74F245 which is mounted on a piggy back on the back panel.

Changes made in the back panel :

In the original design a single ECL clock was going to a pair or delay cards. This has been removed and connected to different ECL clock sources in the clock generation card.

The DLYLD\ signals are routed through P1A pin 7 of delay back panel connectors.

Corrections in DPC card

Anish Roshi. D
Dt: 8-9-96

PCB tracks to be removed

Solder side

1. Cut the PCB track connection between U4 pin 5 to TP2.
2. Cut the PCB track coming to U8 pin 4 near that pin.
3. Cut the PCB track coming to U11 pin 2 near that pin.
4. Cut the PCB track coming to U17 pin 5 near that pin.
5. Cut the PCB track coming to U17 pin 12 near that pin.
6. Cut the PCB track coming to U17 pin 3 near that pin.
7. Remove th connection between U17 pin 12 to U19 pin 3.

Component side

1. Cut the PCB track coming to U4 pin 1 (**careful**).

2. Cut the PCB track coming to U4 pin 5 (**careful**).

Interconnections to be made

1. U18 pin 5 to TP2.
2. U8 pin 4 to U4 pin 5.
3. U11 pin 2 to U18 pin 11.
4. TP16 to GND (**careful**; C20 GND pin can be used).
5. U18 pin 10 to U4 pin 1.
6. U9 pin 18 to U3 pin 18.
7. U22 pin 8 to U22 pin 10.
8. U13 pin 2 to P1B21
9. U13 pin 5 to P1B25
10. U13 pin 7 to P1B26
11. U13 pin 10 to P1B27
12. U7 pin 14 to P1A6
13. P1A 5, P1B 20, 22, 28 to GND.

Corrections in Delay Card

Anish Roshi. D
Dt: 8-9-96

PCB tracks to be removed

Solder side:

1. Remove the **wire** connected between U22 pin 1 and U22 pin 5.
2. Cut the PCB track connected to P1B pin 29 (euro conn.) near the connector pin.
3. Remove the PCB track between U2 pin2 & U2 pin 6.
4. Cut the PCB track connected between U3 pin 11 and U10 pin 7 **at both ends.**
5. Cut the PCB track connection between U20 pin 12 and U24 pin 11 **at both ends.**
6. Cut the PCB track connection coming to U21 pin 1 near that pin.
7. Remove the PCB track connection between U14 pin 2 and U14 pin 6.

8. Cut the PCB track coming to U10 pin 2 near that pin.
9. Cut the PCB track connection between U2 pin 8 and U2 pin 12.
10. Cut the PCB track connection coming to U10 pin 4 near that pin.
11. Cut the PCB track coming to P1B pin 23 (euro conn.).
12. Cut the PCB track coming (**from the via**) to U10 pin 5 near that pin.
13. Cut the PCB track coming to U22 pin 5 near that pin.
14. Cut the PCB track coming to U16 pin 13 near that pin.

Component side :

1. Cut the PCB track connection between P1A pin 19 and TP2. **Cut it between the connector pin and TP2.**
2. Cut the PCB track connection to TP15 near that test point. (TP15 is between U15 & U14.)
3. Cut the PCB track **going** between U16 pin 3 & 4 near U16.
4. Cut the PCB track connection to U16 pin 5 near U16.
5. Cut the PCB track connection to U16 pin 6 near U16.
6. Cut the PCB track connection to U24 pin 11 near U24.
7. Cut the PCB track connected to U16 pin 4 (**inside IC base U16**).
8. Cut the PCB track coming to U16 pin 3.
9. Cut the PCB track coming to U2 pin 11 (**inside IC base U2**).
10. Cut the PCB track coming to zip U9 (R8; connection going to U10 pin 11) from U2 pin 11.
11. Cut the PCB track coming to U2 pin 9.
12. Cut the PCB track coming to U16 pin 3 (**inside IC base U16**; coming from U10 pin 5).
13. Cut the PCB track coming to U22 pin 5 near that pin.
14. Cut the PCB track coming to U23 pin 1 (going to the via near the **LABEL** U23).
15. Cut the PCB track coming to via TP18.
16. Cut the PCB track connection between U2 pin 6 & U6 pin 11.
17. Cut the PCB track coming to P1B 6 and connect it to P1B 7.

Lift the following IC pins from the base

1. U14 pin 9 & pin 12
2. U10 pin 14

Check whether IC in the base U17 is 74F163.

Interconnections to be made

1. Connect the **track removed from P1B pin 29** to P1A pin 1
2. U10 pin 9 to TP2.
3. U2 pin 6 to U10 pin 7 to U5 pin 2.
4. U5 pin 4 to U16 pin 6.
5. U5 pin 5 to U14 pin 6 to U10 pin 2.
6. U5 pin 6 to U14 pin 2.
7. U14 pin 9 to U14 pin 12.
8. Connect 0.1 mfd between U10 pin 10 and U10 pin 14.
9. U10 pin 17 to U16 pin 5.
10. U10 pin 18 to U23 pin 1.
11. U16 pin 10 to U24 pin 11.
12. U16 pin 11 to U20 pin 12.
13. U21 pin 1 to U21 pin 11.
14. U11 pin 1 to P1B pin 23.
15. U11 pin 13 to U11 pin 3.
16. U2 pin 12 to U11 pin 11 to U16 pin 3.
17. U2 pin 11 to U2 pin 3.
18. U16 pin 4 to U5 pin 1.
19. U2 pin 2 to U5 pin 3.
20. U22 pin 3 to U5 pin 11.
21. U10 pin 4 to U22 pin 5.
22. U11 pin 4 to U11 pin 7.

23. U16 pin 13 to U22 pin 7.

24. U2 pin 9 to U5 pin 12.

25. U4 pin 15 to U5 pin 13.

26. TP18 to U22 pin 1.

27. U15 pin2 to U18 pin 1.

28. U10 pin 13 to U6 pin 11.

29. P1B 8 to GND.

TEST POINTS IN DPC CARD

MAKANDEYULU, G. ANISH ROSHI, D. CHARUDATTA, K.

Updated on : 14-9-96

CHECK THE WAVEFORMS AT FOLLOWING POINTS

1) U29, U38 PINS 4,5,12,13 —— CLK 32 MHz.
2) U8 PIN 6 —— CLK 32, 16, 8, 4, 2, 1, 0.5, 0.25 for control wds 3040,3041,3042,3043,3044, 3045,3046,3047 respectively.
3) U41,35,33,34,30,39 PIN 9 —— CLK 32 MHz.
4) U16, 21, 26, 27 PIN 18 (piggy back) —— CLK 32 MHz.
5) U11, U14 PIN 2 — CLK 32 MHz.
6) U17 PIN 12 — BSTAINIT\ 32 ns pulse.
7) U17 PIN 9 —— CAPRST\ 32 ns pulse.
8) U24 PIN 2 — BSTAINIT\ 32 ns pulse.
9) U24 PIN 5 —— DLYRST\ 32 ns pulse.

TEST POINTS IN DELAY CARD

CHECK THE WAVEFORMS AT FOLLOWING POINTS

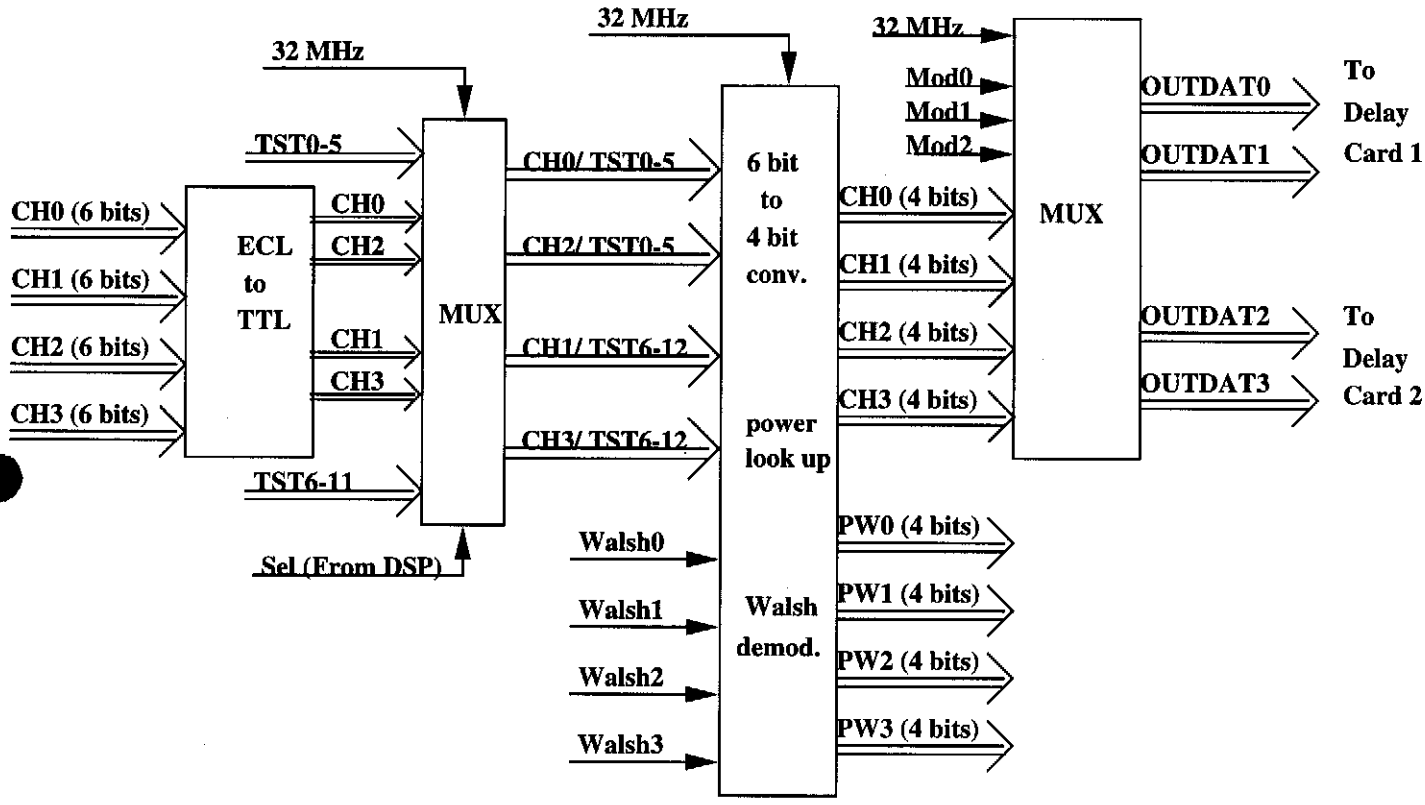
A) WRITE SECTION

1) U2 PIN 3 & 11 —— DPCCLK\ 32 MHZ.(IF Control wd is 3040)
2) U11 PIN 1 —— DLYRST\ (STAINIT) 30ns WIDE
3) U17 PIN 1 —— BRST\
4) U17 PIN 2 —— ADRINC 16 MHZ (IF Control wd is 3040)
5) U3 PIN 11 —— ODDCLK
6) U7 PIN 11 —— ADRINC
7) U19 PIN 6 —— WADRD0
8) U15 PIN 6 —— WADRD0
9) U19 PIN 2 —— ADRINC
10) U15 PIN 2 —— ADRINC
11) U18 PIN 1 —— ADRINC
12) U18 PIN 19 —— BRST\
13) U18 PIN 20 —— VCC

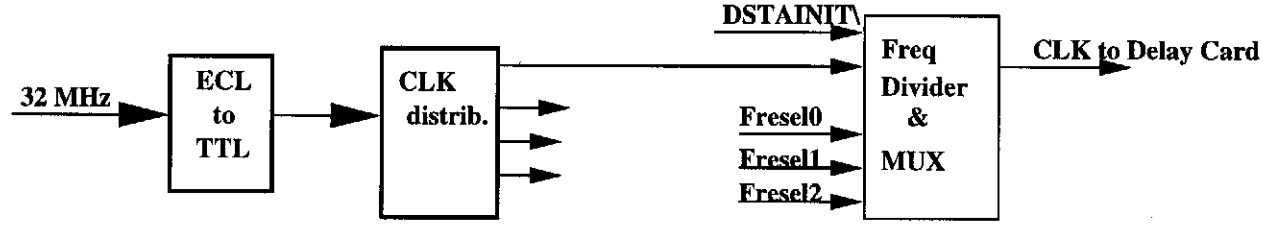
B) READ SECTION

1) U20 PIN 12 & 13 —— 32 MHz CLK
2) U10 PIN 17 —— BDLYLD\ (DINIT\ ) 32 ns WIDE
3) U8 PIN 11 —— CNTLSB
4) U8 PIN 24 —— BDLYLD\ (DINIT\ )
5) U19 PIN 42 —— RDADDO
6) U15 PIN 42 —— RDADDO
7) U13 PIN 2 —— CNTLSB
8) U13 PIN 9 —— BDLYLD\ (DINIT\ )
9) U21 PIN 1 —— BCNTLSB (16 MHz CLK)
10) U21 PIN 11 —— BCNTLSB (16 MHz)
11) U23 PIN 11 —— BCNTLSB (16 MHz)
12) U23 PIN 1 —— BCNTLSB\ (16 MHz CLK)
13) U25 PIN 11 —— 32 MHz CLK
14) U28 PIN 9 —— TFCLK2 (32 MHz)
15) U27 PIN 9 —— TFCLK2 (32 MHz)

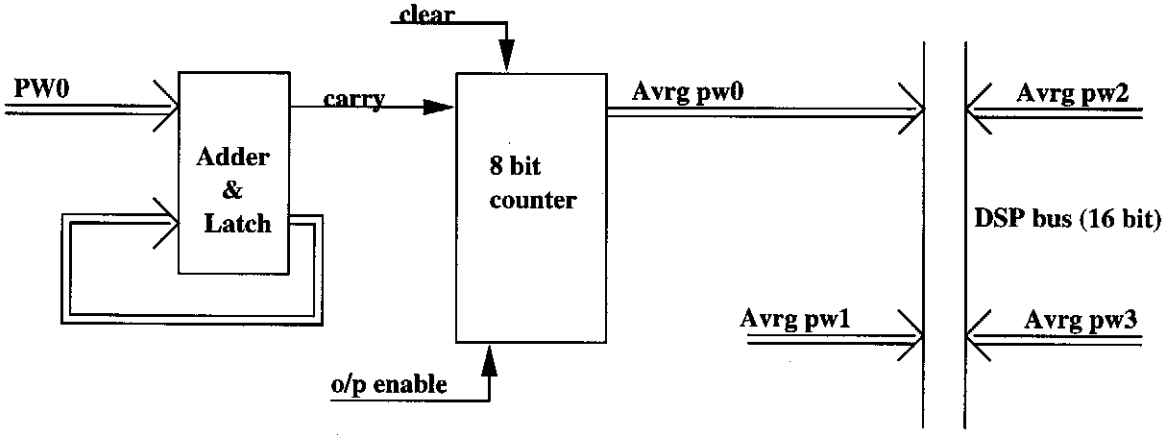
DPC CARD: BLOCK DIAGRAM



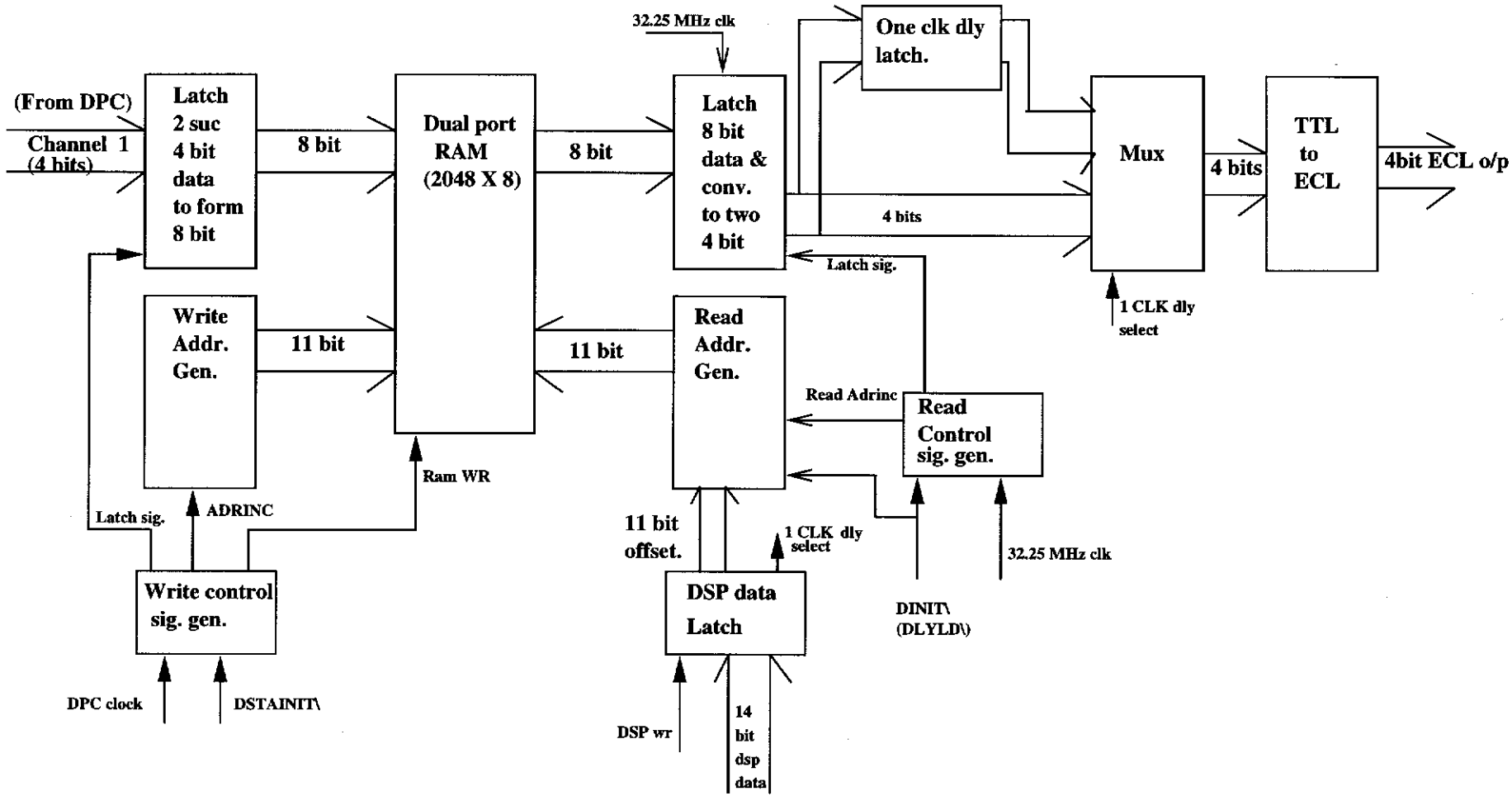
Clock to Delay Card

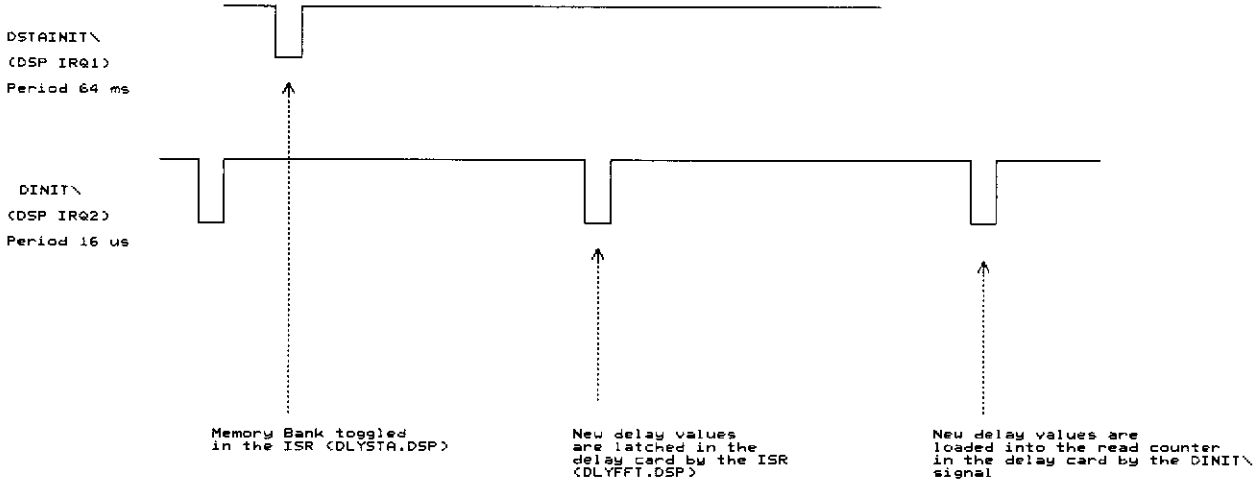


Power



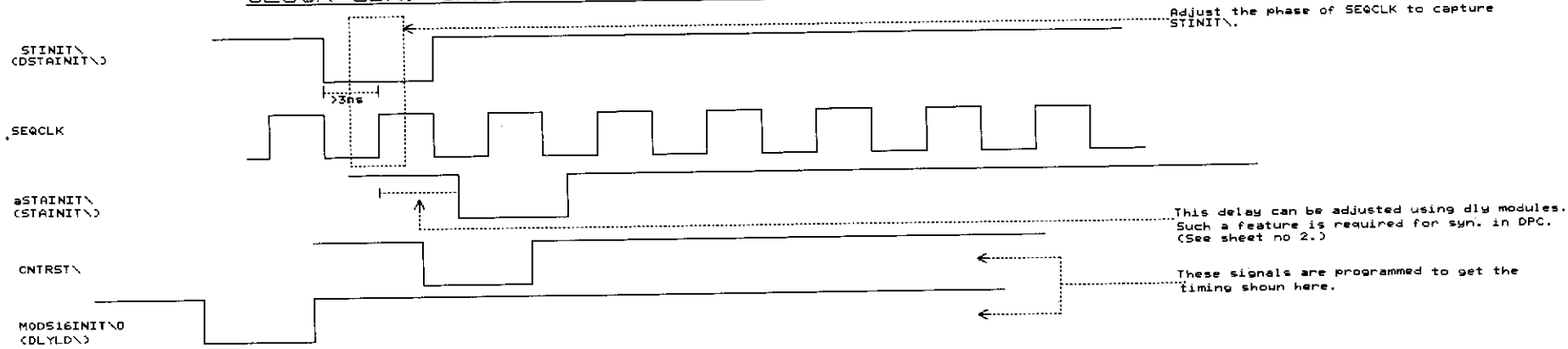
DELAY CARD: BLOCK DIAGRAM



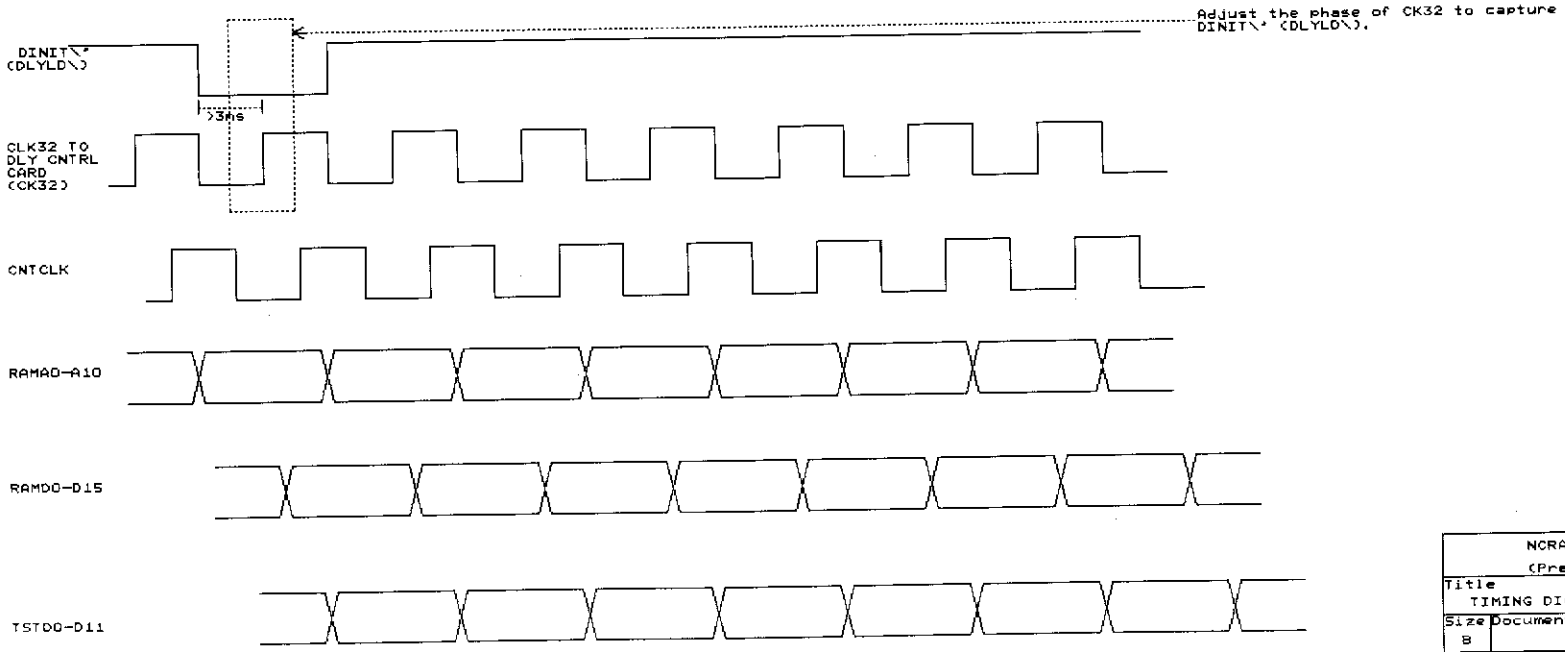


NCRA-TIFR		
(Prepared by Anish Roshi. D)		
Title: Delay loading		
Size: B	Document Number: DLYDPC0.TIM	REV:
Date: November 1, 1996	Sheet 1 of 1	

CLOCK GEN. CARD: TIMING DIAGRAM.

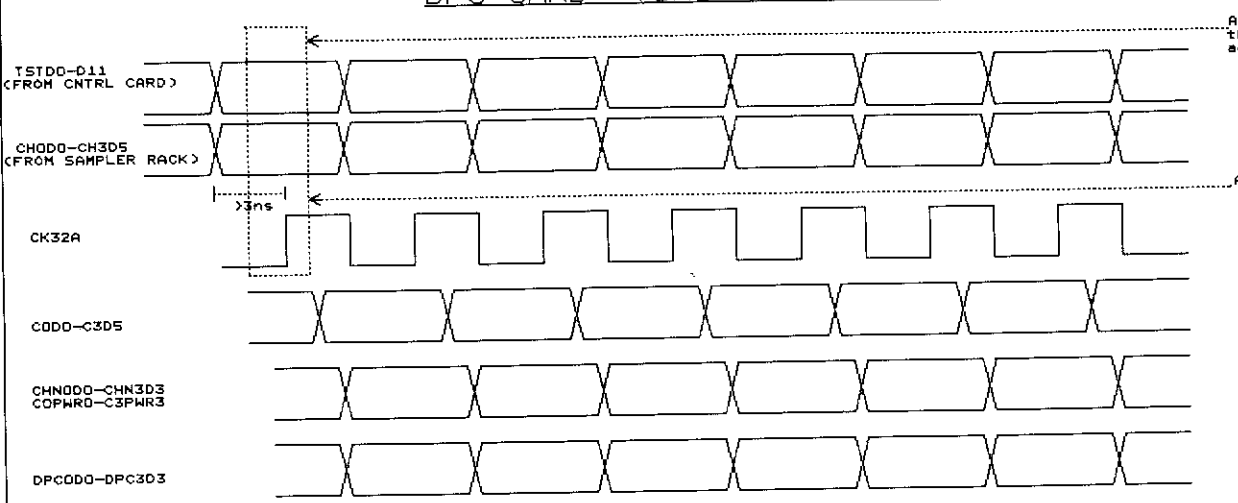


DLY CNTRL CARD: TIMING DIAGRAM.

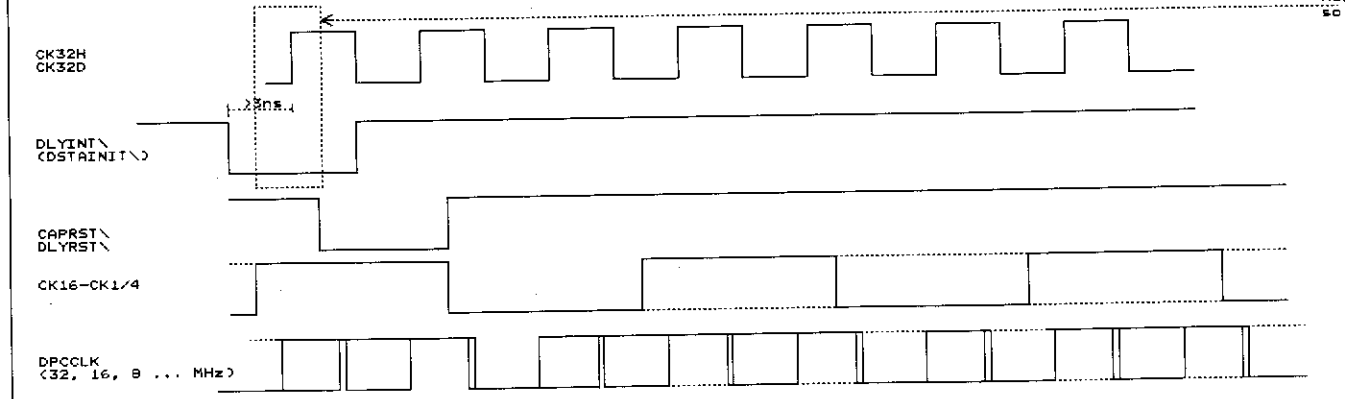


NCRA-TIFR, PUNE (Prepared by Anish Roshi. D)		
Title: TIMING DIG. CLOCK GEN. & DLY CNTRL CARD		
Size: B	Document Number: DLYDPC1.TIM	REV
Date: October 31, 1996	Sheet 1 of 4	

DPC CARD: TIMING DIAG. OF DATA FLOW

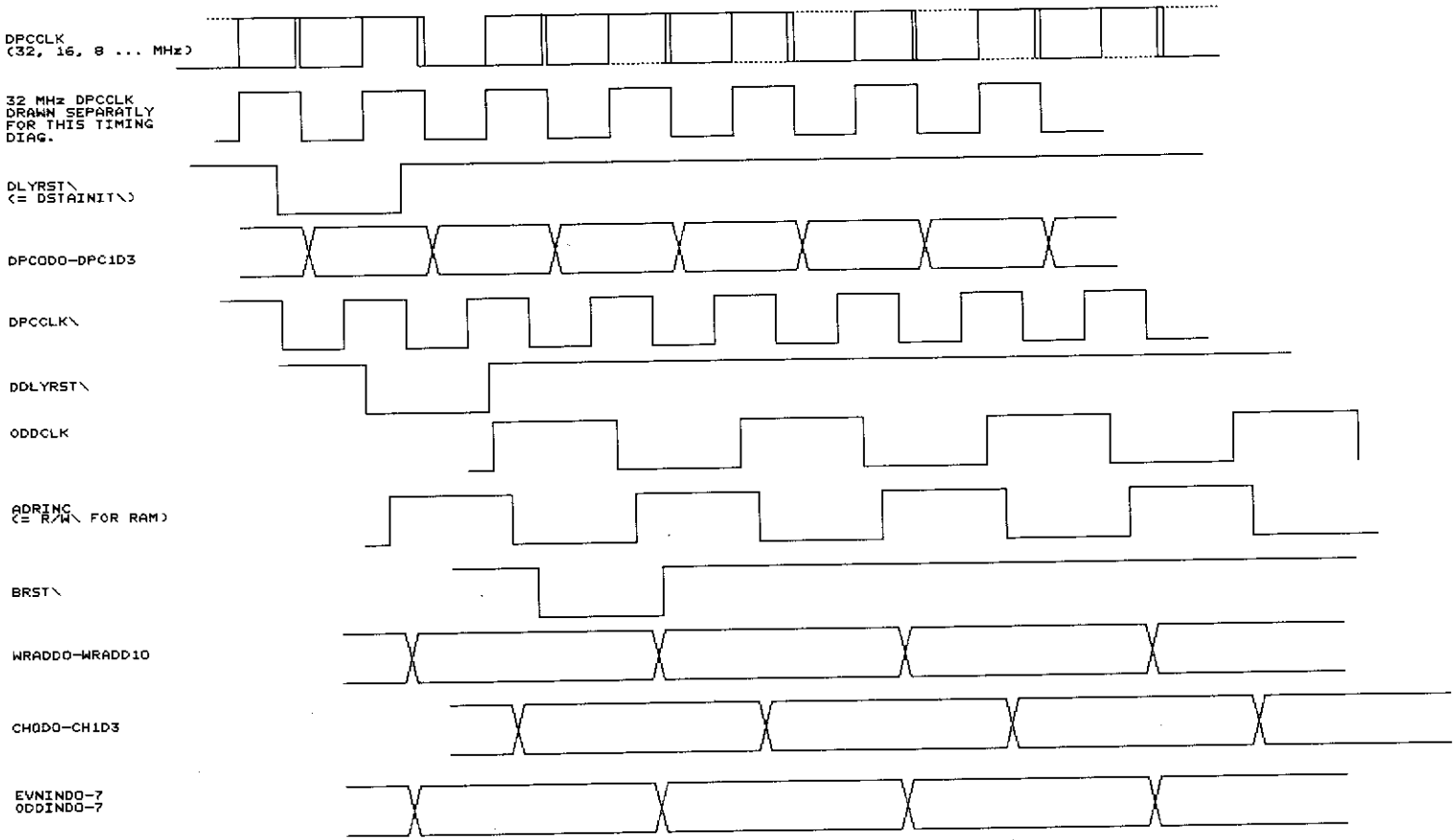


DPC CARD: ADRR CLOCK GEN.

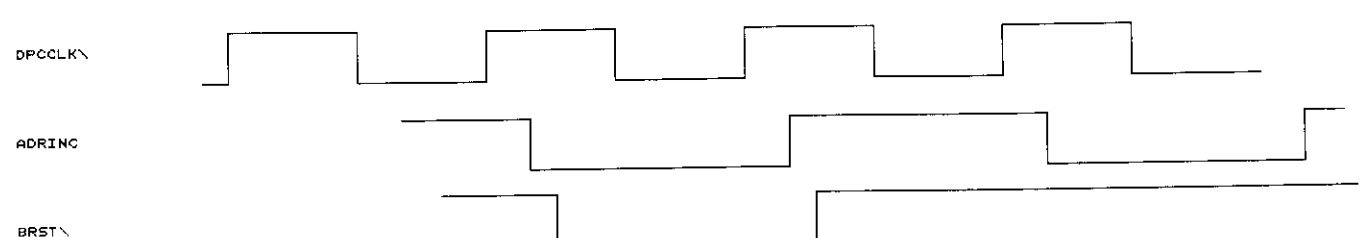


NCRA-TIFR, PUNE	
(Prepared by Anish Roshi, D)	
Title: DPC: DATA FLOW TIMING & ADRCLK GEN.	
Size: B	Document Number: DLYDPC2.TIM — REV:
Date: October 31, 1996	Sheet 2 of 4

DELAY WRITE SECTION TIMING DIAGRAM

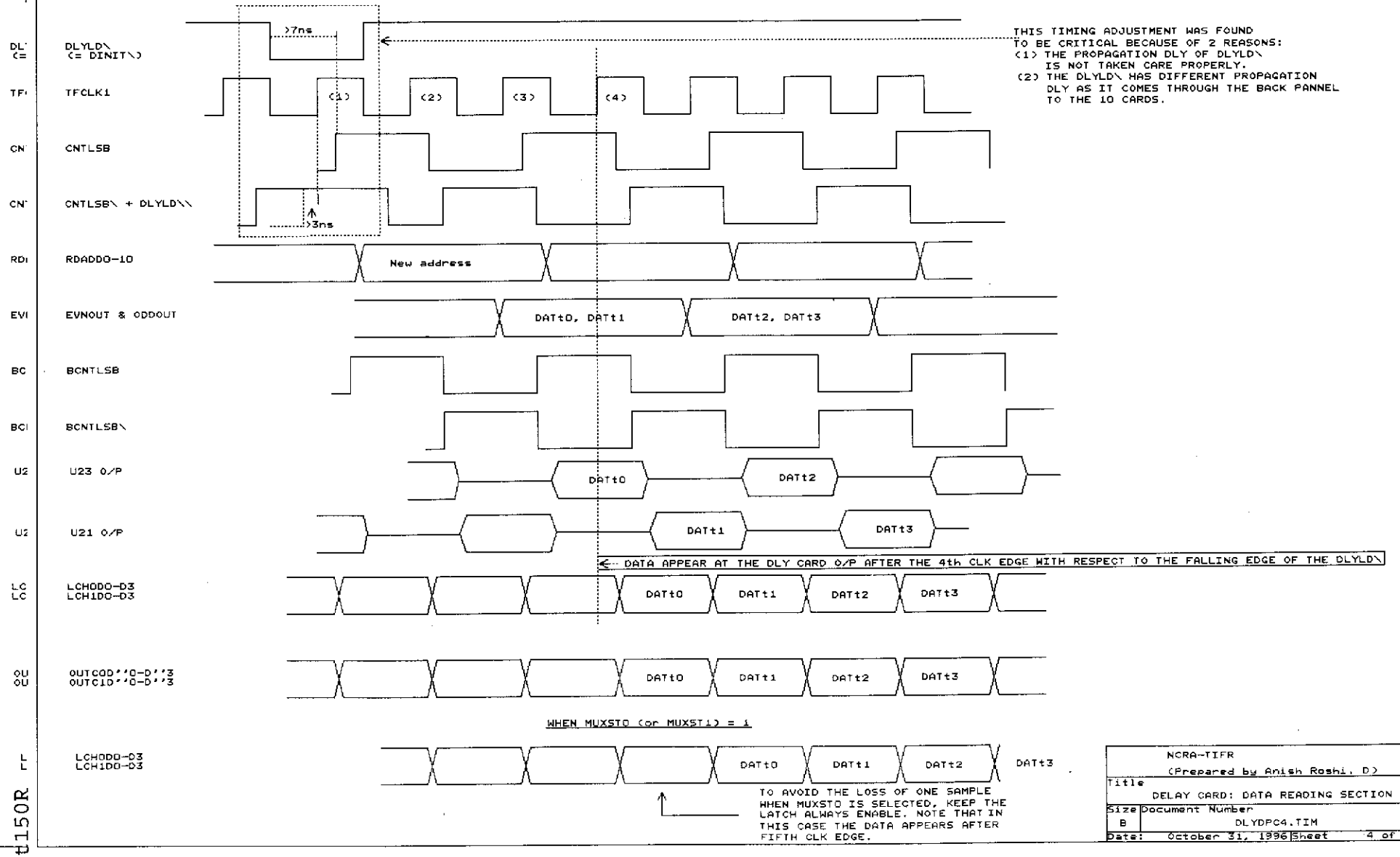


TIMING DIAG. FOR DPCCLK\ = 16 MHz (Notice BRST\)



NCRA-TIFR (PUNE)	
(Prepared by Anish Roshi. D)	
Title: DELAY WRITE SECTION TIM DIAG.	
Size: B	Document Number: DLYDPC3.TIM
Date: October 31, 1996	Sheet 3 of

DELAY CARD DATA READING SECTION



NCRA-TIFR	
(Prepared by Anish Roshi, D)	
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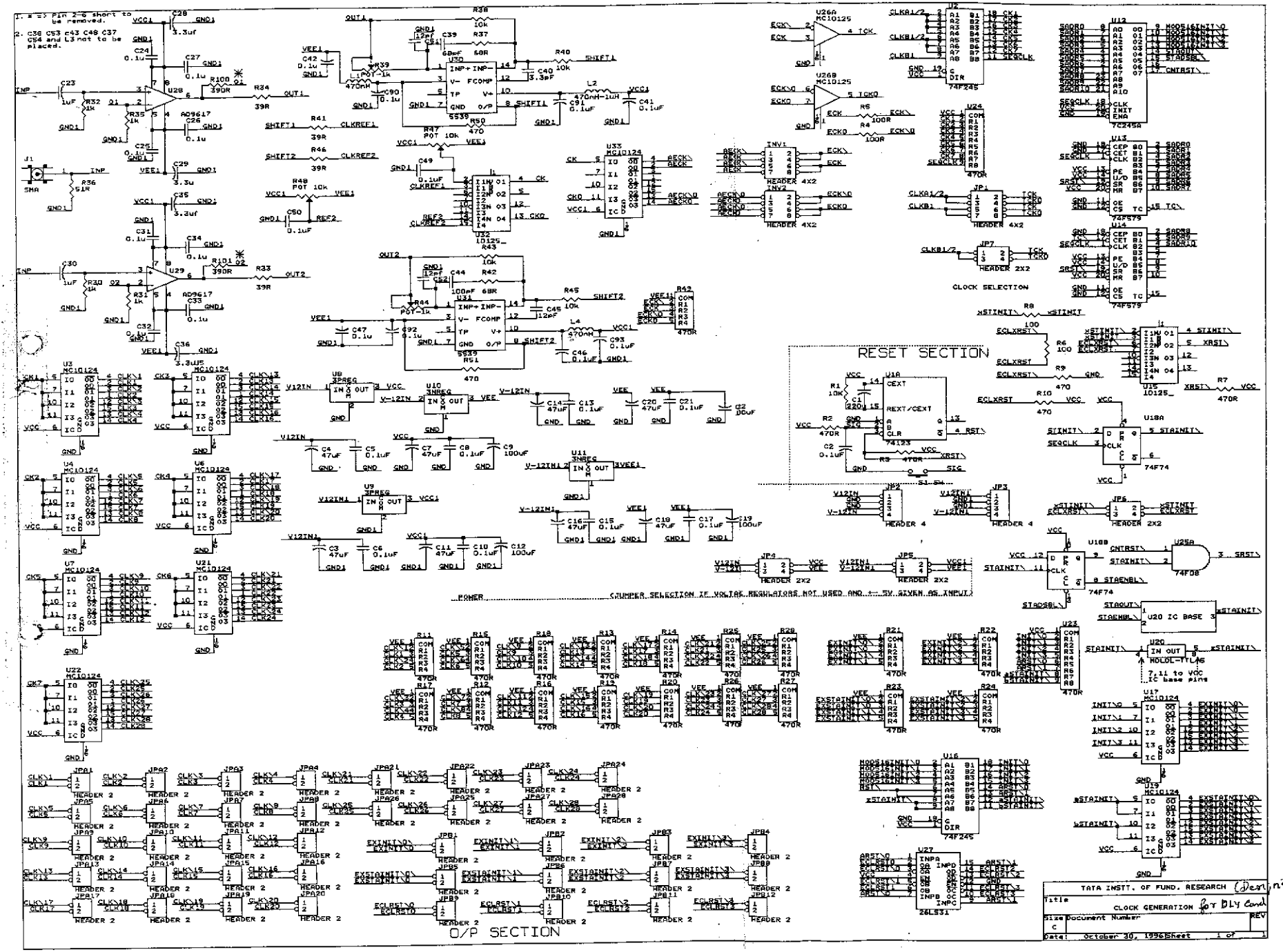
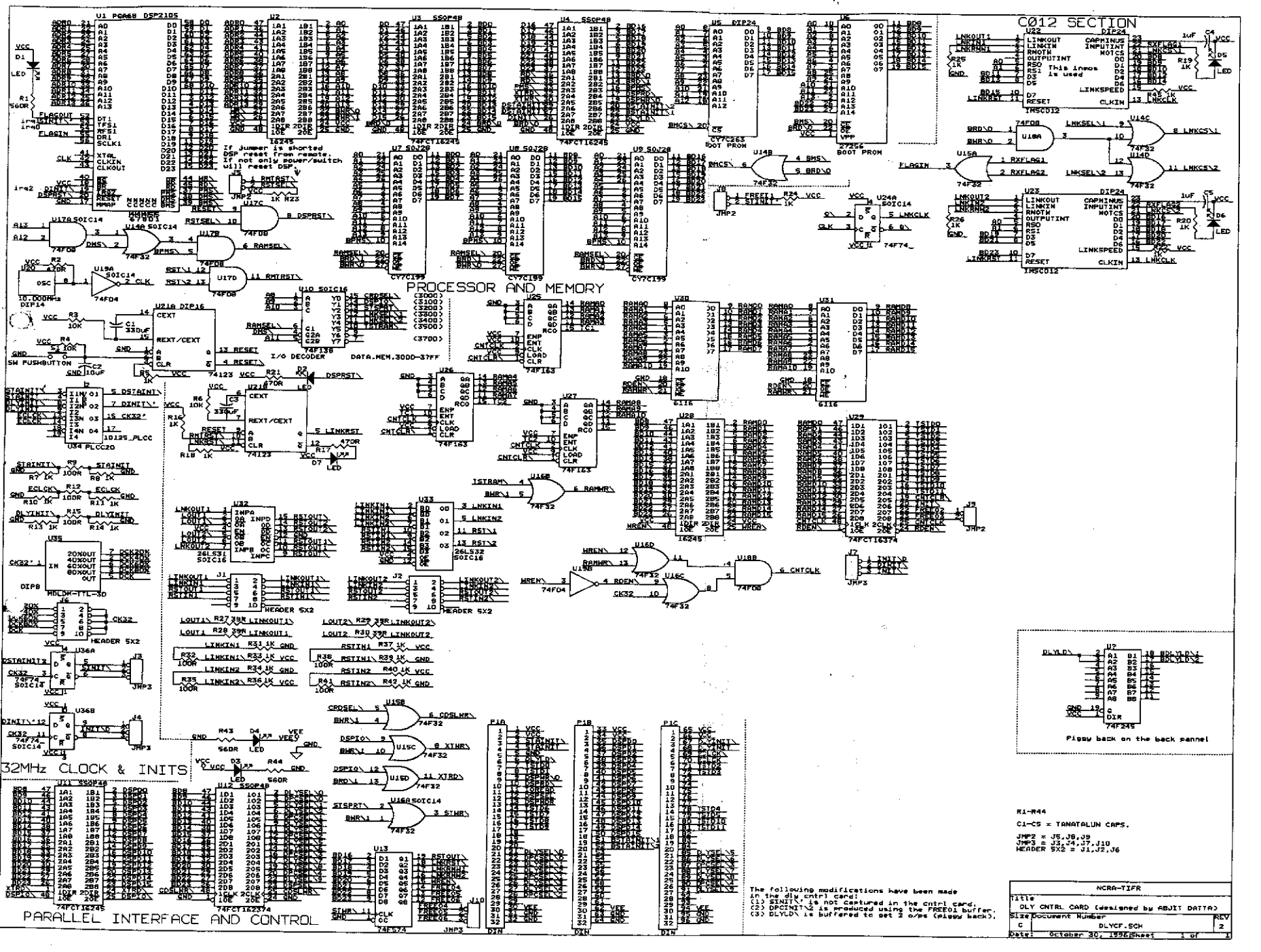
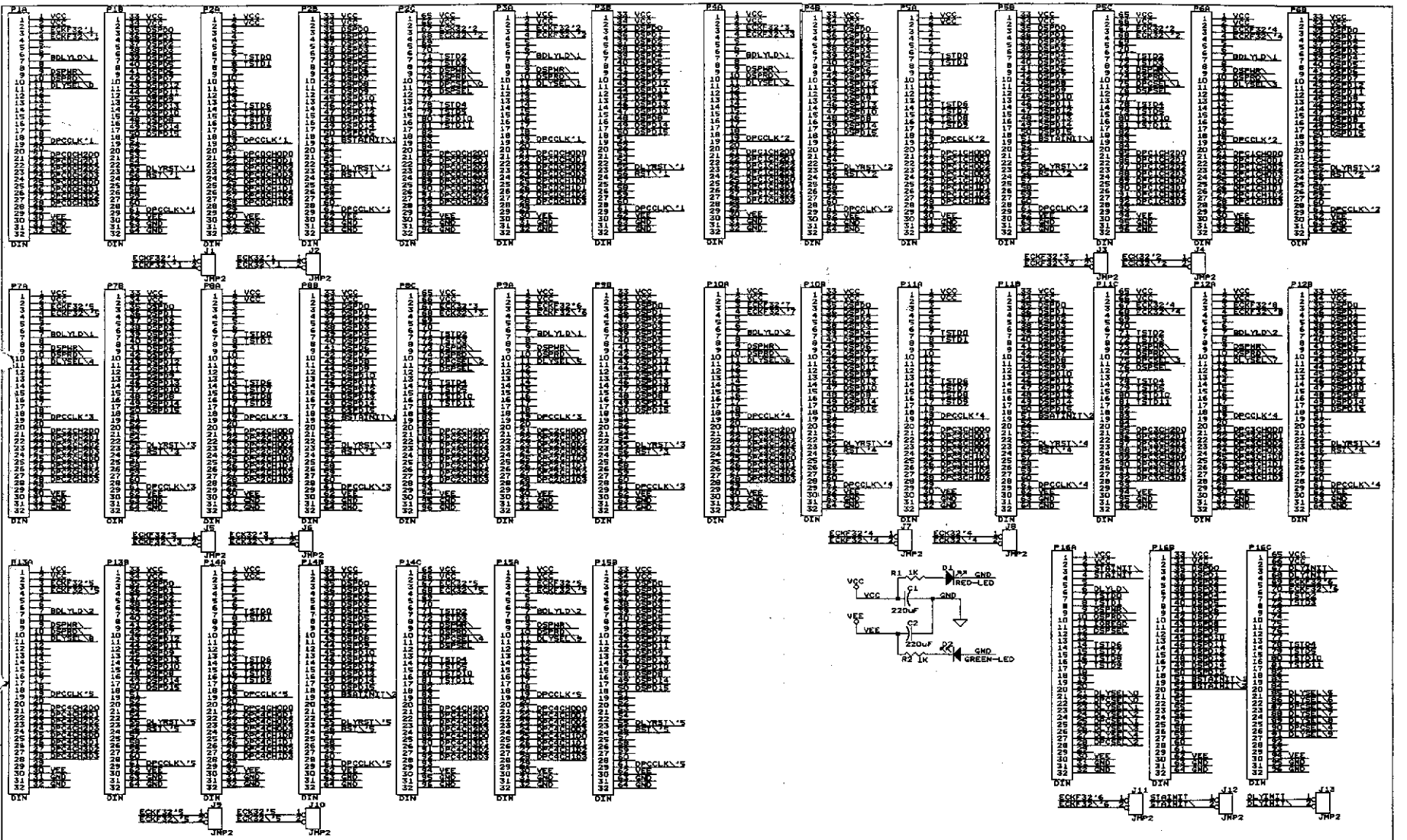
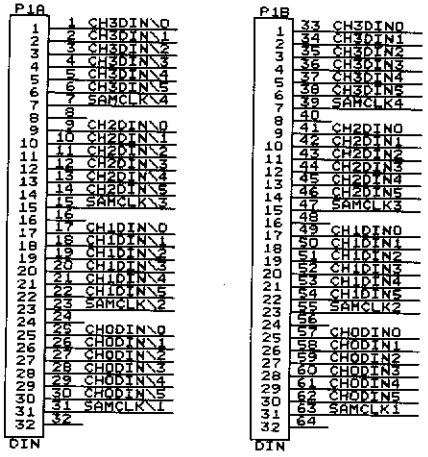
Date: October 31, 1996	Sheet 4 of 4
REV	

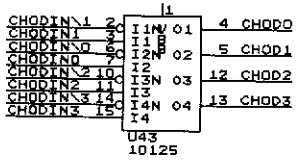

1. R 51 Pin 2-6 short to be removed.
2. C38 C53 C43 C48 C37 C54 and L3 not to be placed.
RESET SECTION
CLOCK SELECTION
POWER
JUMPER SELECTION IF VOLTAK REGULATORS NOT USED AND +-5V FROM AGNEW
O/P SECTION
TATA INSTT. OF FUND. RESEARCH
Design by Rakesh M
Title
CLOCK GENERATION for DLy card
Size
Document Number
REV
Date: October 30, 1996 Sheet 1 of 1

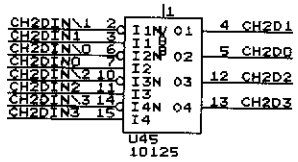

C012 SECTION
PROCESSOR AND MEMORY
I/O DECODER
DATA.MEM.3000-37FF
32MHz CLOCK & INITS
PARALLEL INTERFACE AND CONTROL
Piggy back on the back pannel
R1-R44
C1-C5 = TANATALUN CAPS.
JMP2 = J5,J8,J9
JMP3 = J3,J4,J7,J10
HEADER 5X2 = J1,J2,J6
The following modifications have been made in the dly cntrl card:
(1) SINIT\ is not captured in the cntrl card.
(2) DPCINIT\2 is produced using the FREE01 buffer.
(3) DLYLD\ is buffered to get 2 o/ps (piggy back).
NCRA-TIFR
DLY CNTRL CARD (designed by ABJIT DATTA)
DLYCF.SCH
October 30, 1996
1 of 1

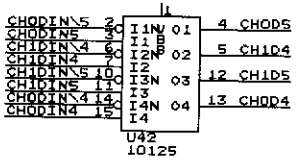

NCRA-TIFR
Title
DELAY-DPC BACK PLANE PCB (by A. DATTA)
Size Document Number REV
C DLYBPLN.SCH 2
Date: October 30, 1996 Sheet 1 of 1

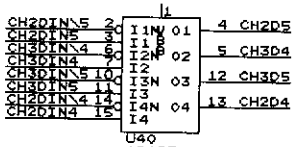
DPC 4 Sheets

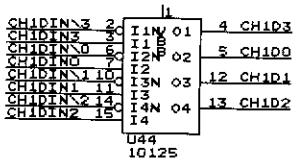


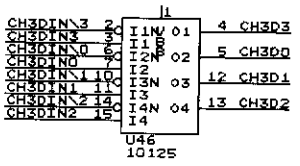


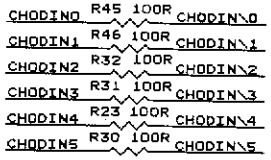


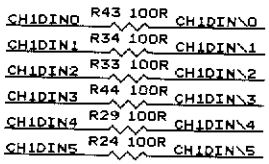


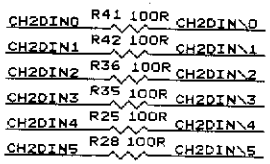


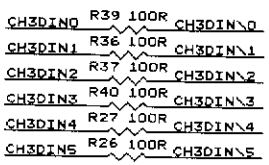




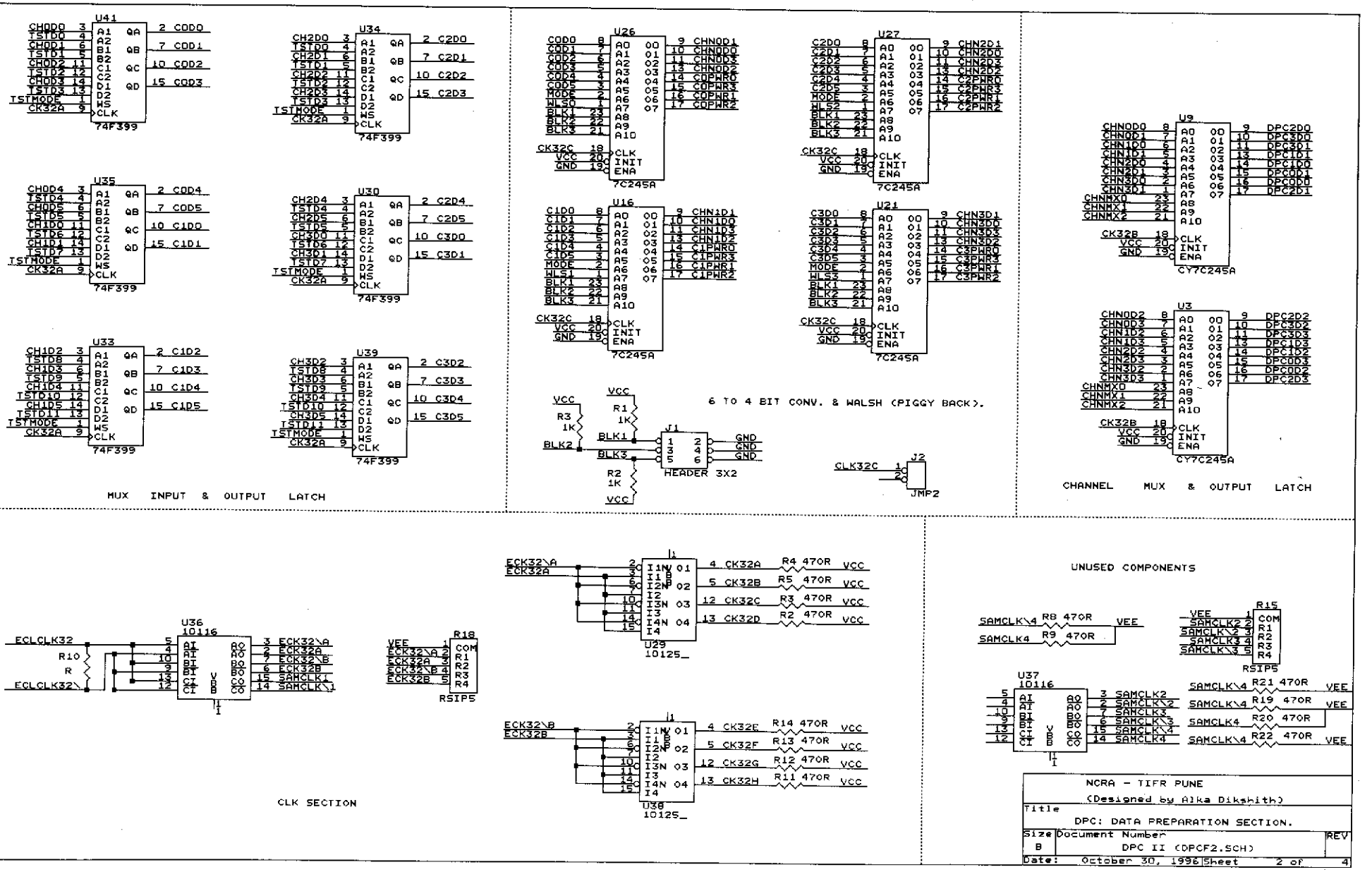


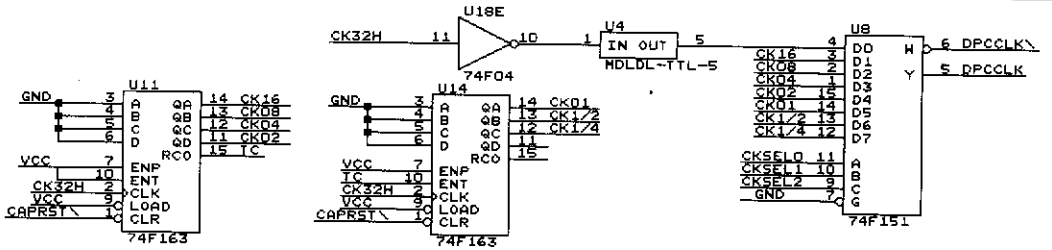




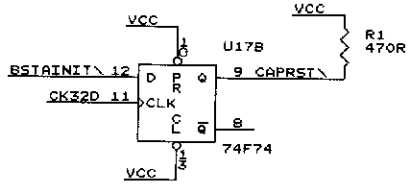


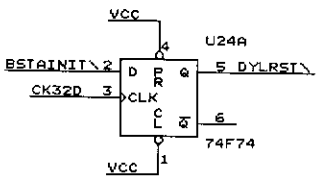
NCRA-TIFR PUNE	
(Designed by Alka Dikshith)	
Title	DPC: INPUT DATA CONVERSION (ECL to TTL)
Size B	Document Number DPC CARD I (DPCF1.SCH) REV
Date: October 30, 1996	Sheet 1 of 4


MUX INPUT & OUTPUT LATCH
6 TO 4 BIT CONV. & WALSH (PIGGY BACK).
CHANNEL MUX & OUTPUT LATCH
CLK SECTION
UNUSED COMPONENTS
NCRA - TIFR PUNE
(Designed by Alka Dikshith)
Title
DPC: DATA PREPARATION SECTION.
Size B
Document Number
DPC II (DPCF2.SCH)
REV
Date: October 30, 1996 Sheet 2 of 4

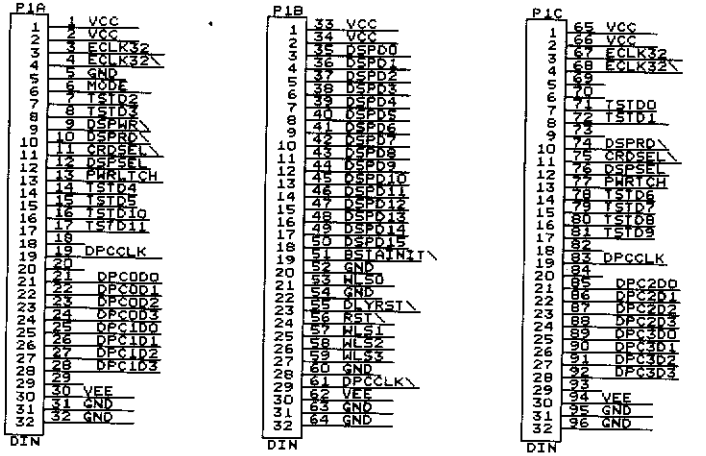


CLKS FOR DELAY CARDS



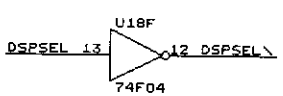


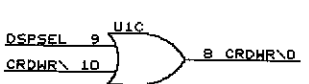
CAPTURED STAINIT FOR DELAY CARDS

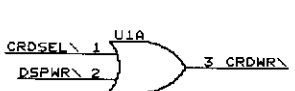


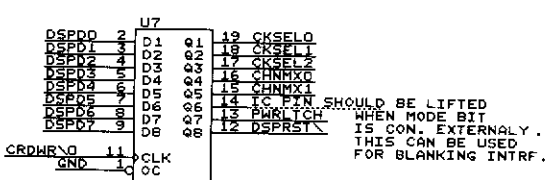
BACK PANNEL CONNECTORS

(24)

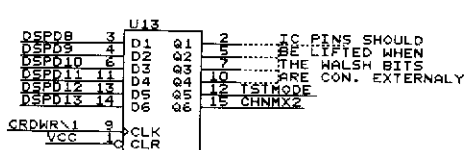




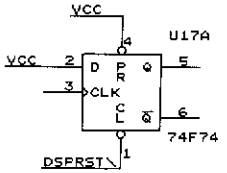


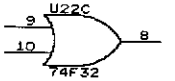


UNUSED COMPONENTS

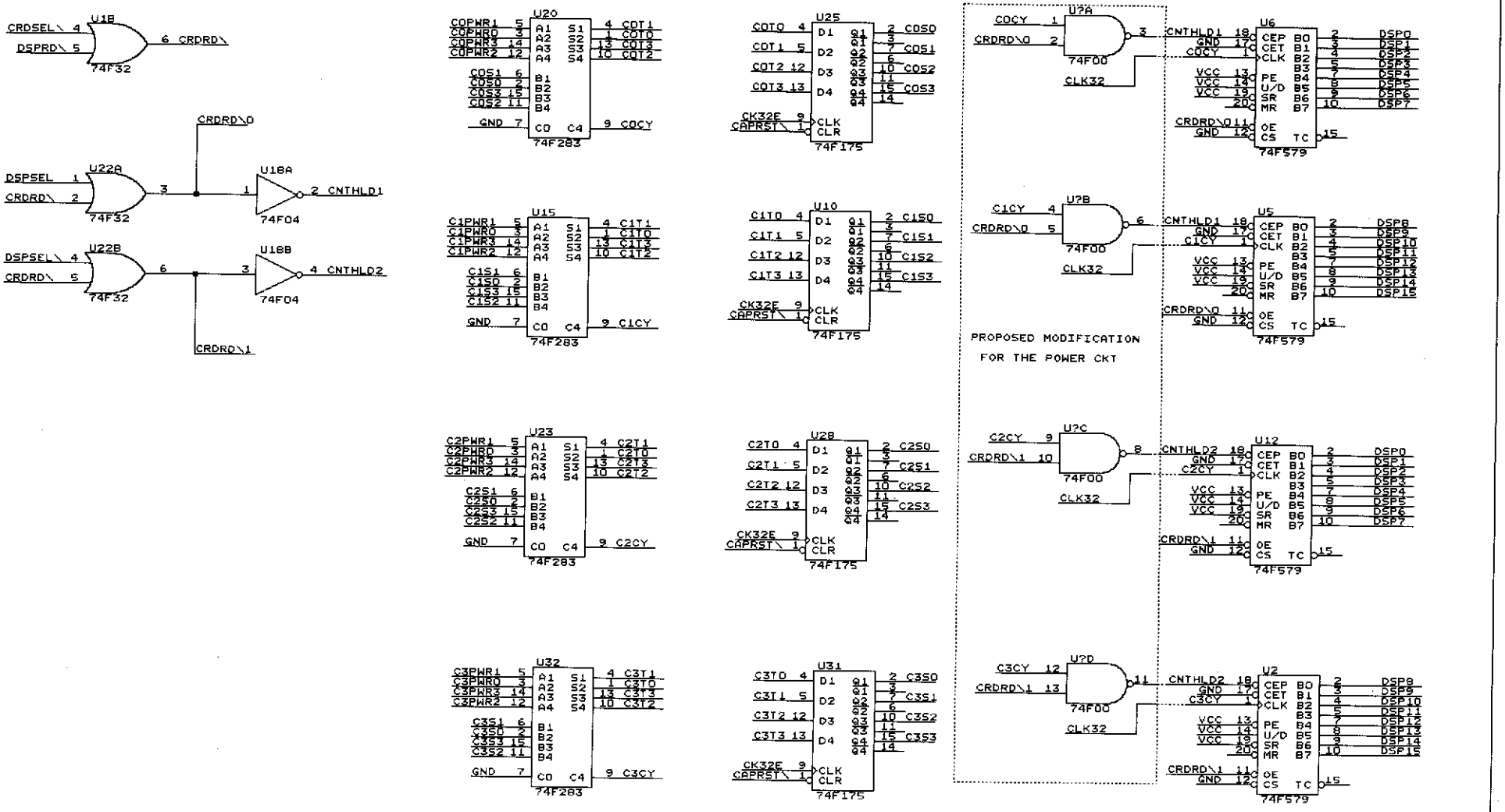


CONTROL WORD FROM DSP

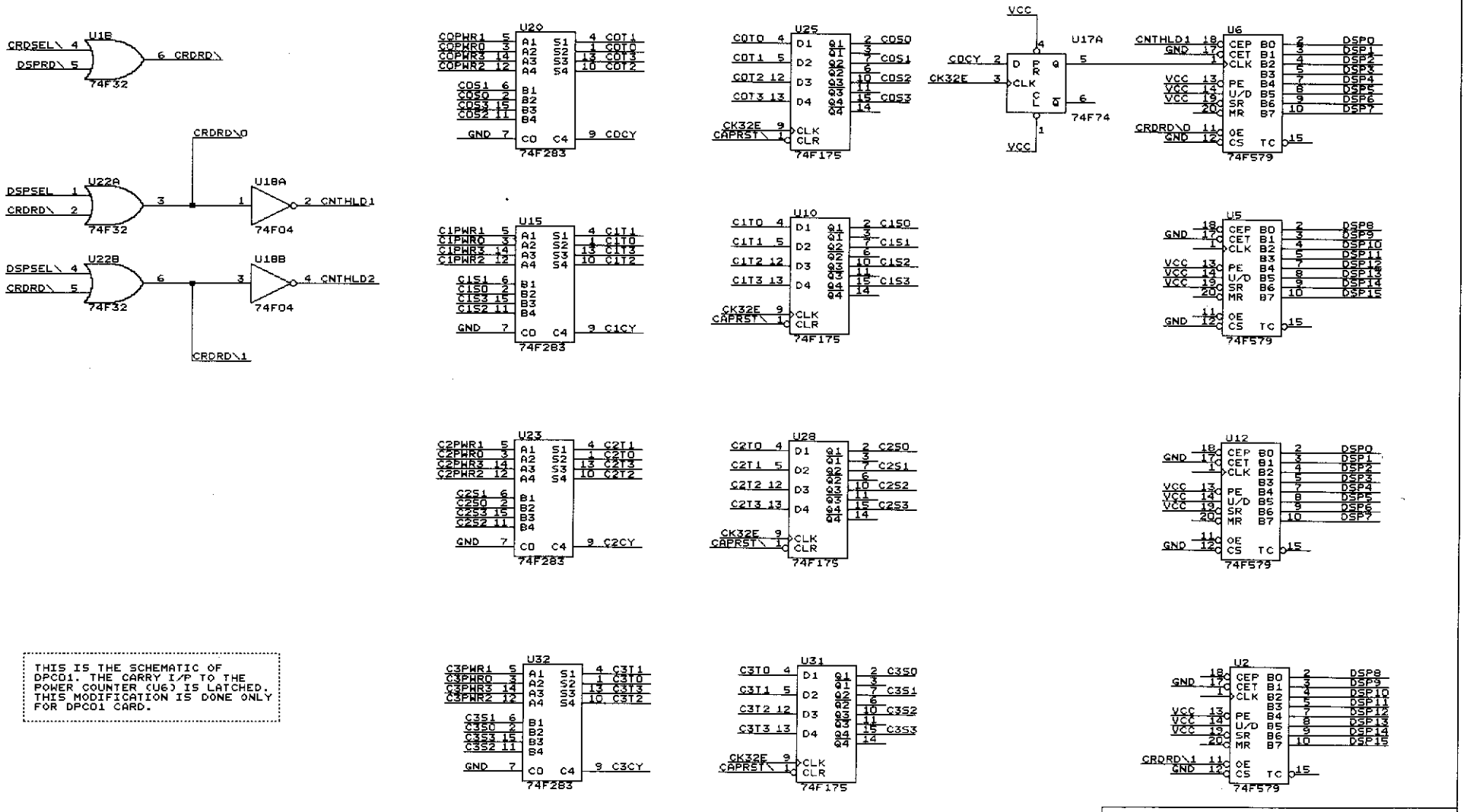




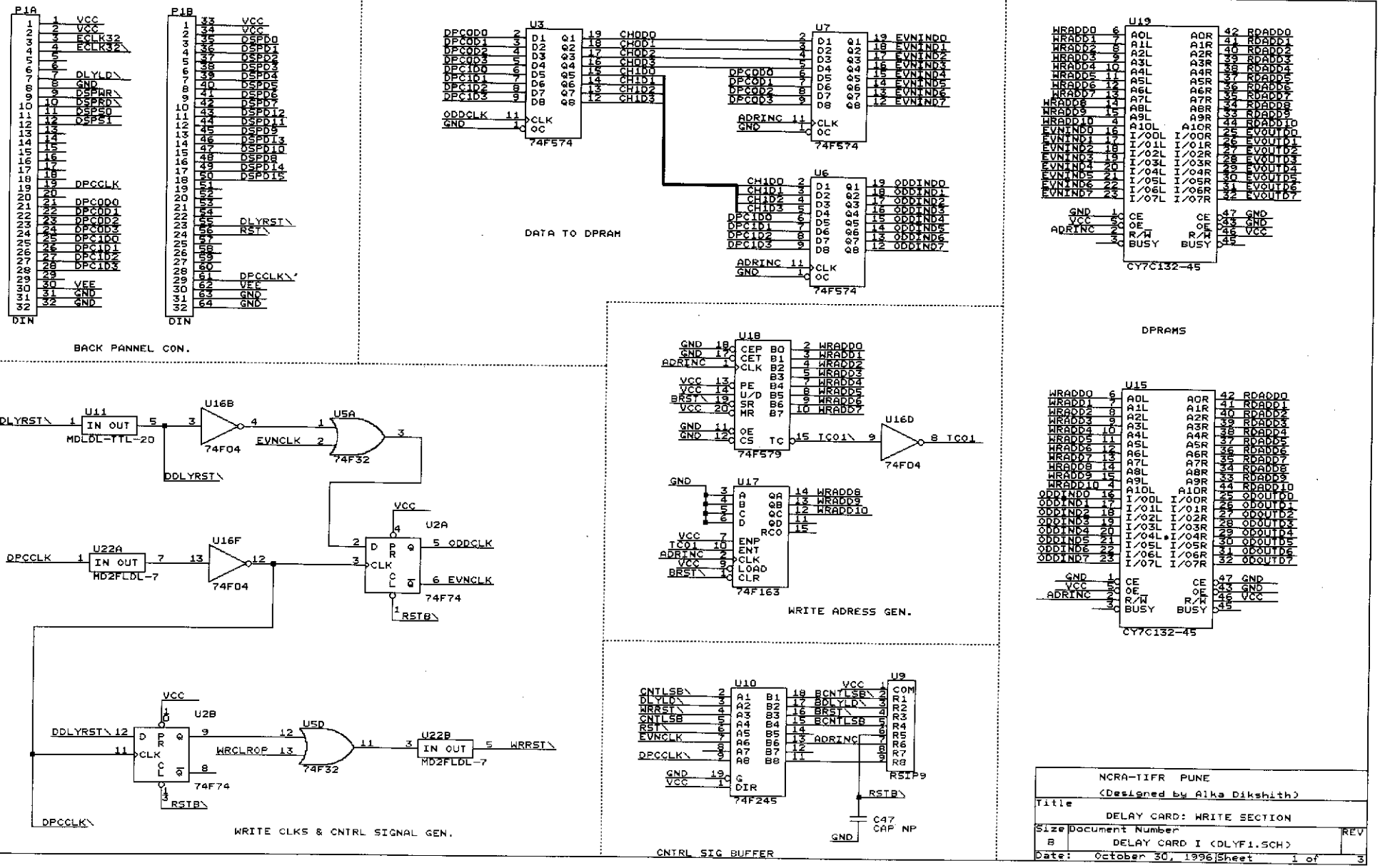
NCRA - TIFR PUNE (Designed by Alka Dikshith)		
Title: DPC: RST & CLK FOR DLY CARD; DPC CNTRL WORD.		
Size: B	Document Number: DPC III (DPCF3.SCH)	REV
Date: October 30, 1996	Sheet 3 of 4	

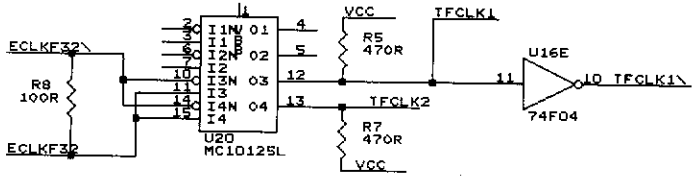


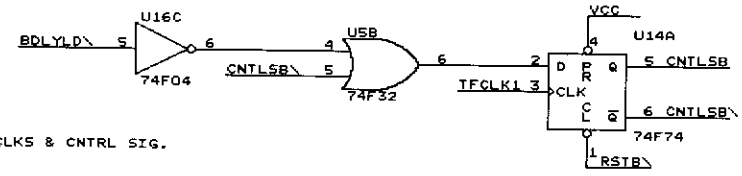
NCRA-TIFR PUNE (Designed by Alka Dikshith)		
Title: DPC: POWER ACCUM.		
Size: B	Document Number: DPC IV (DPCF4.SCH)	REV
Date: October 30, 1996	Sheet 4 of 4	


U1B
CRDSEL\ 4
DSPRD\ 5
6 CRDRD\
74F32
CRDRD\0
U22A
DSPSEL 1
CRDRD\ 2
3
74F32
U18A
1
2 CNTHLD1
74F04
U22B
DSPSEL\ 4
CRDRD\ 5
6
74F32
U18B
3
4 CNTHLD2
74F04
CRDRD\1
U20
COPWR1 5
COPWR0 3
COPWR3 14
COPWR2 12
COS1 6
COS0 2
COS3 15
COS2 11
GND 7
A1 A2 A3 A4
B1 B2 B3 B4
S1 S2 S3 S4
CO C4
4 COT1
1 COT0
13 COT3
10 COT2
9 CDCY
74F283
U25
COT0 4
COT1 5
COT2 12
COT3 13
CK32E 9
CAPRST\ 1
D1 D2 D3 D4
CLK CLR
Q1 Q2 Q3 Q4
2 COS0
3 COS1
6 COS2
11 COS3
14
74F175
VCC
4
U17A
CDCY 2
CK32E 3
D PR Q
CLK
CL Q
5
6
74F74
1
VCC
U6
CNTHLD1 18
GND 17
1
VCC 13
VCC 14
VCC 19
20
CRDRD\0 11
GND 12
CEP CET CLK PE U/D SR MR OE CS
B0 B1 B2 B3 B4 B5 B6 B7 TC
2 3 4 5 6 7 8 9 10 15
DSP0 DSP1 DSP2 DSP3 DSP4 DSP5 DSP6 DSP7
74F579
U15
C1PWR1 5
C1PWR0 3
C1PWR3 14
C1PWR2 12
C1S1 6
C1S0 2
C1S3 15
C1S2 11
GND 7
4 C1T1
1 C1T0
13 C1T3
10 C1T2
9 C1CY
74F283
U10
C1T0 4
C1T1 5
C1T2 12
C1T3 13
CK32E 9
CAPRST\ 1
2 C1S0
3 C1S1
6 C1S2
11 C1S3
14
74F175
U5
18
GND 17
1
VCC 13
VCC 14
VCC 19
20
11
GND 12
DSP8 DSP9 DSP10 DSP11 DSP12 DSP13 DSP14 DSP15
74F579
U23
C2PWR1 5
C2PWR0 3
C2PWR3 14
C2PWR2 12
C2S1 6
C2S0 2
C2S3 15
C2S2 11
GND 7
4 C2T1
1 C2T0
13 C2T3
10 C2T2
9 C2CY
74F283
U28
C2T0 4
C2T1 5
C2T2 12
C2T3 13
CK32E 9
CAPRST\ 1
2 C2S0
3 C2S1
6 C2S2
11 C2S3
14
74F175
U12
18
GND 17
1
VCC 13
VCC 14
VCC 19
20
11
GND 12
DSP0 DSP1 DSP2 DSP3 DSP4 DSP5 DSP6 DSP7
74F579
(26)
THIS IS THE SCHEMATIC OF DPC01. THE CARRY I/P TO THE POWER COUNTER (U6) IS LATCHED. THIS MODIFICATION IS DONE ONLY FOR DPC01 CARD.
U32
C3PWR1 5
C3PWR0 3
C3PWR3 14
C3PWR2 12
C3S1 6
C3S0 2
C3S3 15
C3S2 11
GND 7
4 C3T1
1 C3T0
13 C3T3
10 C3T2
9 C3CY
74F283
U31
C3T0 4
C3T1 5
C3T2 12
C3T3 13
CK32E 9
CAPRST\ 1
2 C3S0
3 C3S1
6 C3S2
11 C3S3
14
74F175
U2
18
GND 17
1
VCC 13
VCC 14
VCC 19
20
CRDRD\1 11
GND 12
DSP8 DSP9 DSP10 DSP11 DSP12 DSP13 DSP14 DSP15
74F579
NCRA-TIFR PUNE
(Designed by Alka Dikshith)
Title
DPC: POWER ACCUM. OF DPC01 CARD.
Size B
Document Number
DPC V (DPCF5.SCH)
REV
Date: October 30, 1996 Sheet 1 of 1

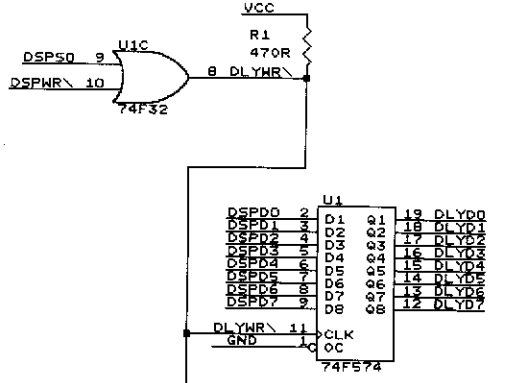
DELAY CARD 3 Sheets



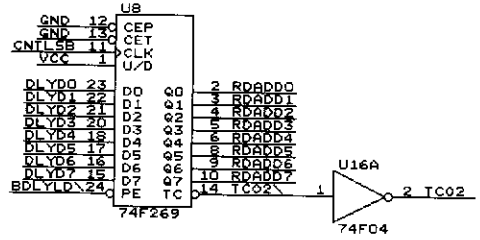


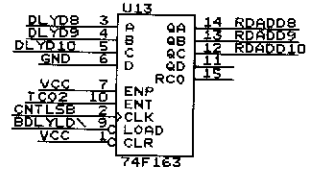


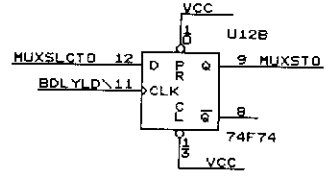
READ CLKS & CNTRL SIG.

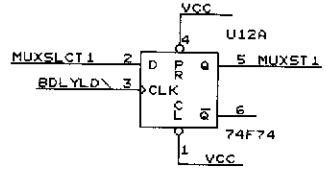


DLY VALUE FROM DSP

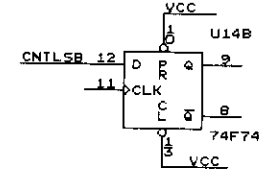




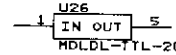




READ ADDRESS GEN.



UNUSED COMPONENTS

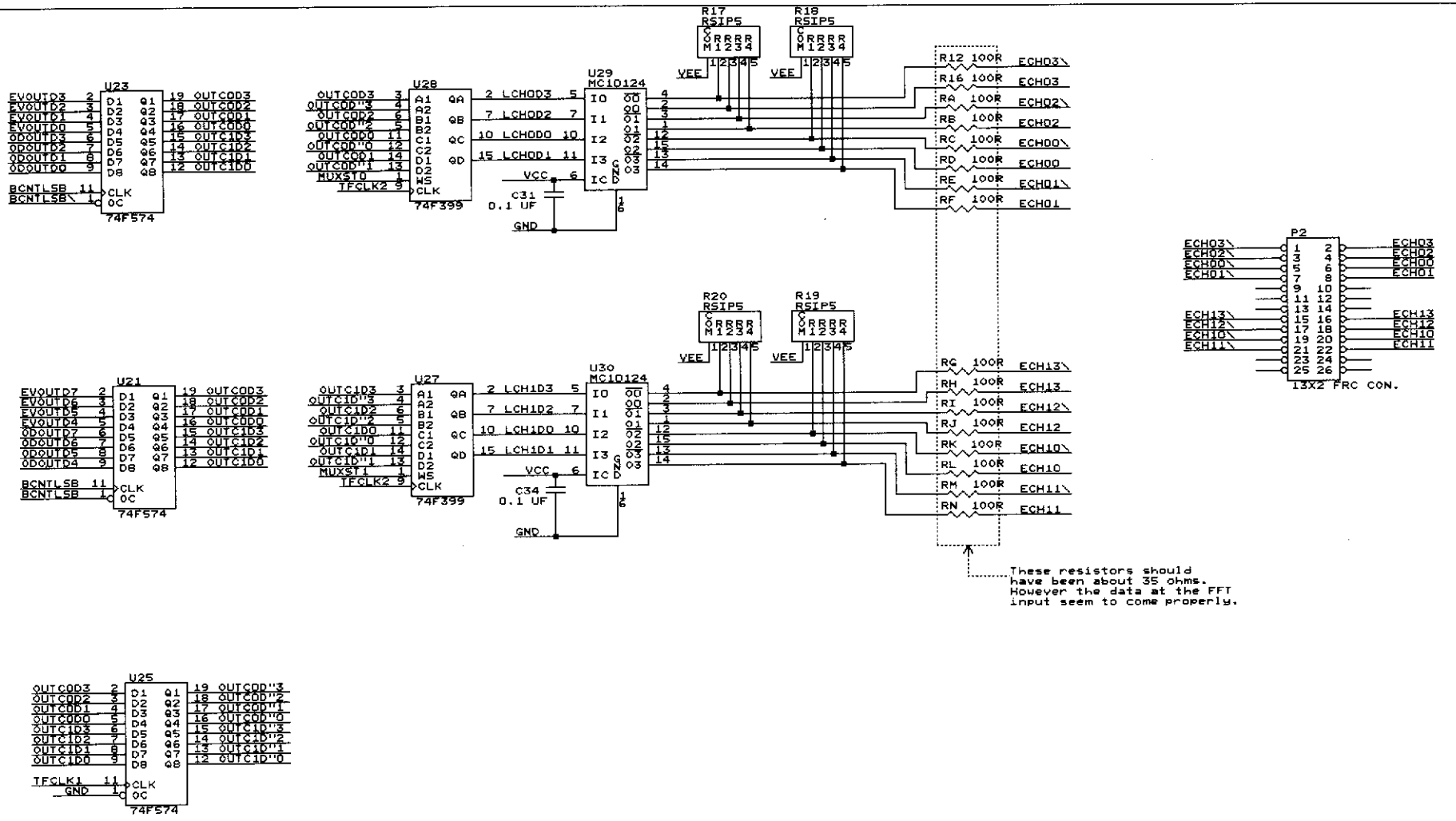


NCRA-TIFR PUNE
(Designed by Alka Dikshith)

Title
DELAY CARD: RD CLK, CNTRL SIG & ADDR GEN

Size	Document Number	REV
B	DELAY CARD II (DLYF2.SCH)	

Date: October 30, 1996 Sheet 2 of 3



NCRA-TIFR PUNE (Designed by Alka Dikshith)		
Title: DELAY CARD: DATA READING SECTION		
Size: B	Document Number: DELAY CARD III (DLYF3.SCH)	REV
Date: October 30, 1996	Sheet 3 of 3	

The following is the test procedure for validating the DPC cards (assuming the Control card and its interface works!)
- BangaraRaju, Markandeyulu 2nd July 1996.

Verify the power supply output points and ensure +5.00(Vcc) and -5.20(Vee) are set properly.

First ensure that the Control Card is plugged properly into the backplane slot(P16 - 7th slot from the left - 96pin euro).
Make sure the Clock input (J11), STAINIT\(J12) and DLYINIT\(J13) are properly connected on the backplane(rear).

Insert the DPC card into one of the corresponding slots(P2, P5, P8, P11, P14 - 96pin euro) and ensure the clock input is connected in the respective clock jumper on the backplane.

Step 1: Setup the control card and get the kernel running.

At the PC prompt run
>> fc2105 <return>
This gives a menu on the screen describing various commands.

Select '2' for FO led test and see if the FO led on the control card (top corner) blinks.

-- Select '0' for downloading .exe file
give 'tstdata.exe' as the argument
(To download 2048 words for TSTData, CLR, INIT etc and store in external data ram in the buffer tst_data)

-- Select '5' for downloading test data on to the control card RAMs.

-- Select '0' for downloading .exe file
give 'dpc_cmd.exe' as the argument
(This enables the user to send various control words to a selected DPC card)

-- Select '6' for sending a DPC command
give card address (5 for broadcast) and 3040(test mode)
2040(normal mode)
(This enables the asynchronous reset to the selected DPC card(s))

-- Select '6' for sending the next DPC command
give card address and 30c0(test mode)
20c0(normal mode)
(This disables the asynchronous reset)

This much setup is bare minimum for checking the various control signals on the DPC card.

Set the oscilloscope trigger level to ECL level(about -1.0Volts).
- Check U29 - 2 & 3, U38 - 2 & 3
(Clocks to the Sampler need not be checked since in the final system the clock to the Sampler is not supplied from the DPC)
Look for a proper clock of 32ns period.

Set the oscilloscope trigger level for a TTL signal(about +2.5Volts).
- Check U41, U34, U35, U30, U33, U39 - pin 9 (CLK32A)
  U9, U3 - pin 18 (DCK32B\)
  U18 - pins 5 & 6 (CK32B)
  U29 - pin 12 (this is directly wired to the piggy back card)
  U24 - pin 3 (CK32D)
  U17 - pin 11 (CK32D)
  U25, U10, U28, U31 - pin 9 (CK32E)
  U11, U14 - pin 2 (CK32H)
  U8 - pin 4 (CK32H)
  Look for a proper clock with 32ns period.

- Latch a probe on to U8 - pin 6.(ADRCLK\)
-- Select '6' for sending a DPC command
  give card address and control word as 3041 and look for a
  divide-by-2 clock.
(Repeat this for 3042 to 3047 and observe the change in the clock period)

- Latch probe on U13-9 or U7-11 (CRDWR0\) Scope in single shot mode.
-- Select '6' for sending a DPC command
  give card address and control word as 3040
- Check if CRDWR0\ shows a pulse.

- Verify the control word set on the latches U7 & U13.
- TestMode / NormalMode :
  Latch a probe on to U13 - pin 12.(TSTMODE)
-- Select '6' for sending a DPC command
  give card address and control word as 20c0 for TSTMODE=0
  30c0 for TSTMODE=1

- INITs and Resets
-- Select '6' for sending a DPC command
  give card address and control word as 3040.
(This makes DSPRST\ 'lo' and enables the one-time reset RST\)
- Check if DLYINIT\ is coming on U22-10.
- Check if RST\ is enabled on U22 - pin 6. (pulse=64ns; period=32ms)
- Check if CAPRST\ is also coming on U17-9. (pulse=64ns; period=32ms)
-- Select '6' for sending a DPC command
  give card address and control word as 30c0.

-- Select '0' for downloading .exe file
  give 'POWER.EXE' as the argument
-- Select '0' for downloading .exe file
  give 'PWRAPP.EXE' as the argument
(Once these two .exe files are loaded Power reading option in the
main menu is enabled)
- Latch a probe on U18-13 (DSPSEL) and configure the scope for single shot mode.
-- Select '7' for reading power from DPC
  give card address and select DSPSEL = 0 or DSPSEL =1
- Check if the signal DSPSEL is toggling
- Check on U22-3 (CRDRD0\) for DSPSEL=0
  U22-6 (CRDRD1\) for DSPSEL=1

Data Path:
-- Select '0' for downloading .exe file
give DPC_CMD.EXE as argument
-- Select '6' for sending a DPC command
give card address and control word as 2040
-- Select '6' for sending a DPC command
give card address and control word as 20c0 (Normal data)

- If no input is given the DPC card, the first stage ECL-TTL converters will output a '0'.
- Check on U43, U45, U42, U40, U44, U46 - pins 4, 5, 12, 13 for a '0'
- Since NormalMode is selected the output of the MUX(74F399) should also be a '0'
- Check U41, U34, U35, U30, U33, U39 - pins 2, 7, 10, 15.

- Check U16, U21, U26, U27 if the addresses are all '0' (CODEROM)
(The CODEROM data for address=0x00 is 0x7F)
- Check U16, U21, U26, U27 if the output is 0x7F (CODEROM)

(The output of the CODEROM goes to the MUXROM)
- Check U3 and U9 for address = 0x4FF
(In the MUXROM for address = 0x4FF, data = 0xFF)

-- Select '6' for sending a DPC command
give card address and control word as 3040
-- Select '6' for sending a DPC command
give card address and control word as 30c0 (TSTMODE)
- Probe on U20, U15, U23, U32 for the 4-bit input from CODEROM
(It should read '0' on pins 3, 5, 12 and a pulse train on pin 14
width=32ns; period=16us)

- With this data probe on U20, U15, U23, U32 - pin 9 for the carry output.
(It should have a pulse train of width=32ns; period=64us)

-- Select '0' for downloading .exe file
give 'POWER.EXE' as the argument
-- Select '0' for downloading .exe file
give 'PWRAPP.EXE' as the argument
(Once these two .exe files are loaded Power reading option in the main menu is enabled)
-- Select '7' for reading power
give card address and select DSPSEL=0 for U5 & U6
DSPSEL=1 for U2 & U12

-- Select '3' for reading data from 2105 Memory
give no. of values to be read and choose DM ('0')

(The choosen number of counter data is displayed. The data, in TSTMODE should have identical bytes and each value should repeat 4 times.
Eg: 3232
3232
3232
3232

3333
3333
3333
3333
3434
3434
3434
3434

The following is the test procedure for validating the DPC cards (assuming the Control card and its interface works!)
- BangaraRaju, Markandeyulu 8th July 1996.

Verify the power supply output points and ensure +5.00(Vcc) and -5.20(Vee) are set properly.

First ensure that the Control Card is plugged properly into the backplane slot(P16 - 7th slot from the left - 96pin euro).
Make sure the Clock input (J11), STAINIT\(J12) and DLYINIT\(J13) are properly connected on the backplane(rear).

Insert the Delay card into one of the corresponding slots(P1, P3, P4, P6, P7, P9, P10, P12, P13, P15 - 96pin euro) and ensure the clock input is connected in the respective clock jumper on the backplane.

Step 1: Setup the control card and get the kernel running.

At the PC prompt run
>> fc2105 <return>
This gives a menu on the screen describing various commands.

Select '2' for FO led test and see if the FO led on
the control card (top corner) blinks.

-- Select '0' for downloading .exe file
give 'tstdata.exe' as the argument
(To download 2048 words for TSTData, CLR, INIT etc and store in external data ram in the buffer tst_data)

-- Select '5' for downloading test data on to the control card RAMs.

-- Select '0' for downloading .exe file
give 'dpc_cmd.exe' as the argument
(This enables the user to send various control words to a selected DPC card)

-- Select '6' for sending a DPC command
give card address (5 for broadcast) and 3040(test mode)
2040(normal mode)
(This enables the asynchronous reset to the selected DPC card(s))

-- Select '6' for sending the next DPC command
give card address and 30c0(test mode)
20c0(normal mode)
(This disables the asynchronous reset)

This much setup is bare minimum for checking the various control signals on the Delay card.

- On the clock(ECL) input two terminating resistors(100ohm) are put on the same pair, giving a effective line-to-line termination of 50 ohms!! Remove one of resistors (R6 preferably) and verify that

the line-to-line termination is 100ohms.

- Set the oscilloscope trigger level to ECL level(about -1.0Volts).
- Check U20 - pins 10, 11, 14, 15
  Look for a proper clock of 32ns period.

- Set the oscilloscope trigger level for a TTL signal(about +2.5Volts).
- Check U20 - pins 12(IFCLK) & 13(TFCLK)
  Look for a proper TTL clock of 32ns period.

- Probe on U2 - 3 and check for a clock (DPCCLK)
  U16 - 13 and check for a clock (DPCCLK\)
(This depends on the CKSEL option choosen on the DPC card)

- Check for the following clocks and control signals
  U2-11, U10-11 (DPCCLK\\')
  U16-12 (DPCCLK\\)
  U25-11, U27,U28-9 (DFCLK)
  U24-11 (IFCLK)

(Some of the signals are latched on the Delay card using 32MHz clock)
  U2-5, U3-11 (ODDCLK)
  U2-6, U6,U7-11 (EVENCLK)

  U14-5, U16-3 (CNTLSB)
  U10-2, U16-4 (CNTLSB\)
  U10-18, U11-5 (BCNTLSB\)
  U11-6 (LACHCLK)
  U2-9 (ADRINC)
  U10-15 (BCNTLSB)
  U10-13 (RAMWR\)
  U16-6 (O/PENBL\)

  U10-16 (BRST\) This is DLYINIT\ captured on DPC card by 32MHz clock.
  width=64ns; period=32ms
-- Select '0' for downloading .exe file
  give 'dpc_cmd.exe' as argument
-- Select '6' for giving a DPC command
  give card address and control word as 3040
  U10-14 (RSTB\) This is a one-time reset from the DPC card.
  width=64ns; period=32ms
-- Select '6' for giving a DPC command
  give card address and control word as 30c0
  U14-9 (CDLYLD\) This TDLYLD\ captured by CNTLSB

  The Read and Write addresses for U15 and U19 have be checked.
  U15, U19-pins 4,15-6 (WRADD[10..0])
  U15, U19-pins 44,33-42 (RDADD[10..0])

Data Path:
  With the current test data being loaded
  DPC input = 0x20 corresponds to Delay input = 0x00
  DPC input = 0x37 corresponds to Delay input = 0x05 (per channel)

(Assuming the DPC is configured for test mode.)

- Check U3 input
The data is having a single pulse(32ns) of value 0x55 in a 16us period.
As per the timing this data can only be latched by the EVENCLK.
- Check the output of U3 is 0x00.
- Check if U6 & U7 latch the data 0x55.
This data is now written into the DPRAMs.
- Check EVNIND[7..0] on U19 & ODDIND[7..0] on U15 - pins 23-16
- Check the DPRAMs give out the same data at the output.
EVOUTD[7..0] on U19 & ODOUTD[7..0] on U15 - pins 32-25
- This data is latched in U21 & U23, the whose outputs are tied together. (OUTC0D[3..0], OUTC1D[3..0])
- For MUXST[1..0] = 0,
The data from U21 & U23 is selected in U27 & U28.
For MUXST[1..0] = 3,
The data from U24 is selected in U27 & U28.
- Check if U27 & U28 give a pulse of value 0x06.

Corrections required for the DPC Card

The following chips should NOT be populated : U19(74F32)

Remove IC base of U24(74F74) and solder the IC directly on to the card.

Put the following straps:

1. Put a thick wire from
   P1-A1,B1,C1 to L1-1 (bypassing the fuse and the inductor).

2. P1-B16 to U13-14

3. U13-15 to U3-21 & U9-21

4. U38-8 to Vee. (Piggy back base has to be put and the
   (corresponding pins on the card to be removed)

5. U17-4 to U19-6 & U19-3

6. U22-3 to U18-1
   U22-6 to U18-3

   U18-2 to U5-18 & U6-18
   U18-4 to U2-18 & U12-18

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7. Put a 150pf capicitor on the following:
   U15-9 to GND
   U20-9 to GND
   U23-9 to GND
   U32-9 to GND

Corrections required for the Delay Card

The following chips should NOT be populated : U11(74F08)
U22 & U28(Delay-line)

Remove resistor R6(100ohms)(Duplicate termination on the ECL clock)

Put the following straps:

1. Put a thick wire from
   P1-A1,B1 to L1-1 (bypassing the fuse and the inductor).

2. U28-2 to U29-5
   U28-7 to U29-7

3. U27-2 to U30-5
   U27-7 to U30-7

4. U26-1 to U26-5 (bypassing the delay-line)

5. U22-1 to U22-5 (bypassing the delay-line)

6. U18-19 to U17-1 (Piggy back base has to be put and the
   U18-20 to Vcc (corresponding pins on the card to be removed)

7. U14-1 to U10-14 (Piggy back base has to be put and the
   (corresponding pins on the card to be removed)

8. U30-8 to Vee (Piggy back base has to be put and the
   (corresponding pins on the card to be removed)

9. U11-5 to U11-6