DSP Platform for Pulsar Signal Processing

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Overview

Here we give an overview of the objectives, the overall signal flow and the projected time scales and manpower requirements for the DSP Platform for pulsar signal processing, being built by us at NCRA.

Objectives

The prototype of a DSP platform to meet the major requirements of pulsar signal processing for the GMRT is being presently implemented. This platform aims to provide two kinds of processing modes - coherent dedispersion mode (CD mode) and incoherent dedispersion (ID) mode. In both modes, the signals can be processed with full polarimetry information i.e. all 4 Stokes parameters can be available.

In the CD mode, the prototype will have the following capabilities : (i) take the GMRT Array Combiner (GAC) output for one sideband (phased array sum for 256 complex spectral channels at an effective rate of 16 Msamples/sec) and both polarisations. (ii) perform inverse FFT to obtain the phased array time domain signal (in quadrature sampling mode i.e. complex time samples at the rate of 16 Msamples/sec) for both polarisations. (iii) filter out a sub-band of 0.5 - 2 MHz from the time domain signals and do coherent dedispersion on these to obtain microsecond resolution data in all 4 Stokes parameters. (iv) perform time domain integration and/or time domain folding on the dedispersed data to obtain a final data rate compatible with the recording set-up (C-DAC DAS or S2 recorder).

In the ID mode, the prototype will have the following capabilities : (i) take the GAC output for one sideband (phased array sum for 256 complex spectral channels at an effective rate of 16 Msamples/sec) and both polarisations. (ii) compute Stokes parameters for data in each frequency channel, including correction for differential Faraday rotation across the band. (iii) post process the Stokes parameter time series with any of the following options : incoherent dedispersion , time domain integration , time domain folding , time domain

gating to obtain a final data rate compatible with the recording set-up (C-DAC DAS or S2 recorder).

The bulk of the signal processing computations required in the two modes are performed by an array of DSP chips (the ADSP-21020). A replica of the system will be needed to handle the second side band from GMRT. This status report describes the system architecture along with card level details.

Signal flow outline

Firstly we describe the overall signal flow in the two modes of operation. Figure 1 shows the overall block diagram of the system configuration.

For the CD mode the complex signal from the GAC (for each polarisation) is first inverse fourier transformed to get back the time domain signal corresponding to the GMRT phased array (coherent) sum. Since only the one sided spectra is available, the data are arranged to produce complex time domain signals, corresponding to quadrature sampled real time domain signals. In this mode, the first data conditioning card (DCC) is used simply to convert the data format to the NRAO ASIC format and the second DCC is used to convert from the NRAO ASIC mode to normal mode. Both the pipelines in the FFT card are fed with the same data (either L or R polarisation). The FFT system is clocked at 16 MHz rate for this mode. In this mode, the second stage TRIG inputs (T2) are taken as the TRIG values output by the FFT control card. The time resolution required dictates doing a coherent dedispersion of 0.5 - 2 MHz subbands at a time. Hence the 16 MHz complex signal is send through a digital filter card (DFC) where it is not only filtered but also decimated to the nyquist rate of the bandpass (1 - 4 MHz). The complex output from the filter card is read by a DSP microcomputer (the I/O node) and blocks of data are send sequentially to an array of DSP microcomputers for doing the coherent dedispersion. Each of the DSP microcomputer in the array, takes the required forward FFT (of $\approx$ 4K length) multiplies with the inverse of the transfer function of the ISM and then inverse fourier transforms it, to give the dedispersed time series. The time series for the two polarisations can then be simply "detected" and added to give the total power time series, or combined appropriately to obtain the time series for the 4 Stokes parameters. This data is read back sequentially by the I/O node from each of the DSP cards in the array. The data rate is reduced at the I/O card by time domain folding or time domain integration. The data is then written to the DAS.

For the ID mode one of the NRAO ASICs in each FFT pipeline is used as a complex multiplier in order to obtain the products RR* , LL* , RL* and LR* . This can be achieved by putting the ASIC in radix 2 mode and clocking the FFT pipeline at 32 MHz, with input data coming in at only 16 MHz. While one data stream comes from the regular ASIC input port, the other comes via the TRIG port of the ASIC. We will use stage 2 of the ASIC pipeline for this purpose. The rest of the ASICS in the pipeline are put in bypass mode. The 0th stage and 4th

stage external addresses are set respectively to compensate for the scrambling from 0th stage to 2nd stage and to compensate for the scrambling from the 2nd stage to the 4th stage, ensuring proper data sequence at the multiplication stage and at the pipeline output stage. In one FFT card, R* is fed in place of the second stage TRIGS, while in the other FFT card, L* is fed in place of the second stage TRIGS. This switching is achieved in the first DCC. The channel ordered products are then send to the second DCC (only for format conversion) and thence to the DFC. This can be used to collapse upto 4 adjacent channels for each product, or can be in bypass mode where the data goes through unaltered. This data, at 16 MHz or less (when packed across 32 bit wide DSP bus), is read in appropriate sized chunks by the different DSP cards (in sequential order) where it is post processed in the desired manner. The I/O DSP node then reads the results from these compute DSP nodes and to writes the data out to the DAS.

Projected time scales & manpower requirements

The detailed card level design for the cards in the DSP bin (the DSP array and peripheral cards, including backplane) has been done. The PCB layouts for these cards are almost ready and the orders for the PCBs will go out within the next 30 days or so. The detailed card level design for the other cards (FFT system, Filter card and peripheral cards) is also done and PCB layouts for some of these are also complete. For the FFT system we will use the GMRT correlator cards with the appropriate "strapping" to bypass the 4/6 bit input mode and the Fringe ROM. PCB orders for the rest of the cards will go out by end of December or so. Subject to the manpower availability outlined below, the prototype version should be ready in the lab by April-May and available for site testing by June-July.

The manpower requirement is estimated to be about 1 full time engineer till December and about 2 full time engineers from then to completion of the prototype. The persons identified at present for this are : Mr. S.M. Izhak (half time till December and full time thereafter) and Mr. G. Markandeyalu (half time till December and about 50-70% time thereafter). A major part of the work will be included as the M.Tech. project for Mr. S. Izhak, which is to be for two semesters, starting from January '95. In addition to the above manpower, we will need one full time lab assistant from December '94 / January '95 onwards. Help from one more person in the category of staff/post-doc/astronomer will also be useful.

Hardware Details

The hardware can be clearly demarcated into two sets - the data conditioning, the inverse FFT/Stokes parameter calculation & the filtering; and the I/O

node, the DSP array & the peripheral interface. The hardware for the first set required to handle two polarizations and one sideband will be placed in one bin (the SOB - Synchronous Operation Bin). The latter set does the coherent/incoherent dedispersion and some post processing. As this set is basically an array of DSP chips, which are programmable, it is a highly flexible and powerful computational platform; and could be used for various other signal processing applications as well. The hardware for this set required to cater to one sideband will be placed in one bin (the DAB - DSP Array Bin). The data signal from the SOB is send to the DAB in the form of ECL signals. A part of the DSP bus is connected to the SOB from DAB (via TTL differential), for control and monitor.

The details of the hardware chain is clearly shown in figure 1. The card wise details are as follows.

Synchronous Operation Bin - SOB

Frequency Domain Data Conditioning Card (DCC-FD)

The data coming from the GAC has (1+8, 1+8) sign magnitude format, which has to be converted to the (4,4,4) format used by the FFT pipeline for CD mode and (5,5,0) format for ID mode. In addition, for the ID mode, the input to the second pipeline of each FFT card has to be switched to the other polarisation signal and the 2nd stage TRIGS have to be replaced by the complex conjugate and delayed version of the R or L polarisation. All these features are implemented on this card with the appropriate combination of MUXes and FIFOs. The rates at each input and output on this card are 16 Msamples/sec.

The TTL data lines coming from the GAC first go to three 64k x 4 lookup RAMs which do the format conversion mentioned above. Only the magnitude needs to be reformatted (8+8 = 16 lines; hence 64k address space). The real and imaginary input sign bits are passed directly onto the respective output bits. The lookup RAM is loaded from the DSP bus. In the test mode, a 16 bit counter addresses these RAMs to generate any test pattern loaded into it by the DSP bus.

GMRT FFT Controller (GFC)

A GFC is required to control the GMRT FFT Pipeline, GFPs. One GFC will be used to control two GFPs corresponding to two polarizations of a sideband. So there will be two such cards for catering two sidebands. This will be the same standard control card that is being designed for GMRT, however the twiddle factors and the address ordering will be changed appropriately.

GMRT FFT Pipeline (GFP)

To do a 256 point inverse FFT requires 4 stages of Radix-4 . Hence one of the 5 stages will be in bypass mode. GFP essentially are the same cards that are being used in the GMRT correlator.

0.0.1 Domain Data Conditioning Card (DCC-TD)

The DCC-TD is basically the same card DCC-FD. The input data lines connected appropriately so that (7,7,4) 18 bit data goes to a look up table which converts into (1+8,1+8) format. The only difference between the DCC-FD and the DCC-TD, is that the stage 2 TRIG input (T2) will not be used at all and the complex conjugation and FIFO will be deactivated. Here again, as in DCC-FD, a test signal can be injected in place of the real data.

Digital Filter Card (DFC)

The Digital Filter Card basically has two digital FIR filter chips, namely HSP 43168 (Harris Semiconductors). The HSP43168 has two FIR cells in it, each with 4 taps (MACs). The two FIRs in a chip can be used independently or could be cascaded to obtain double the number of taps - 8 taps (filter coefficients). While filtering real time series the filter coefficients are usually symmetrical. For such cases, a preaddition facility (before MAC), helps in doubling the effective number of taps on one chip (16 taps). The number of taps increases again when the signal is decimated. Thus when 1 MHz is filtered from 16 MHz band, one could obatin 256 (=16*16) taps on one chip. The control signal for each FIR chip is derived from a EPLD, EPM 5032.

The card is designed to retain all the flexibilities and options that the chip provides. Thus with the two FIR chips, there are atleast 3 options of filtering available. The first one is to send a real time series to one chip and the result to the next. The second option is to send a real time series to the first chip and to toggle the sign bit of every alternate sample coming out from this, thus effectively multiplying the signal by $f_s/4$ (one fourth of sampling frequency) and then a complex filtering in the next stage to obtain complex time series corresponding to quadratue modulated sampling of the subband. The third option is to send a complex time series to each of the FIR chips and perform a complex filtering of the time series (the real part in one chip and the imaginary in the other). For most of our applications, we will use the third mode.

The control and status registers connected to the DSP bus will be used to configure and check the card. The coefficients will be downloaded by the I/O node through the DSP bus. The output from this card comes out in the form of ECL signals. Though in the CD mode, the output data rate will not exceed about 4 MHz, for the ID mode application it will be possible to send the data unaffected through the DFC at 16 MHz rate (bypass mode).

DSP Array Bin - DAB

The DSP Array Bin as mentioned earlier consists of the I/O DSP node, the comput DSP nodes, the Input Interface Card, the Peripheral Support Card and the Format Conversion card. There is provision to plug in extra DSP boards to augment the processing capablility and memory capacity.

Format Conversion Card

This card is a simple card which converts the ECL input data bus to TTL. In addition, it converts part of the DSP bus to TTL differential.

Input Interface Card (IIC)

The input interface card accepts TTL data input along with a data strobe and some extra control information (like start). The data can be send to four 8-bit FIFOs in any sequence. Thus the data can be spread out to occupy 32-bit wide bus. This will help in carry out much faster operations and will be very useful in the ID mode. The flow of data into the four FIFOs are completely controlled by an EPLD, which can be set into the appropriate mode by loading the appropriate control bits in the control word. The card can be set up and checked using the control and status port on it. The FIFO locations are decoded as a port address on the DSP bus.

I/O Node

There is no difference between the I/O DSP card and any other DSP card in the array. The same PCBs will be used for both the jobs. However the I/O node which is the master node is distinguished from the slave nodes by its onboard configuration. The I/O node will be the master of the backplane DSP bus and most often will initiate the transfer of data on the bus. The arrival of the input at the IIC is intimated to the master card by the IRQ/0 interrupt line. For interprocessor communication, any communication from master to slave will be initiated by raising the IRQ/1 interrupt and then sending the address of the slave using the four FLAG lines. Similarly any communication from the slave to master is initiated, by the slave. by raising the IRQ/2 interrupt and then sending the slave address on the FLAG lines. Apart from this, message passing can be done from the master to the slave and from slave to the master through the memory mapped buffered memory. This buffered memory present on each card, has two ports - one connected to the backplane DSP bus and the other to the DSP on the card. These are single ported memory with some logic for arbitration to rule out any clash. The buffered memory on each card maps onto unique memory segments of the backplane bus. Thus any location on the buffered memory of any of the card can be accessed uniquely. In the event of a clash appropriate signals are send to the processors involved. The backplane in

the most general case is controlled by the I/O node. In which case it is basically be an extension of the data memory bus of the DSP on the I/O node with some additional control signals to make arbitration easy.

Two banks of program memory and two banks of data memory are available on board, apart from the bufferd memory. All these memories are in the form of 256k capcaity ZIP sockets in which only 64k will be populated initially.

DSP Node

The DSP nodes essentially will serve the purpose of number crunching machines. So the load of I/O on these nodes are kept minimal. The I/O node will time the shuttling of the data in such a fashion that the a new block of data is available to the DSP node whenever it is through with the earlier block. Subsequently the I/O node will retrieve the result from the DSP node. The DSP nodes will work on the blocks in a staggered fashion so that all the nodes do not require input data to be availbable at the same time. The DSP nodes also have two program memory banks and two data memory banks, apart from the buffered memory. All of them are in the form of 256k capacity ZIP sockets. Initialle only 64k will be populated in each bank.

Peripheral Support Card (PSC)

The peripheral support card has two major jobs to perform. The first one is of booting all the DSPs in the DAB. Initially a boot kernel is loaded into the DSP through the TAP (Test Access Port). Then each of the processors will sequentially boot through the centronics port connected to say, a PC. The second job of the PSC is to dump the result. The data is send out in TTL differential for with a strobe. To liberate the I/O node from the task of monitoring the slow device at the other end of the link, it is buffered. The data is dumped into a set of FIFOs whose status can be monitored by the I/O node. The data is then clocked out by a clock signal whose frequency can be programmed by appropriate bits in the control register. Apart from this, there is an optional RS 232 link availbable. This of course will involve a writing a RS232 software driver for DSP. It is possible that it will be available on the public domain by then.

Pulsar DSP Platform – Overall Block Diagram

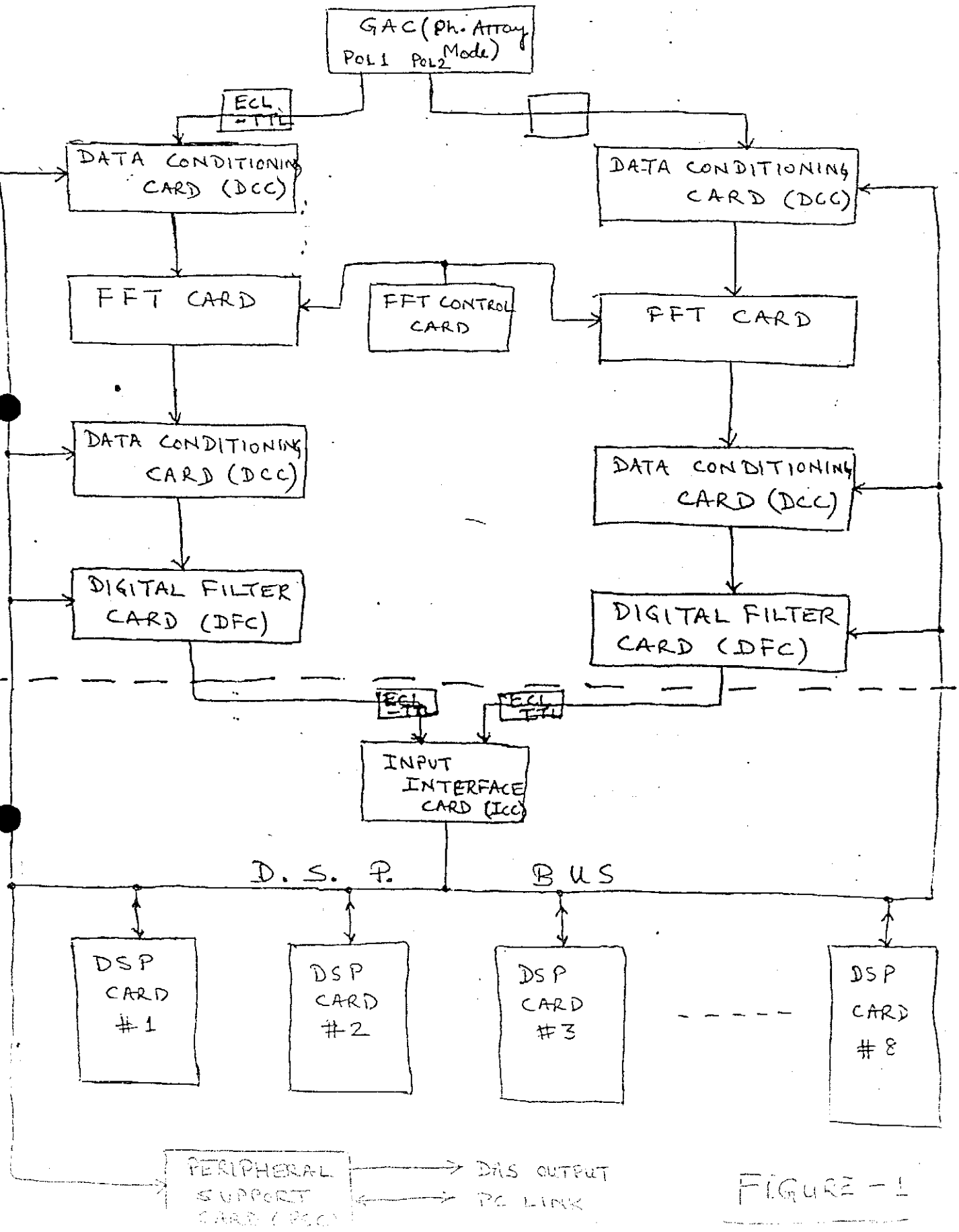


FIGURE – 1

FFT ~~CARD~~ CONFIGURATION

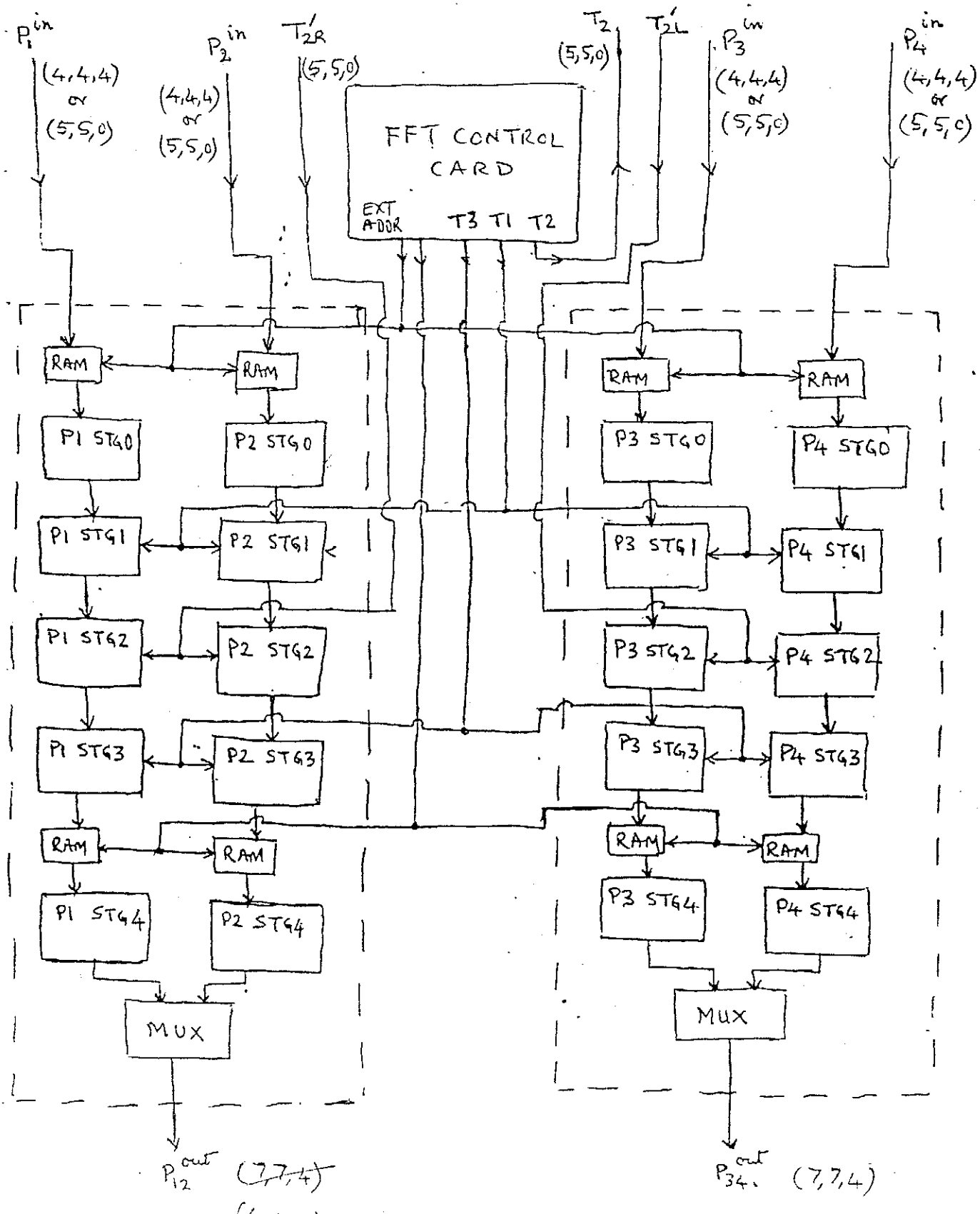


FIGURE - 2

DATA CONDITIONING CARD (DCC)

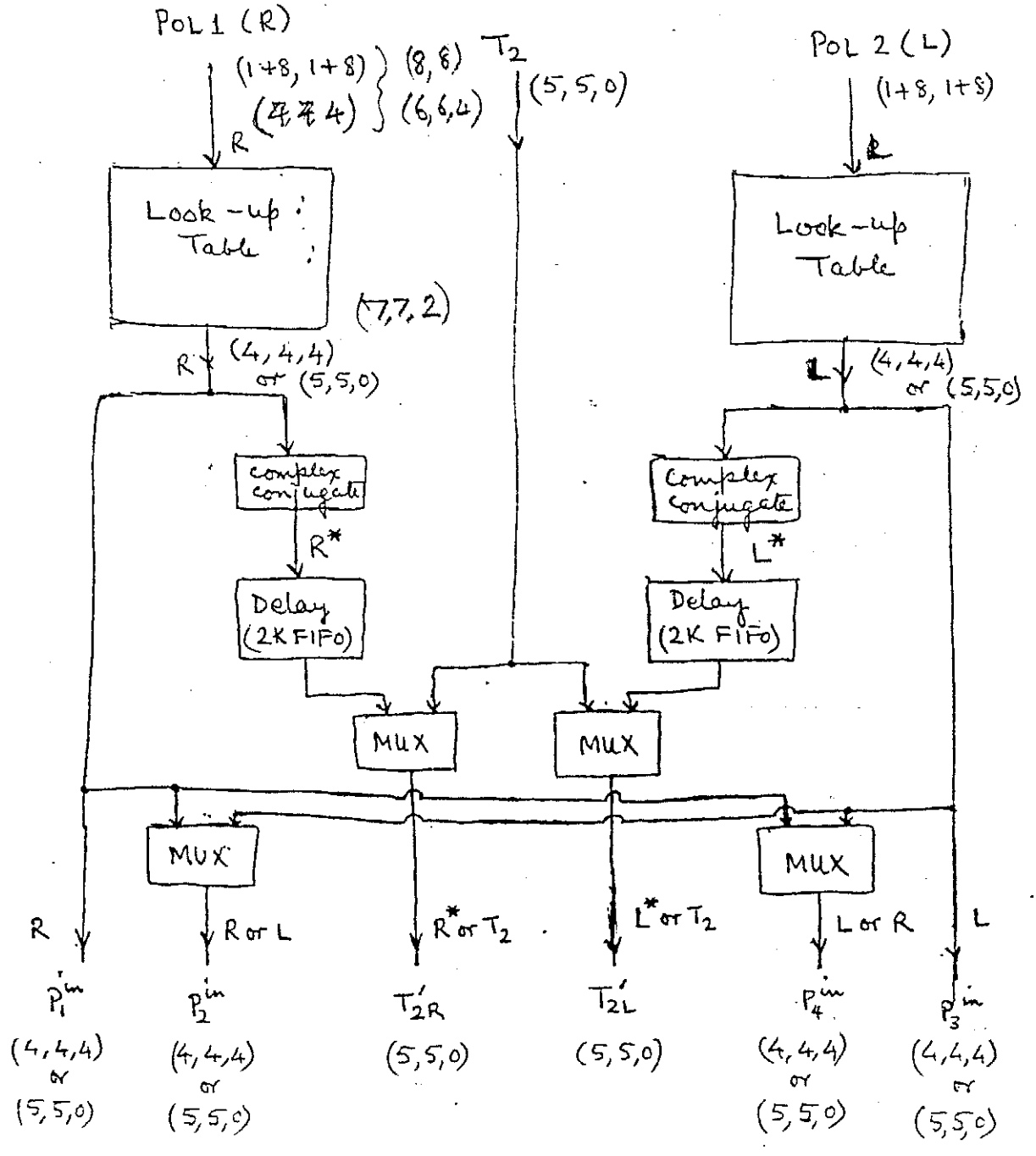
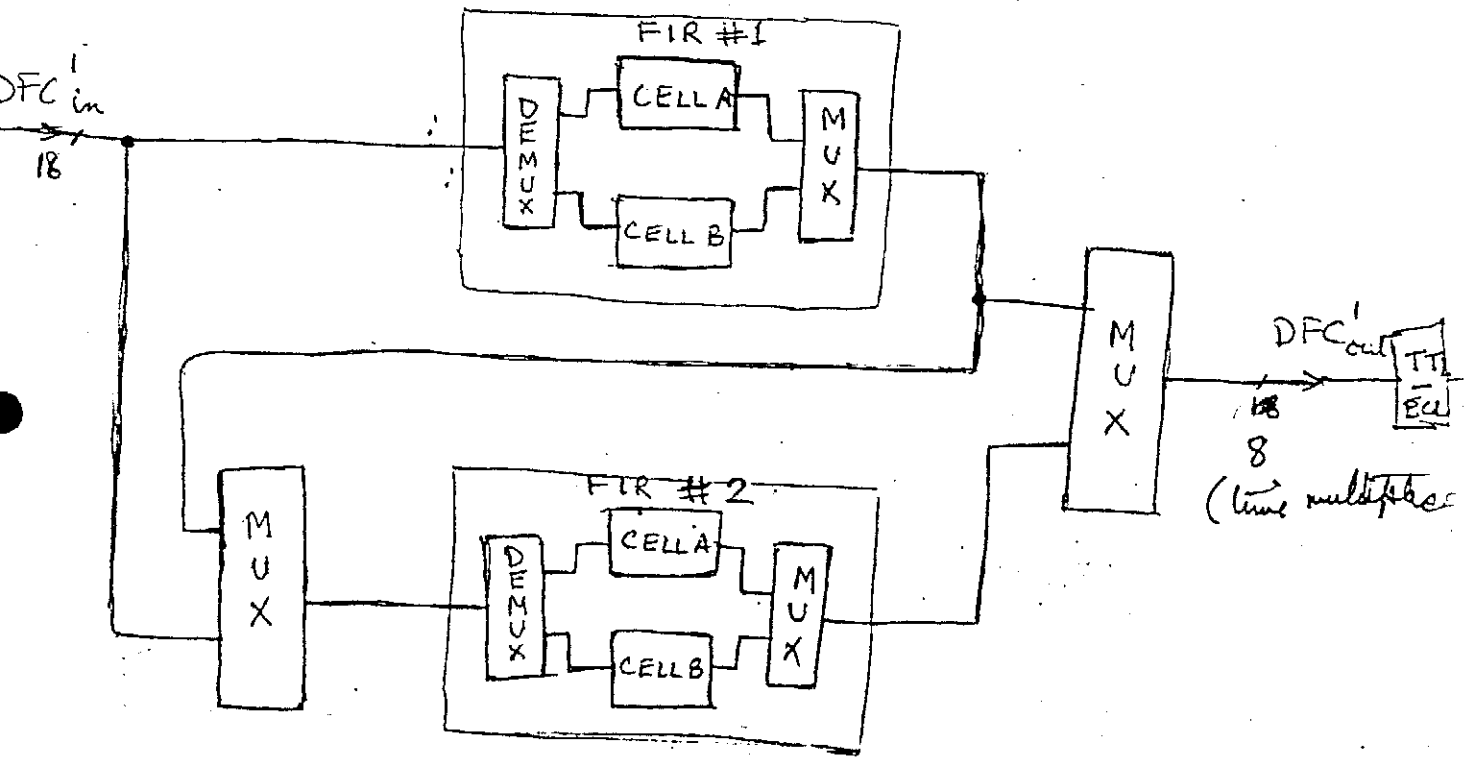


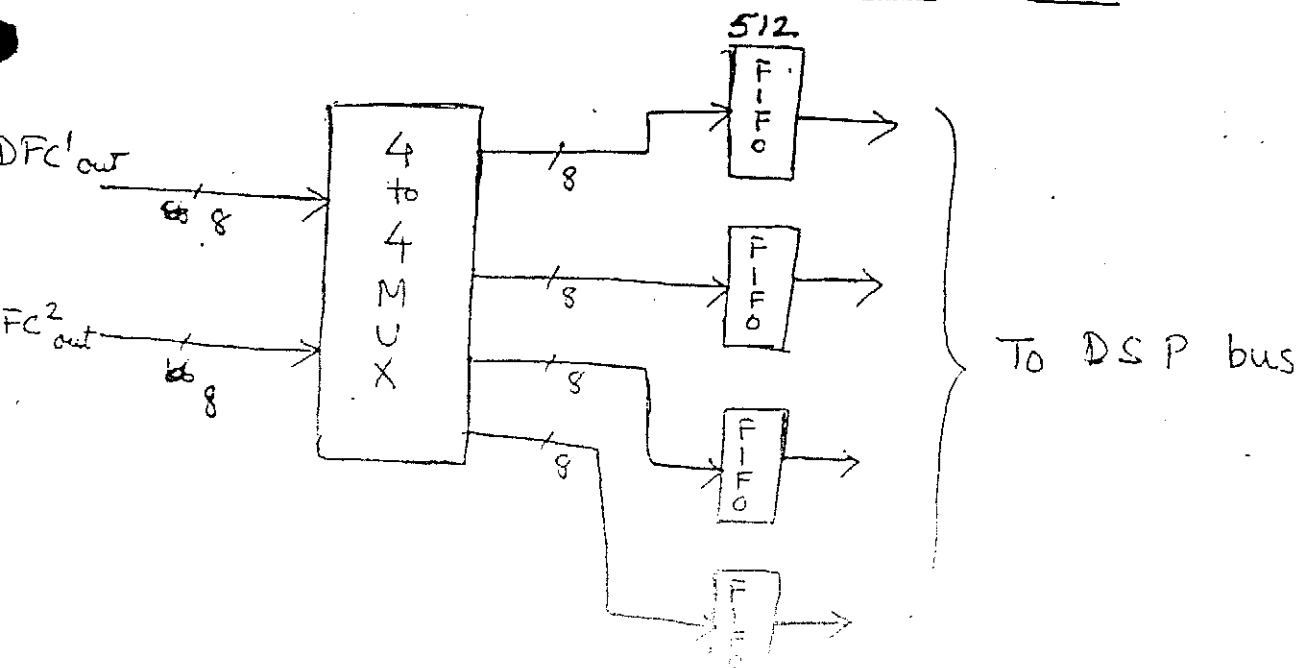
Figure 3

DIGITAL FILTER CARD (DFC)

Figure 4



INPUT INTERFACE CARD (IIC)



ADSP 21020 CARD

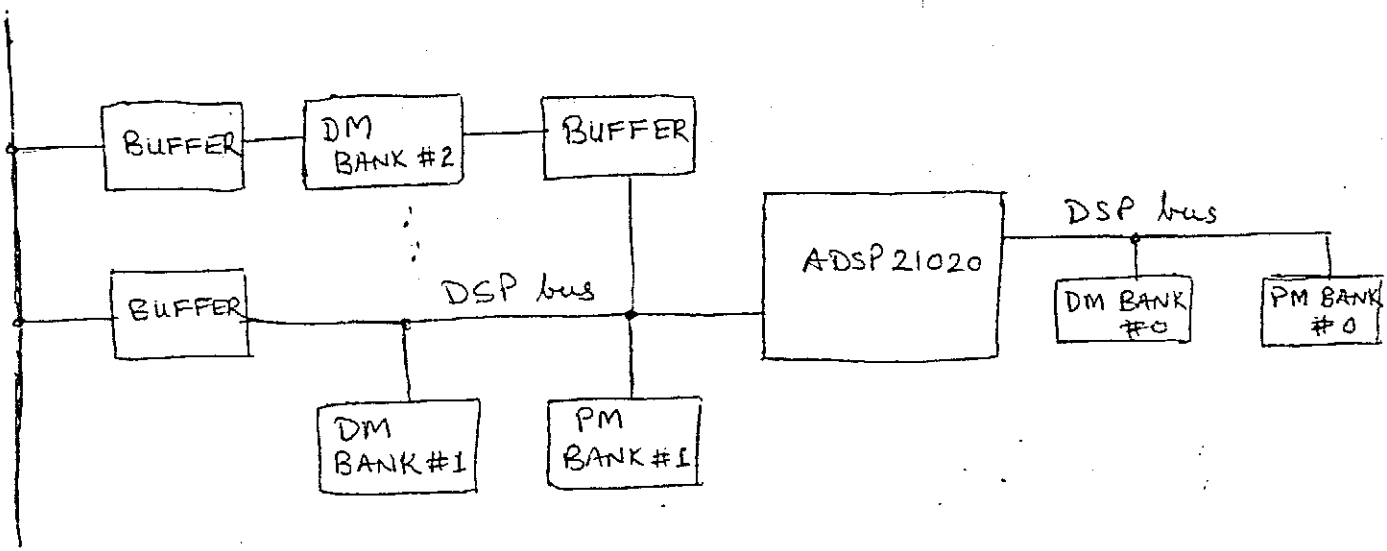


Figure 5