THE GMRT CORRELATOR CLOCK DESIGN DETAILS

SULEKHA DESWANDIKAR

ABSTRACT : The GMRT correlator system requires 32 MHz and 32.25 MHz clock signals of very high stability for the sampling of the baseband signal having a passband of 16 MHz. This report describes the design details of the clock system based on PHASE LOCKED LOOP SYNTHESIS - which provides high phase stability and accuracy catering to the needs of the GMRT correlator system.

DESIGN DETAILS:

A 5 MHz reference signal is taken from a frequency standard. The accuracy of a generated frequency depends upon the reference element selected.

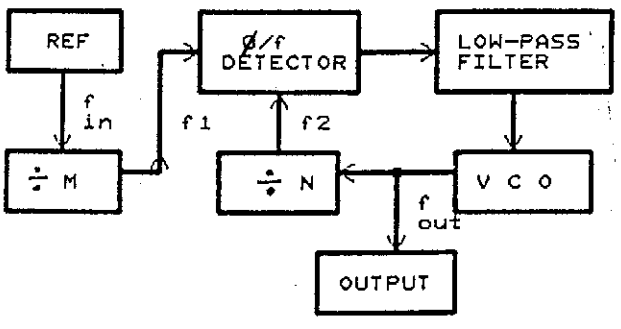
A COMPARATIVE STUDY OF THE VARIOUS FREQUENCY STANDARDS AVAILABLE

FREQUENCY STANDARD	CRYSTAL	RUBIDIUM	CESIUM BEAM
MODEL No	HP 105B	HP 5065A	HP 5061B
ACCURACY	1×10^{-11}	7×10^{-11}	3×10^{-12}
STABILITY			
a> SHORT TERM	5×10^{-5}	5×10^{-12}	5×10^{-11}
b> LONG TERM	5×10^{-10}/day	1×10^{-11}/mth	1×10^{-12}/day
COST	---	$ 29,000	$ 37,000

DESCRIPTION OF THE BLOCK DIAGRAM

Fig 1 shows the block diagram of the entire system. Using low power schottkey TTL counter the 5 MHz reference is down converted to 1 MHz TTL level. This is converted to ECL 1 MHz which branches out to the two PLL's for the synthesis of 32 MHz and 32.25 MHz frequencies

FREQUENCY SYNTHESIS USING PHASE LOCKED LOOP TECHNIQUES



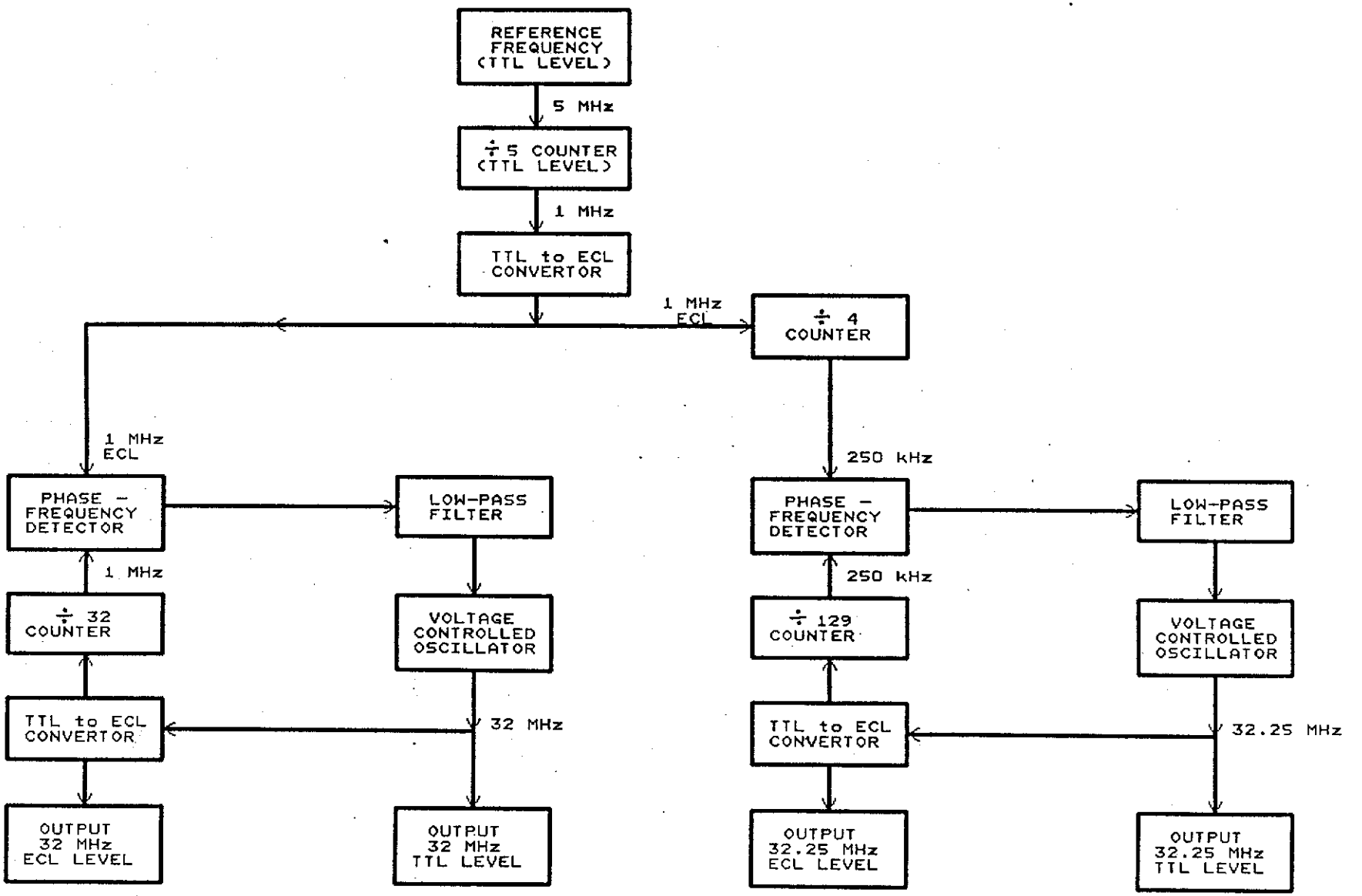
$f1 = f_{ref}/M$

$f2 = f_{out}/N$

Under lock conditions, f1 = f2

$f_{ref}/M = f_{out}/N$

$f_{out} = (N/M) * f_{ref}$



GMRT CORRELATOR CLOCK - BLOCK DIAGRAM

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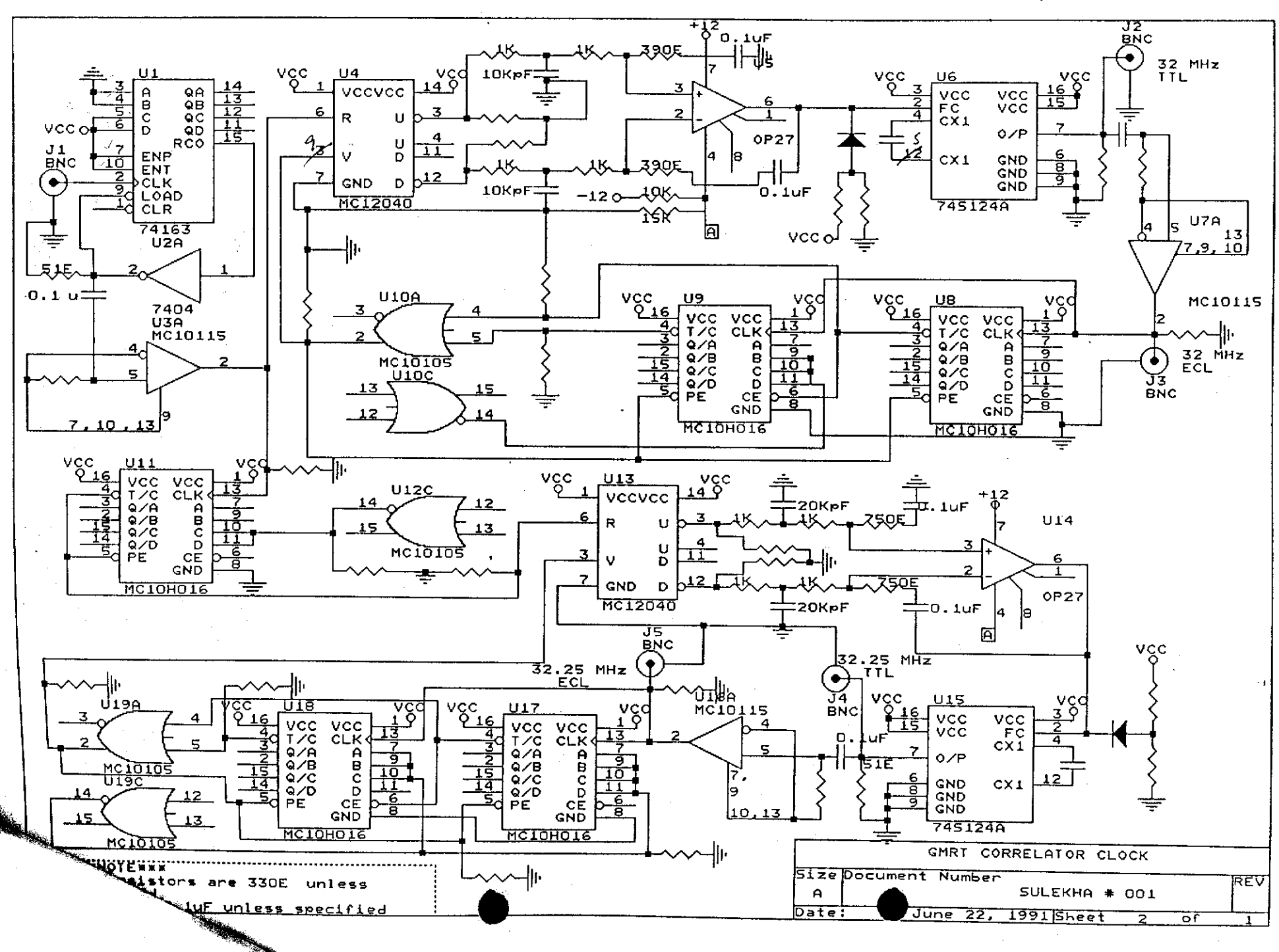

NOTE:
Resistors are 330E unless
.1uF unless specified

GMRT CORRELATOR CLOCK

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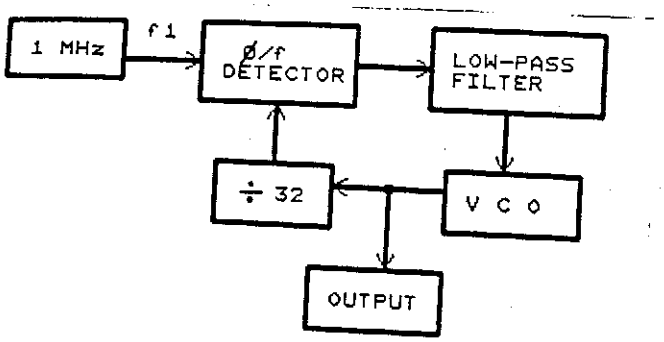
Before the design of any PHASE LOCKED LOOP SYSTEM one has to analyse some critical parameters which determine the performance of the system and at the same time speak for the stability of the system. The purpose of selecting a PLL for frequency synthesis is to go in for **low phase noise, highly reliable and phase synchronisation at the two clock outputs.** Phase locked loop is basically a phase locked servo system. Stability parameter analysis like gain margin and phase margin is very essential for this kind of system. One of the vital parameters in the design of the phase locked loops is the LOOP BAND WIDTH, which in effect determines the capture range, the LOOP LOCK-IN TIME, which decides how fast the loop can go into lock if for some reason or the other it happens to get unlock. The other important one is the **PHASE NOISE PERFORMANCE.** Any practical signal source suffers from random phase jitter and that in effect shows up in the spectral impurity of the signal source. Our requirement of the clock demands high spectral purity. So, a good close-in phase noise performance is required. Thus the LOOP BAND WIDTH becomes critical for low phase noise performance. A narrow loop band width would improve the phase noise performance but it would certainly reduce the capture range of the loop. However a large loop bandwidth would reduce the lock-in time as well as improve upon the probability of getting the loop to lock if unlock, but this would mean a sacrifice at the noise performance end. Thus one has to make a compromise over the loop bandwidth, lock-in time and phase noise performance.

Secondly, the phase noise performance of the clock within the loop bandwidth is close to the reference signal (gets degraded by n^2 where n => multiplication factor). Outside the loop bandwidth - it follows the VCO phase noise profile.

GENERATION OF 32 MHz: (Fig 2)

The 1 MHz is fed to the ECL phase frequency detector as the reference input. The voltage controlled oscillator is designed to give a free running frequency of around 29 MHz as it should not be much less than the desired output frequency, in order to have a low lock-in time and high capture range. The error voltage generated by the low pass filter controls the output frequency of the VCO and maintains it at 32 MHz. This 32 MHz is then fed to a ÷ 32 synchronous counter and the 1 MHz output signal of the counter is given to the phase frequency detector as a feed back. Phase error information is contained in the duty cycle of the output. i.e. the ratio of the output pulse width to the total period. By integrating the outputs of the detector, a voltage is generated to control the frequency of the voltage - controlled oscillator. Any change in frequency of the VCO is in the direction so as to minimise the difference in the phase of the two signals at the phase frequency detector, thereby leading to a stable output. The outputs are available at the VCO in the TTL level as well as in the ECL level.

Thus,



$f1 = f_{in}$

$f2 = f_{out}/32$

under lock conditions,

$f1 = f2$

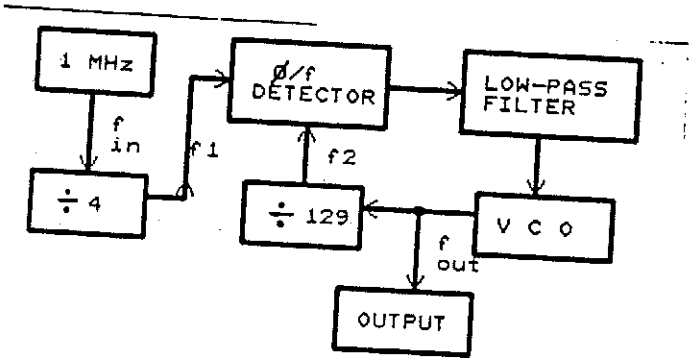
$f_{out} = 32 * f_{in}$

for $f_{in} = 1$ MHz

$f_{out} = 32$ MHz.

GENERATION OF 32.25 MHz (Fig 3)

The 1 MHz ECL signal which goes to the 32 MHz synthesiser is now divided by 4 so as to get a 250 kHz frequency which is fed to the phase frequency detector as the reference input. The voltage controlled oscillator is designed to give a free running frequency of around 29 MHz. The voltage generated by the low pass filter controls the output frequency and maintains it at a fixed value of 32.25 MHz. This frequency is then divided by 129 so as to give 250 kHz at the counter chain outputs, where from it is fed to the phase frequency detector as its variable input.
Thus,



$f1 = f_{in}/4$

$f2 = f_{out}/129$

under lock conditions,

$f1 = f2$

$f_{out} = 129/4 * f_{in}$

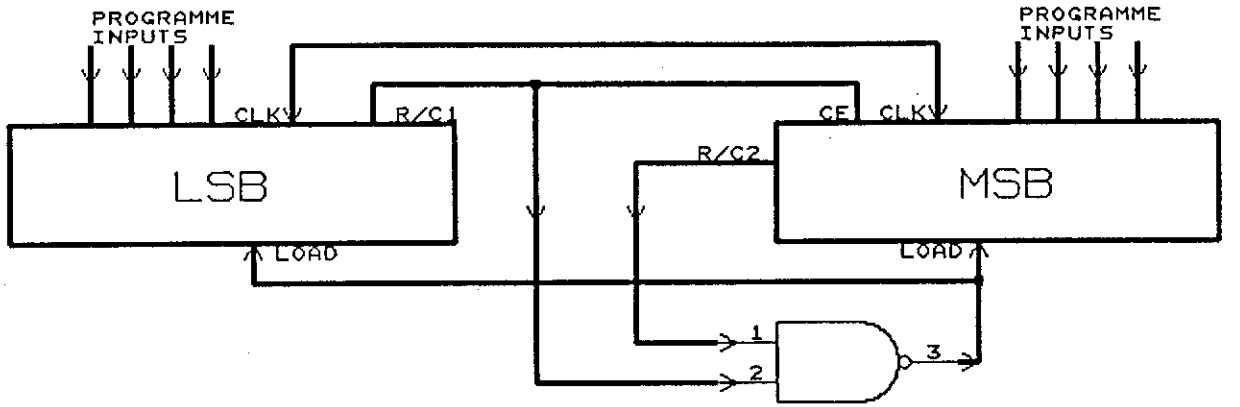
for $f_{in} = 1$ MHz

$f_{out} = 32.25$ MHz.

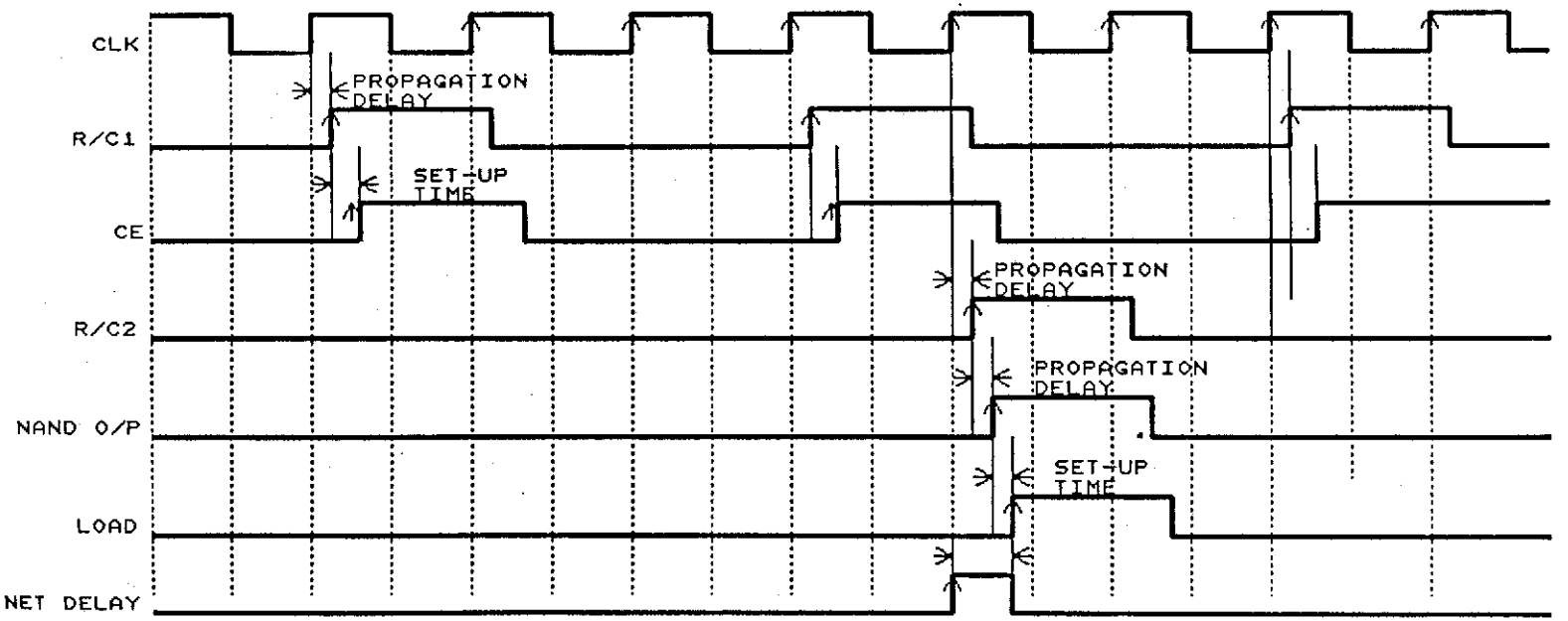
THE NEED FOR SYNCHRONOUS COUNTERS:

It is clear from the data sheets of the TTL , TTL-LS, TTL-ALS, or HCT, that the counters have a finite propagation delay, which cannot be avoided. If counters are to be cascaded using clocks of different frequencies then there is a high probability of difference in the phases at their outputs. This phase ambiguity can neither be tracked nor can it be accurately estimated. Thus the only way to have a minimise this phase ambiguity is to go for SYNCHRONOUS COUNTING. In this case the entire counter chain receives the same clock signal and cascading

TWO COUNTER CASCADE



TIMING DIAGRAM



COUNTER LOOP DELAY ANALYSIS		
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is done in the following manner. The terminal count output of the previous counter is fed to the count enable input of the next counter, thus the counting begins at the same clock pulse but for the time only for which the chip enable is active. This prevents accumulation of delays due to more number of counters and overall delay gets restricted to only one counter delay.

TIMING ANAYLSIS (Fig 4)

A very crucial factor in case of cascading counters is the need for a rigorous TIMING ANALYSIS for the guarenteed operation of the counters in the desired fashion. When counting is done in the method described above the propagation time for the entire chain is reduced to only that of the last counter. However even under this condition the counter chain will **FAIL** to count the programmed input number if the **TOTAL LOOP DELAY IS GREATER THAN ONE CLOCK PERIOD AND THE COUNTER WILL MISS CLOCK PULSES.**. It will be clear from the timing diagram below how the total loop delay plays a vital role in such cascaded counters, else the counter is **headed towards an error in counting.** Designing of this type is most critical and worst case tolerances **MUST** be used if reproducibility and reliability of the design under temperature and voltage extremes is NOT to be compromised. (ref appendix 1)

COMPARATIVE STUDY OF THE VARIOUS INTERGRATED CHIPS

SERIES	74LS	74HCT	74ALS	74AS	74F	ECL
a) t_{pd} clk-RCO	35nS	20nS	20nS	16nS	15nS	2nS
b) set up time	14nS	14nS	13nS	9nS	9.5nS	2nS
c) max.clk freq in MHz	30	28	30	75	90	200
d) NAND delay	4nS	4nS	4nS	4nS	2.5nS	2nS
e) total loop delay	53nS	38nS	37nS	29nS	27nS	6nS
e) max freq for cascading in MHz	< 18	< 26	< 27	< 34	< 37	170 (min)

CONVERSION FROM TTL LEVEL TO ECL

WHY ECL ?

1> From the above discussion it is clear that system designers must critically analyse the timing information from the data sheets. The total loop delay in case of counters designed using TTL -LS, HCT, ALS for the required clock frequency of 32 MHz and 32.25 MHz is greater than $1/f_{clk}$, and thus the scheme fails to

meet the required division specifications. F series and AS series could not be used, as it is clear from the previous table that they meet the requirement critically.

2> As the clock frequency is increased more than 28 MHz for ALS, HCT IC's an extra glitch appears at the terminal count pin due to the loop delay problem mentioned above and this is harmful for cascaded counter chains. (refer appendix for details)

3> Total loop delay in case of ECL counters does not exceed 7 nS.

4> The ECL chips used for this design were readily available.

5> No glitch or any other impurity is found in the output even after cascading the counters and thus can be safely used for division by numbers much larger than 16.

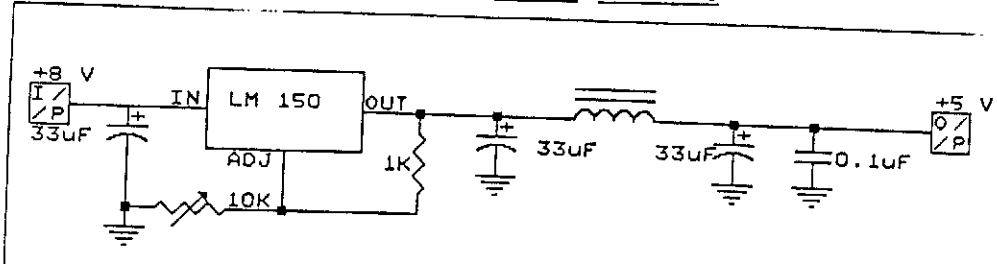
6> The phase frequency detector also governs the phase noise performance. MC 12040 is one of the best phase frequency detectors available in the market at present, with high reference level suppression capability.

7> The circuit was wired on a general purpose board. However the performance would improve if a PCB is made. - BUT - one has to take care in the layout as it is the most critical. I presume that the estimated size of the PCB for entire system should not exceed 4" X 6".

POWER SUPPLY REQUIREMENTS FOR ECL :

Most designers have an aversion towards mixing of ECL and TTL in the same design solely because of the odd power supply requirements of the ECL's. The data sheets for ECL's suggest that to use -5.2 V as V_{EE} supply. More over since, ECL has high input impedence and low output impedence; matched load and driving current is very critical. So a separate supply of -2 V is required to terminate the outputs. BUT in this design a unique approach was taken and the above mentioned drawbacks of ECL's were totally eliminated. A single +5 V power supply was used for both TTL's and ECL's with the proper choice of terminating resistances without compromising the performance of the ECL.

SYSTEM POWER SUPPLY



32 MHz LOOP CHARACTERISTICS

1>	LOOP BAND - WIDTH	9.7 kHz
2>	PHASE MARGIN	66.51
3>	LOCK - IN TIME	40 nS
4>	PHASE NOISE MEASUREMENT :	
	REFERENCE	WAVETEK 178 SYNTHESISED FUNCTION GENERATOR
	SPECTRUM ANALYSER	TEKTRONIX 2710
	REFERENCE FREQUENCY	1 MHz
	OUTPUT FREQUENCY	32 MHz
	RESOLUTION BAND WIDTH	300 Hz
	SPAN	1 kHz
	PHASE NOISE	-40 dBc/Hz at 1 kHz offset

32.25 MHz LOOP CHARACTERISTICS

1>	LOOP BAND - WIDTH	4.695 kHz
2>	PHASE MARGIN	65.678
3>	LOCK - IN TIME	20 nS
4>	PHASE NOISE MEASUREMENT :	
	REFERENCE	WAVETEK 178 SYNTHESISED FUNCTION GENERATOR
	SPECTRUM ANALYSER	TEKTRONIX 2710
	REFERENCE FREQUENCY	1 MHz
	OUTPUT FREQUENCY	32.25 MHz
	RESOLUTION BAND WIDTH	300 Hz
	SPAN	1 kHz
	PHASE NOISE	-39 dBc/Hz at 1 kHz offset

The outputs are available at at both ECL and TTL levels.

TOTAL POWER CONSUMPTION ≈ 7 W.

COMPONENT LIST

	PART No	DESCRIPTION		QUANTITY
1>	74LS163	Progammable 4-bit counnter	(TTL)	1
2>	MC10H016	MECL High speed, progammable 4-bit binary counter	(ECL)	5
3>	MC10105	Triple 2-3-2 input OR/NOR gate	(ECL)	3
4>	MC12040	Phase-Frequency detector	(ECL)	2
5>	OP-27	Low-noise precision op-amp		2
6>	MC74S124	Dual Voltage-Controlled-Oscillator	(TTL)	2
7>	MC10115	Quad line receiver	(ECL)	2
8>	74LS00	Quad dual input nand gate	(TTL)	1

CONCLUSIONS

The performance of the system was found to be satisfactory when tested with WAVETEK 178 SYNTHESISED FUNCTION GENERATOR as reference input. The performance will be improved if the following measures are taken.

1> Instead of a general purpose PCB, a proper layout and PCB should be made.

2> Considerable precaution has to be taken in the layout for tracks wherein different frequencies are generated in order to prevent any cross-talk or modulation.

3> An in built power supply with sufficient isolation would prevent leakage of the line frequency in the system, which in effect will improve the phase - noise performance

4> To improve upon the RMS phase noise performance, a transistorised Voltage-Controlled-Crystal-Oscillator at 32 MHz and 32.25 MHz could be used instead of a simple Voltage-Controlled-Oscillator.

5> Software Analysis could be done to optimise the loop parameters, especially the critical ones like LOOP BAND WIDTH, and PHASE MARGIN.

6> Loop band width can be further reduced in order to reduce the lock - in time.

REFERENCES

1> PHASE LOCKED LOOP TECHNIQUES .....F. M. GARDENER.

2> PHASE LOCKED LOOPS .....BEST.

3> HEWLETT PACKARD APPLICATION NOTE 52-2 (Timing and Frequency calibration).

4> HEWLETT PACKARD APPLICATION NOTE 200-2 (Fundamentals of Quartz Oscillators).

5> HP 5061B Cesium Beam Frequency Standard .....Technical Data.

6> MECL DATA BOOK

7> TTL/ALS/AS DATA BOOK

8> HIGH SPEED CMOS DATA BOOK

9> TTL SCHOTTKEY DATA BOOK

10> CORRELATOR CLOCK - SOME COMMENTS: Goutam Chattopadhay (internal report).