TESTING PROCEDURE FOR DPC/DELAY CARDS

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1 Introduction

Following is the description of procedure adapted for validating the DPC and DELAY cards . Testing procedure for Some sections of the DPC and DELAY cards are common and hence to test those sections the procedure defined is in the beginning of this report. After that this report is divided in to two broad sections viz. DPC testing and DELAY testing. Here are the areas which require a general procedure for both the cards. Leaving aside general information the same document can be used for debugging these cards in the case of field failures .

Note : For mass production the cards should be tested in the same batches as the manufacturing lot batches and care should be taken to use all ICs which are from the same vendor on one manufacturing lot. This will heavily reduce individual card tweeking for timing mismatches. (Although timing mismatch is a remote remote possibility).

2 General testing for both the cards.

1. Visual Inspection and testing of the PCB before populating and after populating.
2. Power Section
3. Clock Section
4. Input Section

3 Visual Inspection and testing of PCB before populating. and after populating.

1. As the saying goes prevention is better then cure ,We should inspect each PCB visually for shorts and opens while PCB manufacturing. Which will save a lot of debugging time .
2. The PTH's are generally (if manufacturing was not up to the mark; worst case condition!!) open due to the discontineuty between the pad and the barrel which should also be randomly checked say in 10generally taken care of) .
3. Each component should be checked for proper functioning before it is placed on PCB. Those IC's which can't be tested on IC tester should be provided with testjigs to test them. Even decoupling capacitors should be batch tested (i.e. say 20selected) on LCR meter before being put on the card.
4. After population of the cards they should be checked for any dry soldering .

4 General Information about Schematics and conventions followed in them.

Both The cards and schematic follow these conventions:

1. To facilitate locating a component on PCB both the cards have component references arranged such that they start from right (once you are holding the card with component side facing you.) and increment in top to bottom fashion and once reaches bottom ,it continues from bottom to top moving towards left.Where as in the schematic they are placed with the group of component which act as a sub group in the schematic so references on schematic are irregular.
2. On the schematic all the active low signals are defined by signal name suffixed by a "-"
3. Most of the connecting names used on the sheets are signal names without any vowels (unless two signals without vowels turn out to be same in that case simple insertion of one vowel is used.). Many times if a signal name consist of more then one word the first two consonants of first word and then first one ,two or three (for the sake of more clarity) consonant of other is used as signal name e.g. even output data is decoded as "evoutd".
4. The buses used in the sheets have least significant bit named with suffix "0" .incoming data to ROM's and RAM's uses "in" in the signal name and out going data uses "out" in the signal name.e.g even output data has "ev-out-d" ("-" are not there)
5. Every signal which is buffered has a suffix "b" before the signal name e.g. rst when buffered is called "brst"

5 Power Section testing.

While testing the card for the first time or debugging it for on site failours this thing one should check first i.e. if the power section works and the card has some problem or the card does not work because there is no power to the card. This is easy to check as both the cards have been provided with LED's to indicate the power status. Red LED indicates the VCC (+5 V) and green LED indicates (-5 V).

On both the cards there is a fuse provided of rating mentioned in the part list as well as on silkscreen of PCB. In no case fuse should be put which is of higher current rating by more then 20specified value. (lower current rating will not work any way !). After the fuse there is a current booster capacitor. Both the +ve and -ve power supplies should be within the range 4.5 to 5.5 which is about 10

If the power (any of them) has dropped by a significant amount, it might be possible that some IC has gone bad but not fully blown up or some decoupling capacitor has become leaky. So it is not drawing enough current to blow the fuse but the LEDs will glow little faintly. The IC can be detected by sensing its temperature (which will be higher)

6 Clock Section testing

1. This section is most important for the proper functioning of the card. There should be proper relationships defined below, between different clocks so as the data flow is not obstructed any where.Both

the cards have clock coming from the backplane as ECL differential signal. The DELAY card has the clock coming in the card which is not the same as DPCcard but with each *FFTINT* pulse both are phase aligned .So at the rising edge of FFTINT both DPC and DELAY card should have their respective clocks going high simultaneously (simultaneous with a maximum error of 4 ns.

2. The clock on DPC card is buffered and sent to samplers for latching reference for data . Check if they have phase errors with respect to each other of more then 4 ns. IF YES you require to change one of the chips and check again.

3. Check the TTL clock at the ECl to TTL converter chips.

4. Check the counter output for generation of clocks which are divisor of system clock. And also check the MUX output which select one of these clocks for DELAY card.

5. Check all the buffer outputs the clock passes through. Then check all the Gates the clock passes through. Also check all the delay lines and flipflops it passes through.

6. Once each clock is checked and found satisfactory.*(the criteria for a clock being satisfactory is that the jitter in the rising edge should not be comparable to the risetime itself. and the duty cycle of the clock should be as specified by the timing diagram at each point.)*

7. the next area to be checked is the counters. Once the clock has been checked the counters should be checked for proper functioning. This is included in the clock section as its functioning directly relates to the clocks. All the counters after reset should give square wave form of various frequencies (related by powers of 2) on its output pins.

7 Input Section

This section has ECL to TTL converters on the DPC card and TTL latches on the DELAY card. The section should be checked by comparing the input and output of the ECL to TTL converters and latches. The latches should not have any difference between input its respective output except some time delay (very small of the order of few ns.). and ECL to TTL converter should only be changed in levels.

Next we should check if the cards reset section is working properly or no. The Delay card uses reset, only to reset or preset some flip flops hence checking the flipflop outputs after providing a delay will tell one the status of delay cards reset.

The DPC card has a bit complicated reset section. This generates two reset pulses from STAinit and the master reset from the control card. One of them is used as card reset. The other is captured STAinit to reset the write counter on the Delay card. If after providing master reset the first STAinit is passed on the reset pins the reset section of the DPC card is working fine.

8 DELAY CARD: FUNCTIONAL TESTING PROCEDURE

8.1 Test setup

The delay card can be functionally tested by providing a fixed delay at the DSP bus (could be zero) and providing a input data which can be either a pulse of 32 ns of 2Kx64 ns wavelength or a sine wave whose

frequency is $(1/2K x 64ns.)$. The output should come out (depending upon the delay) $((a+(2K-d)*64)ns)$ later where a is a fixed delay offset due to data traversing through the card and d is the fixed delay given to the DSP bus.

Caution: During this test the write counter should not be reset every STAcycle. Instead it is only reset whenever the some new fixed delay is loaded.

A work around to this is that the fixed delay is replaced by delay which increments every FFTcycle by 512 clock ticks. This is a preferred configuration for testing functionality of the card.

8.2 Extensive Testing.

The IC pin number are denoted in this document as the dot extension after the IC number, and the positive logic TTL 0 is denote as low level and 1 is denoted as high level.

The DELAY card has several testpoints which when checked for proper waveforms ensure that the card will work fine. The testpoints are as listed below.

TP1 : This testpoint should be a low going pulse of 100ns with a period of 16.384 usec.

TP2 : This should be 32 MHz clock with restrictions of rise time less then 8 ns. The phase jitter in the clock should not be comparable to the rise time.

TP3 : This is a Ground tapping point.

TP4 : This should be a 16 MHz clock.

TP5 : This is a Ground tapping point.

TP6 : This should be a 16 MHz clock which should be 180 deg. out of phase with TP4 clock.

TP7 : This is a Ground tapping point.

TP8 : This should be a 16.125 MHz clock

TP9 : This is buffered version of TP8 clock.

TP10 : This is the 32 MHz clock which is derived from clock of TP2. It should be around 40 ns delayed from the TP2.

TP11 : This should be a high going pulse train of 16.125 MHz frequency. It can either be TP9 and TP12 ANDed or TP9 it self with a gate delay.

TP12 : This is 32.25 MHz clock.

TP13 : This is also a 32.25 MHz clock but out of phase by 180 deg. from TP12.

TP14 : This is a 32 ns low going pulse with a frequency of FFT cycle. i.e. the period is 16.384 usec. (From th the point of system synchronization this pulse should be 4 of 32 MHz clock cycles ahead of the start of FFT cycles.

TP15 : This is a 16 MHz clock derived from TP10.

TP16 : This is a 16.125 MHz clock .

TP17 : This is buffered TP6 clock hence it should be around 5 ns delayed TP6 clock with better current capabilities.

TP18 : This is 32 MHz clock and is 180 deg. out of phase with TP2 clock.

TP19 : This is Ground tapping point.

TP20 : This is a high or low level which decides the 1 clock cycle delay of data for channel 1 data.

TP21 : This is a high or low level which decides the 1 clock cycle delay of data for channel 0 data.

TP22 : This is TP13 delayed by 5 ns. i.e a 32.25 MHz clock.

TP23 : This is a Ground tapping.

For the sake of completeness, notes which are present on the schematic diagram of the delay card are listed below.

1. The references for IC's are so arranged as to move from top to bottom then bottom to top and so on... on the card, starting from 64 pin DIN connector. This is done to ensure quick homedown to a part on the card.
2. All the signals ending with 'áre active low signals.
3. Datalines with suffix as numbers, imply that the highest number suffix is MSB.
4. U14 pin 1 has to be connected to RSTB which is pulled high on the card. (Although this will not affect single card testing it will reduce coherence between different cards in the bin.)
5. U22 pin 1 has to be connected to CNTLSB , on card it is CNTLSB. (Before making this change one should check if the data is as expected even if one has shorted U22 input to output. If so you do not require to make this change. i.e. U22 is optional on the card and just to create proper timing relationship (which will depend upon different IC AC characteristics), and this change is required only if IC U22 is required.
6. All the decoupling capacitors are 220 nf. Electrolytic cap. is 100 uf.
7. Inductor l1 is not required.

9 Bench testing problems and possible solutions.

This section can also be referred to in field testing too. The test setup as explained earlier is setup and data is given to both the channels then if:

1. Data is not present at both channels at the output of the DELAY card.

```
Check if there is any input to the card or no.
 {if input is there check TP4 and TP5
   { if.TP4 and TP5 are as expected,
   }
}
This indicates some problem with the read section of the card.

{ Check if TP11 is as expected.
          {if TP11 is as expected, check output of U23
```

```
                { If output is not present IC U23 needs to be changed.
                  If the output is present, check TP20 and TP21
                }
                       { if TP21 and TP20 are
                          a. Both Low.
                               Check output of U27
                                   {If output not present then
                                     {Both the IC U27 and U29 need
                                      change.
                                     }
                                   else U28 and U30 need a change.
                                   }
                          b. Both high.
                               Then  check TP22.
                          c. TP21 is low.
                               Then U28 or U29 need to be changed
                               and for other channel check TP22.
                          d. TP20 is low.
                               Then U27 or U30  need to be changed and for
                               other channel check TP22.
                       }
                { if TP22 is as expected check U25 output.
                     { if no output is present U25 need a change.
                       If output is present check TP13.
                     }
                         {if TP13 is as expected check U24 output.
                            { If no output U24 need to be changed.}
                         }
                }
                {If TP22 is not as expected, check TP13
                     { If TP13 is as expected check specification of
                       U26 and change U26 if required.
                     }
                     { If TP13 is not as expected check U20.10 and
                       U20.11 if they are differential and of proper
                       ECL levels then then change IC U20. else check
                       the 32.25 MHz clock source on back plane.
                     }
                }
}
{ If TP11 is not as expected, check TP12
           { If TP12 is as expected , check TP9
              { if TP9 is as expected change U11.
                  {  if TP9 is not as expected, Check U10.5
                  }
                      { if U10.5 is as expected change U10
```

```
                        {If U10.5 is not as expected, check TP8
                            {if TP8 is as expected check U8 and U13
                             outputs they should also be as expected
                             else change those ICs
                            }
                        }
                    }
                }
                { If TP12 is not as expected check 32.25 MHz clock
                   input to card.
                }
            }
        }
```

One of them should be the problem with the card.

2. Data is not present at the output of one of the channels although the input to the card is proper.

```
Check TP4 (if channel 0)
    { If TP4 is proper check U7 output.
        {If output is not  present, change U7.}
         If output is present, check U19 output.
              { if output is not present change U19
                if output present, check output of U28
                    { if output is present change U29.
                      If output is not present change U28.
                    }
              }
        }
    }
```

TP4 should be proper other wise one wont receive any data on the other channel too. One of these remedies should be able to solve this problem.

(For Channel 1 replace U7, U19, U28, U29 by U6, U15, U27 and U30 respectively.)

Output of the card is a square functions where as input to the card is a pulse with low frequency.(or sine wave for that matter.)

```
Check if TP15 is as expected (listed earlier).
      {If TP15 is fine, check the outputs of the ICs U18 and U17.
            { If the outputs of ICs U18 and U17 are not
```

```
                    present check U18.20 and U17.1.
                        {if U18.20 and U17.1 are low check U10.16.
                            {if U18.20 and U17.1 are not low then these
                             ICs are to be replaced.
                            }
                        }
                        {if U10.16 is low check U10.4.
                            {if U10.16 is not low then put a wire
                             strap between U18.20 and U10.16.
                            }
                        }
                        {if U10.4 is not low. IC U10 has to be
                         replaced.
                        }
                        {if U10.4 is low check P1.55.
                               { if P1.55 is not low put a wire
                                 strap between P1.55 and U10.4.
                                 if P1.55 is low the card is Ok
                                 check the backplane or respective
                                 DPC card.
                               }
                    }
            }
    }
    {If TP15 is not as expected check TP10.
        {If TP10 is not as expected, check TP18
            {If TP18 is not as expected, check backplane
              for clock coming from DPC card.
              if TP18 is as expected, change U16.
            }
        }
        {If TP10 is as expected, check U10.11
            {If U10.11 is same as TP10, change U2
             If U10.11 is not same as TP10 change U10.
            }
        }
    }
```

One of the things suggested above should be able to solve this problem.

4. Instead of one 32 ns pulses one gets 64 ns pulses.

```
Check the input to the card.
  {The input is little more then 32 ns., check the input source.
```

```
      {This will cause the problem to occur.}
   }
   { The input is less then 32 ns.
        { Check TP4 and TP6 for 180 deg. phase difference
           { if phase difference is not there the problem
             is this, check DPC and Backplane for this.
           }
           {If phase difference is there, check U23.1 and U21.1
              {if U21.1 is tristate, change U16.}
                  {if U23.1 is tristate, check U22.1
                      { if U22.1 is as expected, change U22.}
                         {if U22.1 is not as expected,check TP8.
                            {If TP8 is as expected, change U16}
                            {If TP8 is not as expected, check TP16.
                               {If TP16 is as expected, take out U16 and
                                check TP8.
                                 {If now it is as expected, change U16}
                                 {If still it is not as expected,
                                    change U14.
                                 }

                               }
                            }
                         }

                  }

           }
        }
   }
```

One of these should be able to solve the above mentioned problem.

5. The output has two 32ns consecutive pulses, once in a while even when one 32 ns pulse is given as the input.

```
Check U23 input and U21 input with respect to TP11.
  { If a 64 ns pulse is latched twice, check U11.4
        {If it is same as TP12 change it to TP13, This provision is
         available on card.
        }
        {If it is same as TP13 change it to TP12, This provision is
         available on card.
        }
```

}

. The delay expected and delay achieved between input data and output data is not the same.

```
Check TP1.
    {If TP1 is as mentioned earlier in this document, check U1 input
     and U4 outputs.
        {if the value is equal to the delay set , check TP14
            { TP14 does not get a pulse of 64 ns, check U14.12
                { If U14.12 is not present check on backplane and
                  control card. (Delay card has no problem.)
                }
                { If U14.12 is present, check TP8 with respect to U14.12
                    { If the relation is not such that U14.12 can be
                      captured, check control card.(delay card has no
                      problem.)
                    }
                }
            }
            { If TP14 has a pulse of 64 ns. , Check the output of
              U8. and U13. It must be having some bits stuck to
              high or low. change these ICs.
            }
        }
        { If the value is not equal to delay set, change IC U1 or U4
          which ever required.
        }
 }
 { If TP1 is not as required, check U5.9 and U5.10
     { If these pin's signals are OK, change U5.}
     { If these signals are not OK check back plane and control card
       for this delay card has no problem.
     }
 }
```

of these solutions should be able to eliminate the above mentioned
blem.

se are fairly exhaustive list of problems and there solutions, which may occur during bench testing.

10 DPC CARD : FUNCTIONAL TESTING PROCEDURE