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(Correlator Group)

(Ref: rkm11/SPEC2/sept92)

FINAL DESIGN OF THE DIGITAL SPECTROGRAPH

INTRODUCTION: Design of the Digital Spectrograph has been finalized. This writeup gives a broad introduction to the various features of the Spectrograph. Complete circuit details are also enclosed. Valuable experience gained out of working with the FX ASICs has been utilized and suggestions to include complete Polarization Measurements have also been incorporated.

Main Features: The system consists of the following three main sections:

- (i) **TWO-PIPELINE FFT CARD** --- expected size = 6U
- (ii) **FOUR-ASIC MAC CARD** --- expected size = 3U
- (iii) **CONTROL CARD** --- expected size = 6U

A Microcontroller, 8031, has been included in the Control part. Initializations and TRIG TABLE loading are taken care of by the microcontroller.

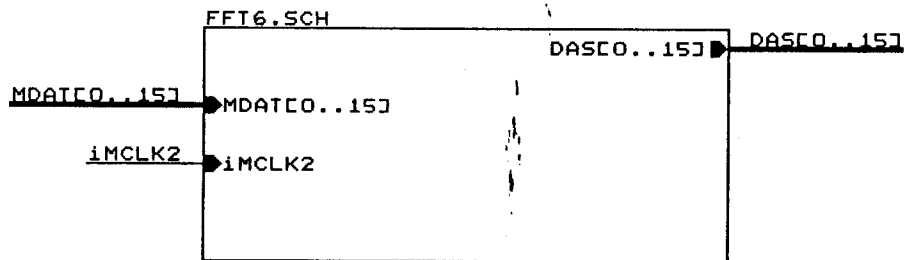
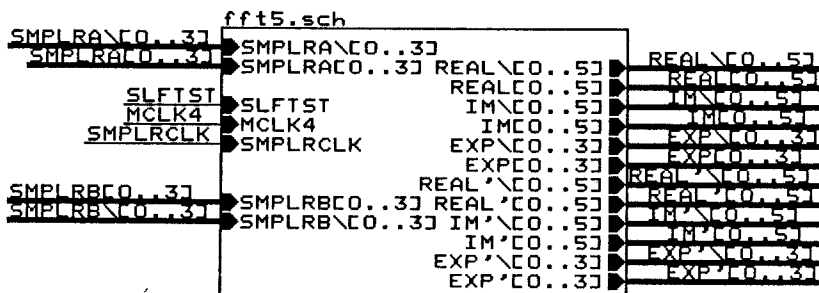
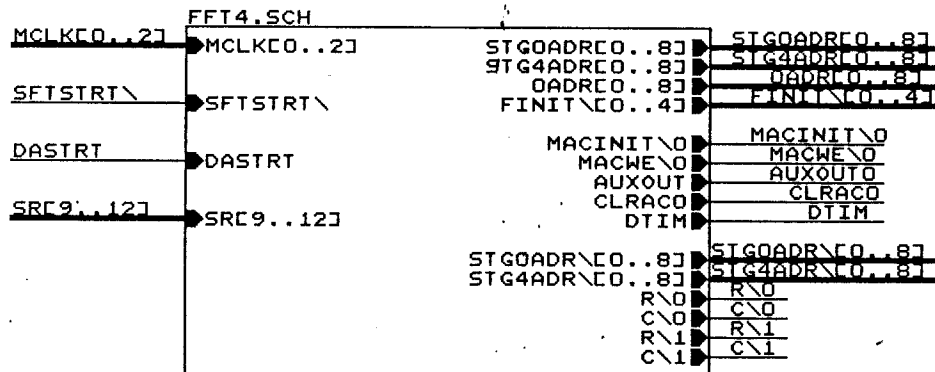
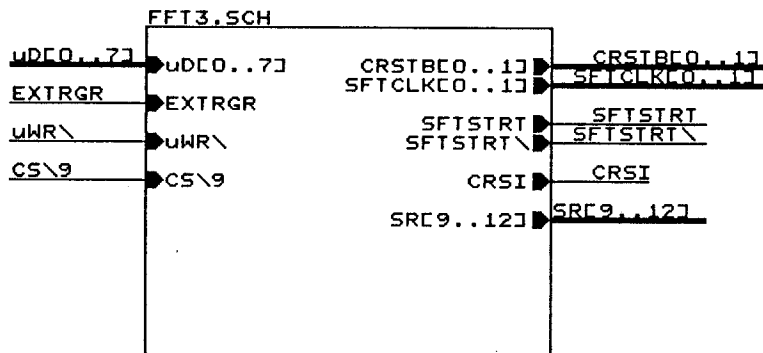
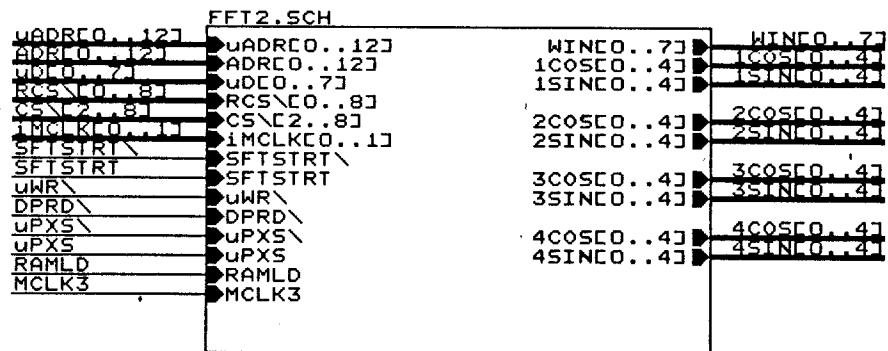
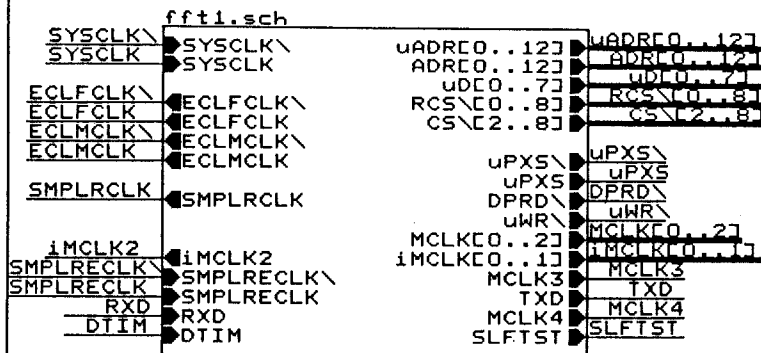
Options have been provided for RAM Check etc.

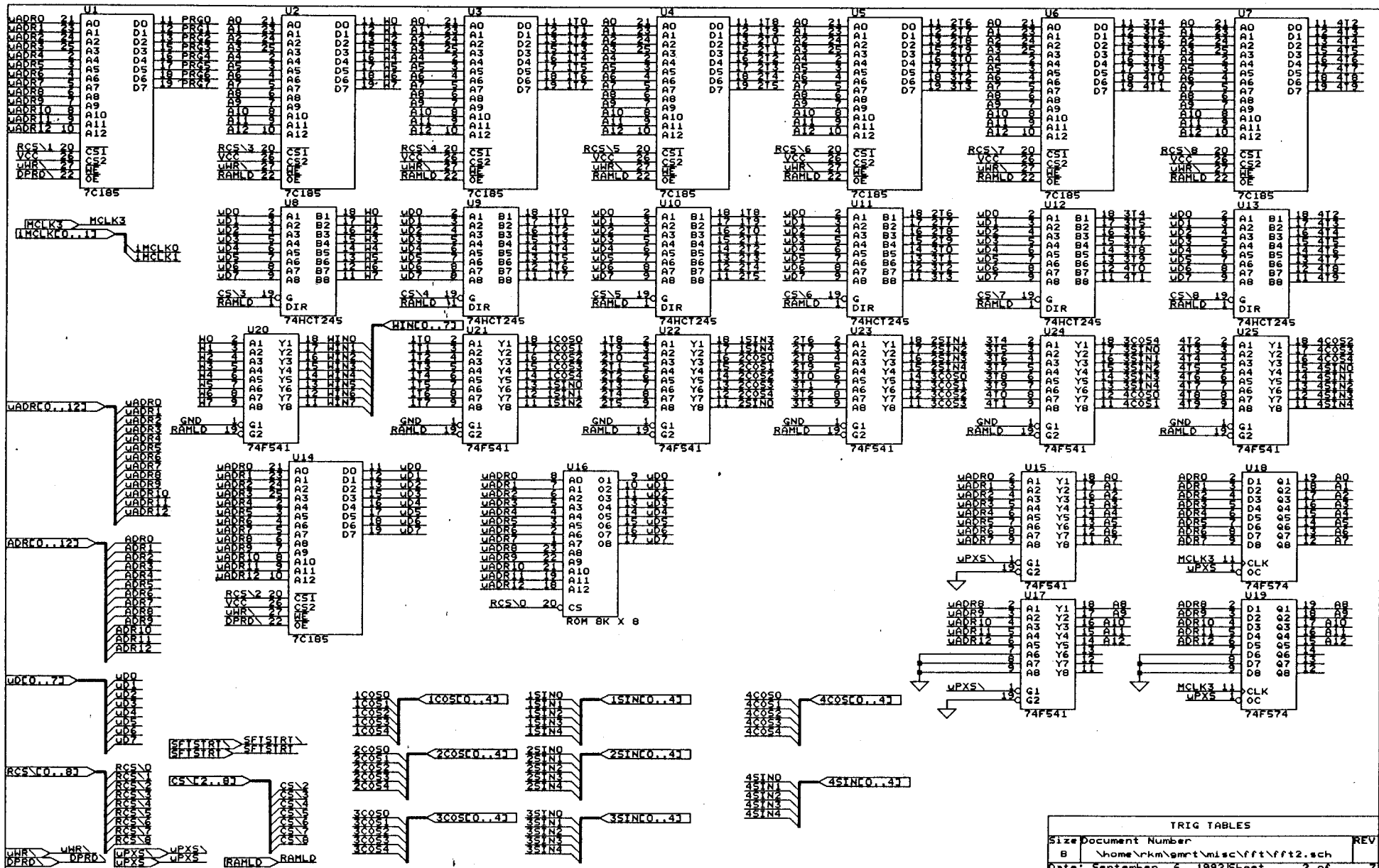
The following measurements can be made :

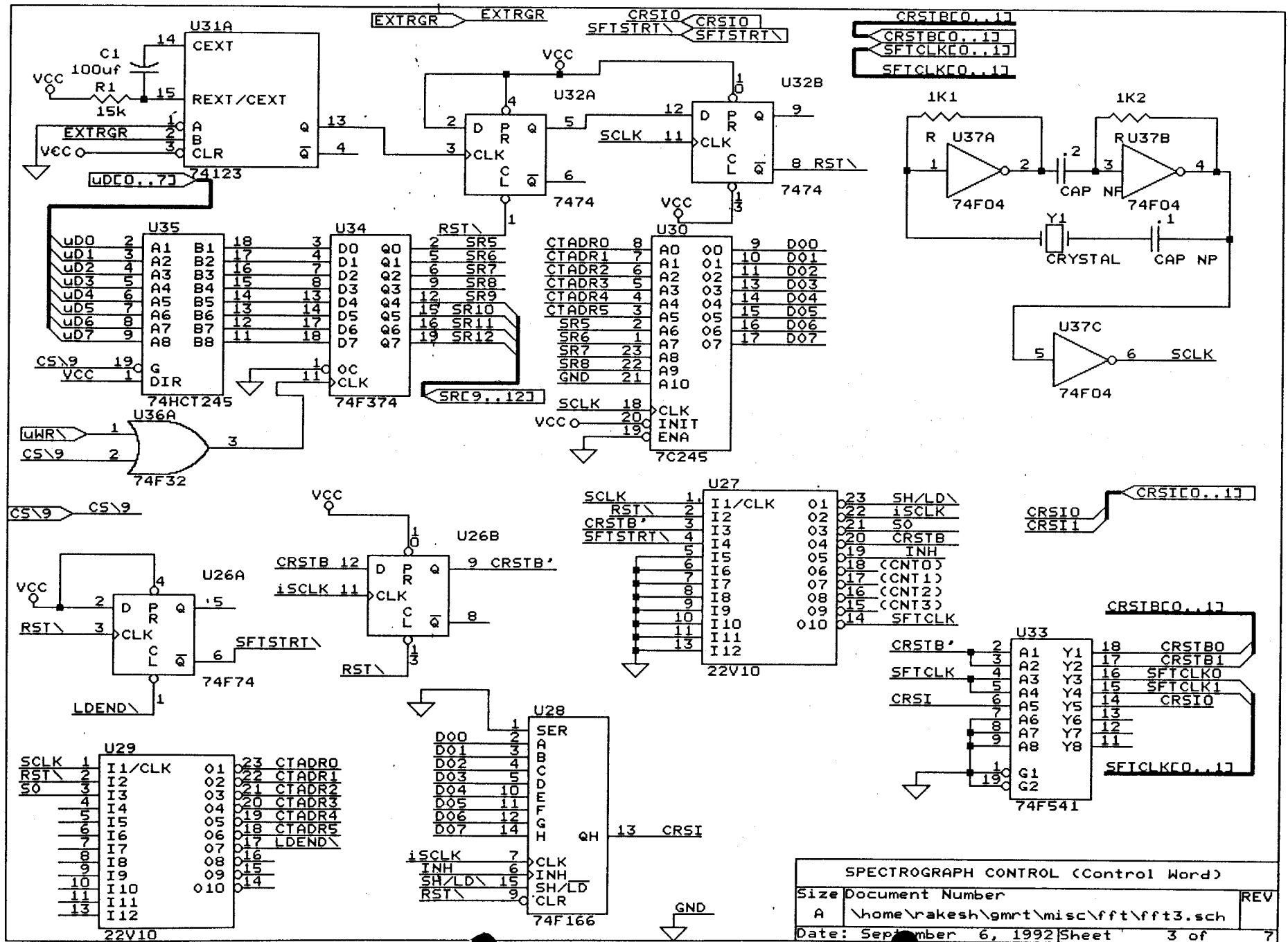
- (i) **Full Polarization : 128 Channels over a Bandwidth of 16 MHz**
- (ii) **Non Polarization : 512 Channel Spectrum over a Band Width of 32 MHz**
- (iii) **Two-Antenna Interferometry : 256 Spectral Point Correlation over a Bandwidth of 16MHz.**

Since till now we have been using NRAO Cards for FFT and MAC, the design of FFT and MAC Cards also provides the much needed indigenous FFT and MAC Cards.

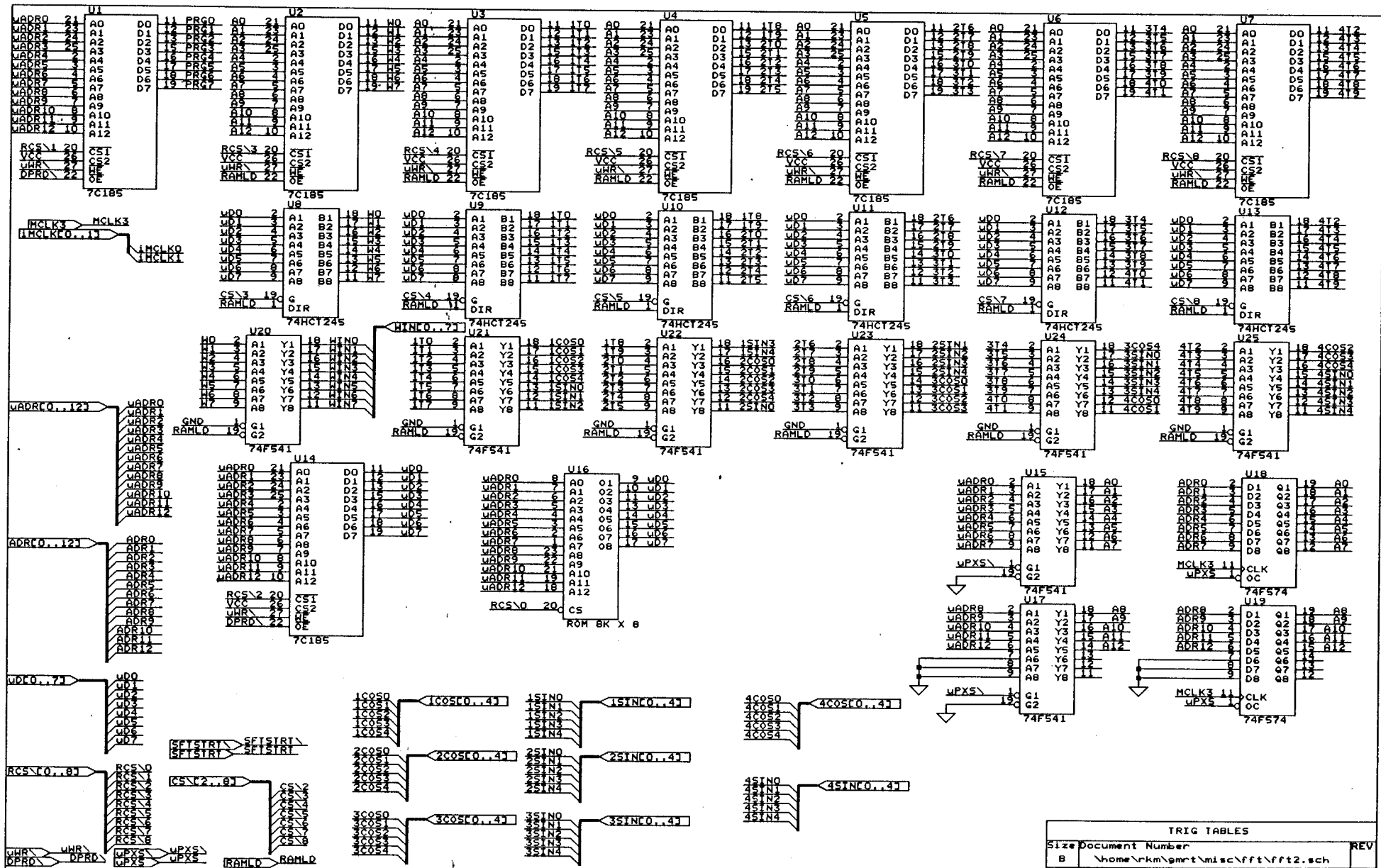
Acknowledgements: I thank Vivek Tatke for cross checking some of the things and offering to undertake the fabrication part in my absence.



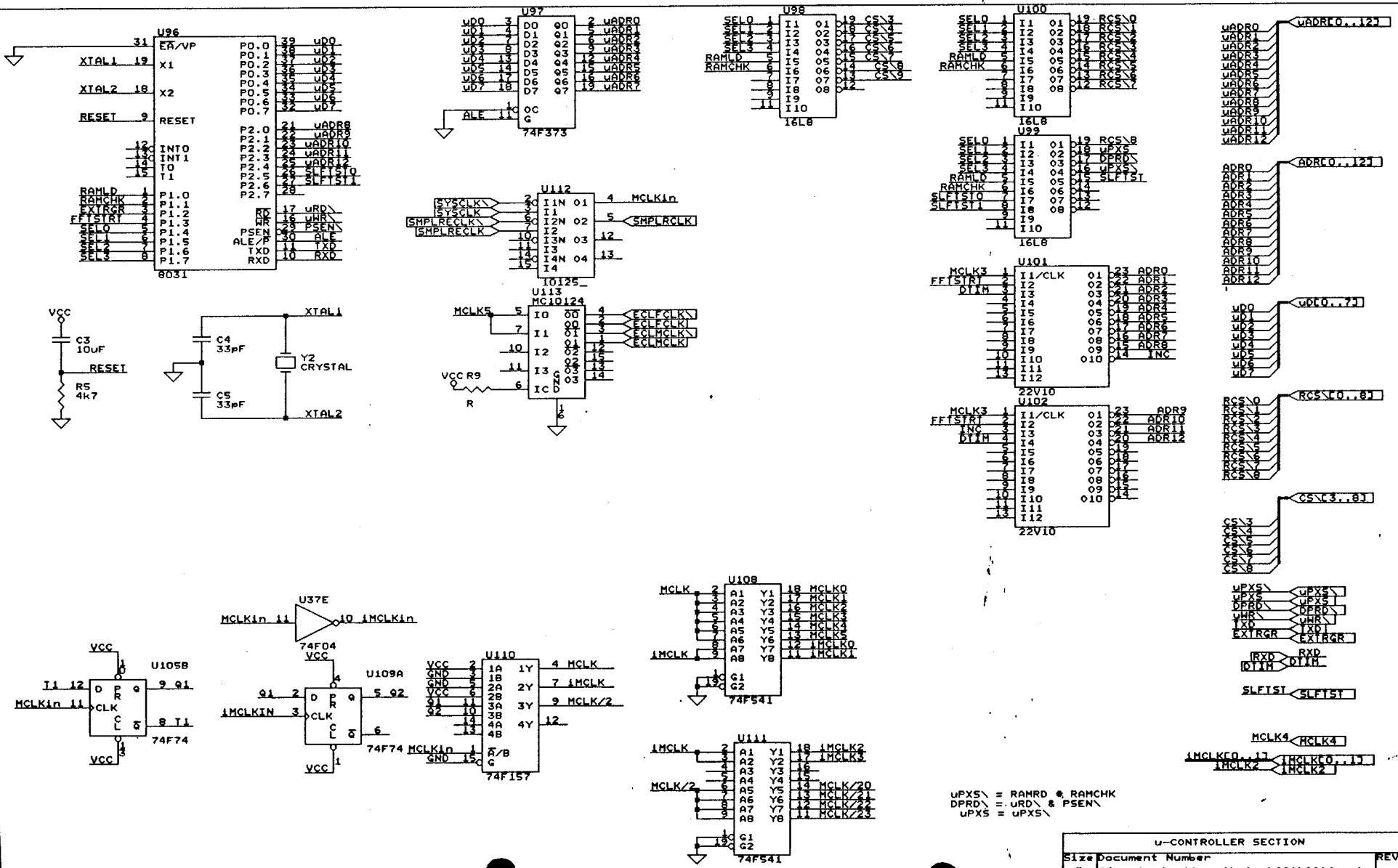


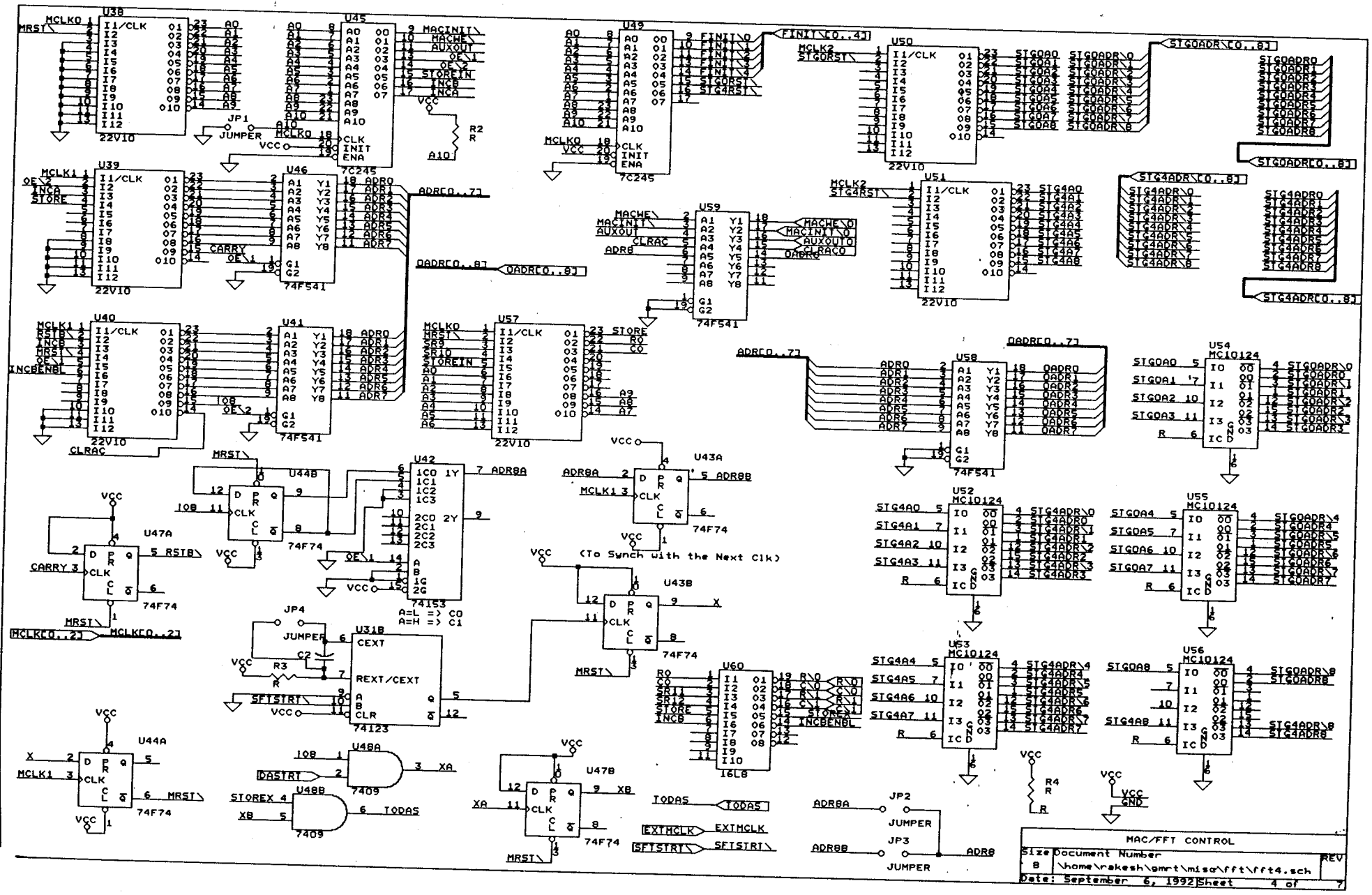


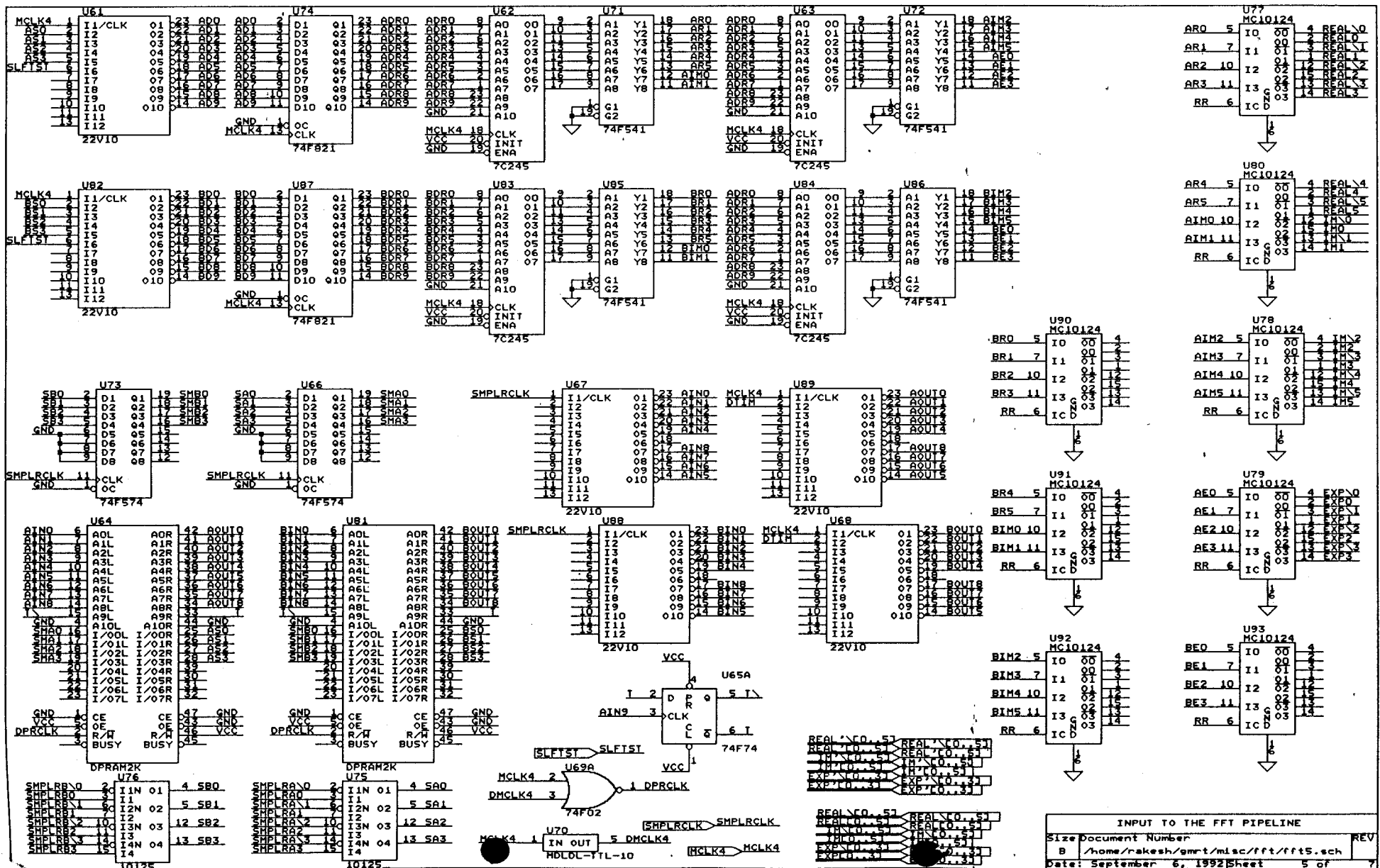
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TRIG TABLES		
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Date:	September 6, 1992	Sheet 2 of 7







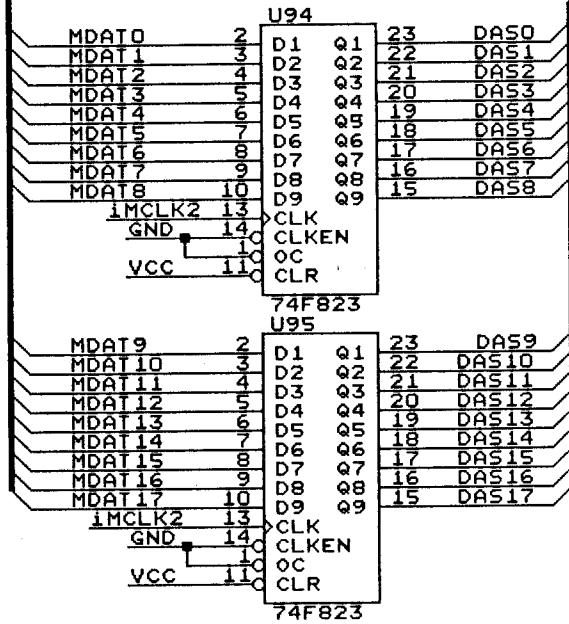
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DAS0..17J DAS0..17J

IMCLK2 IMCLK2

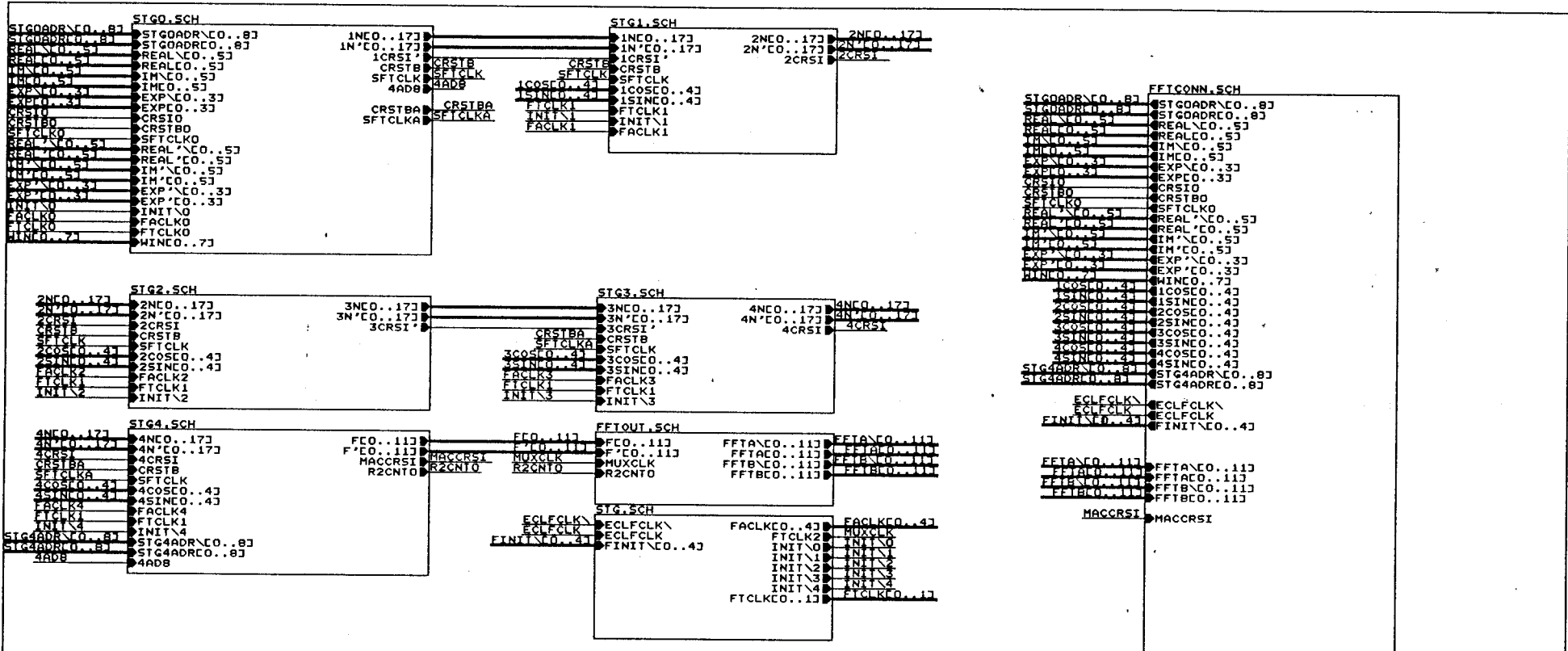
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DAS0..17J

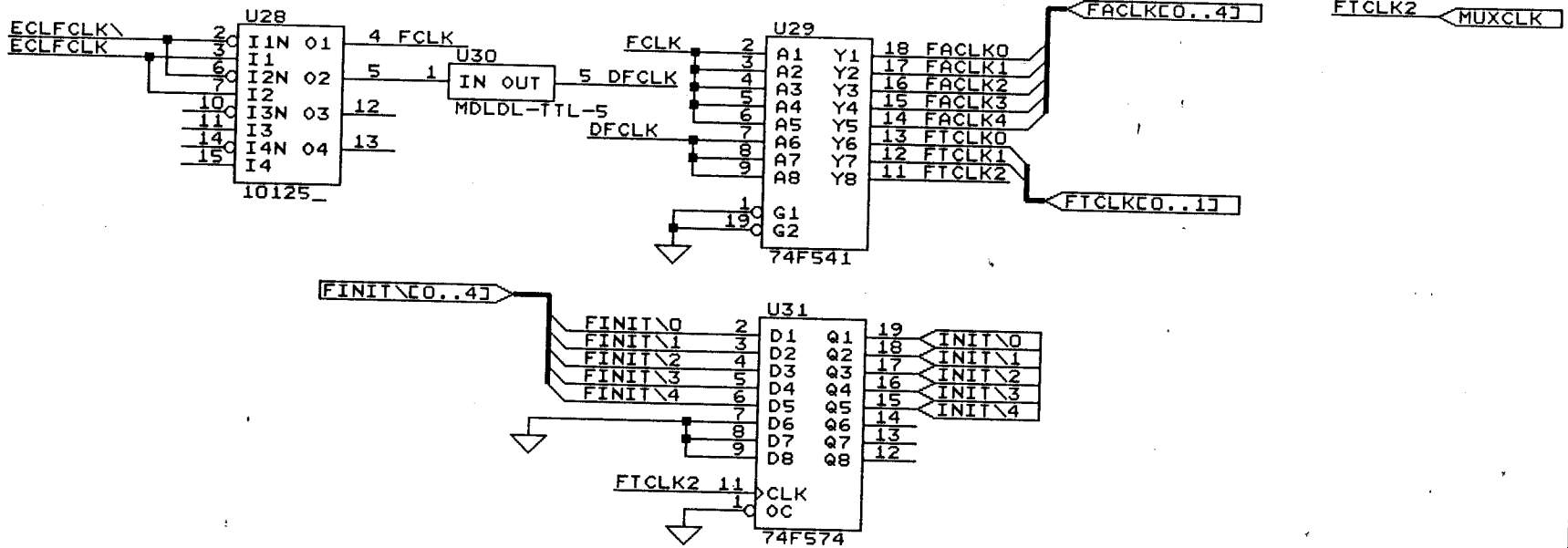


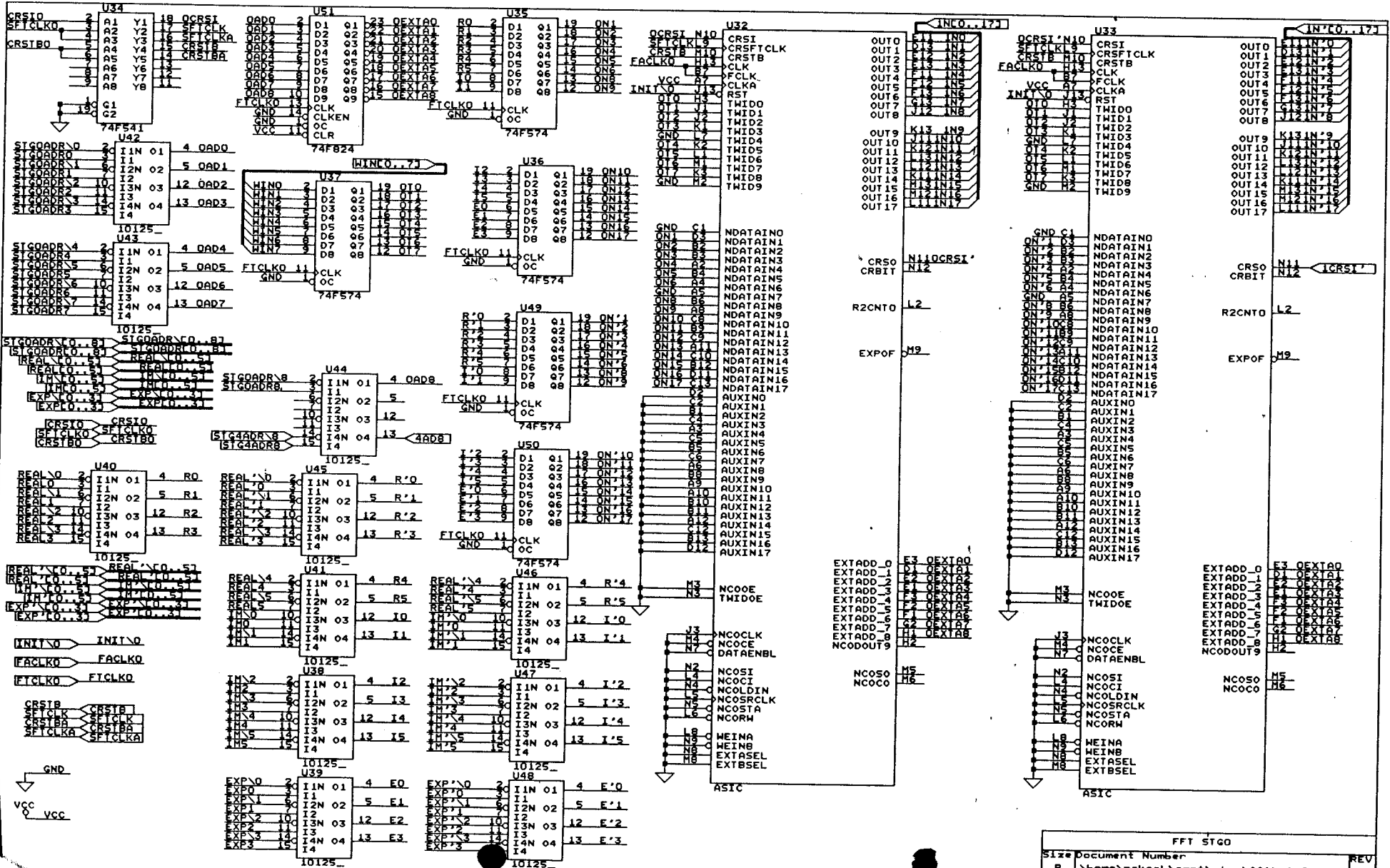
SPECTROGRAPH OUTPUT

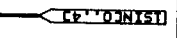
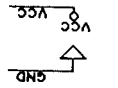
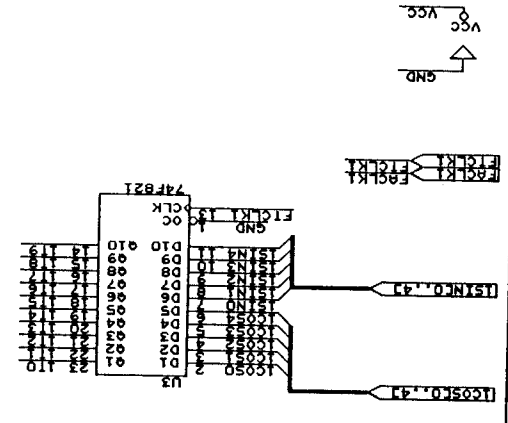
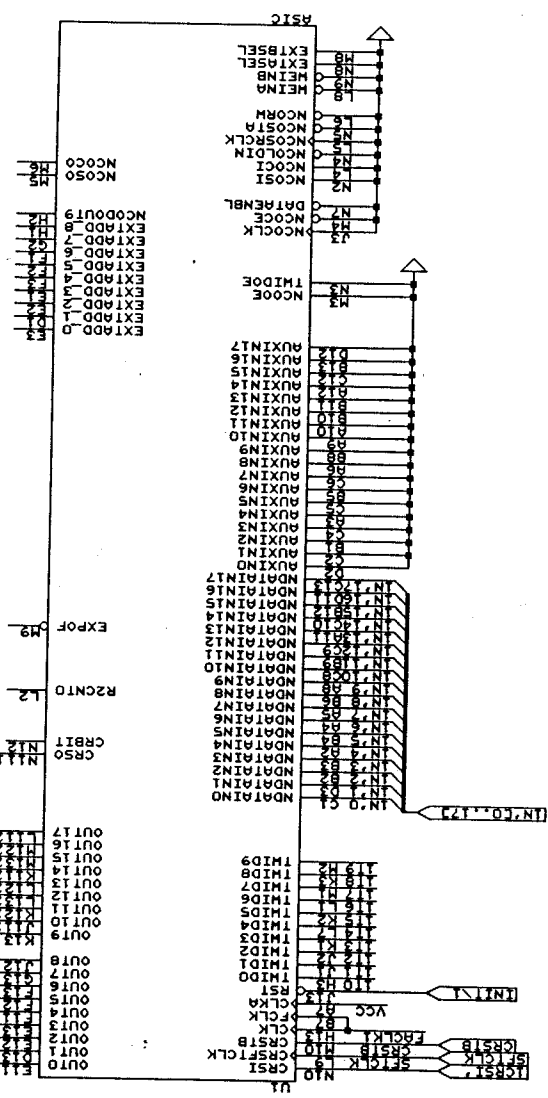
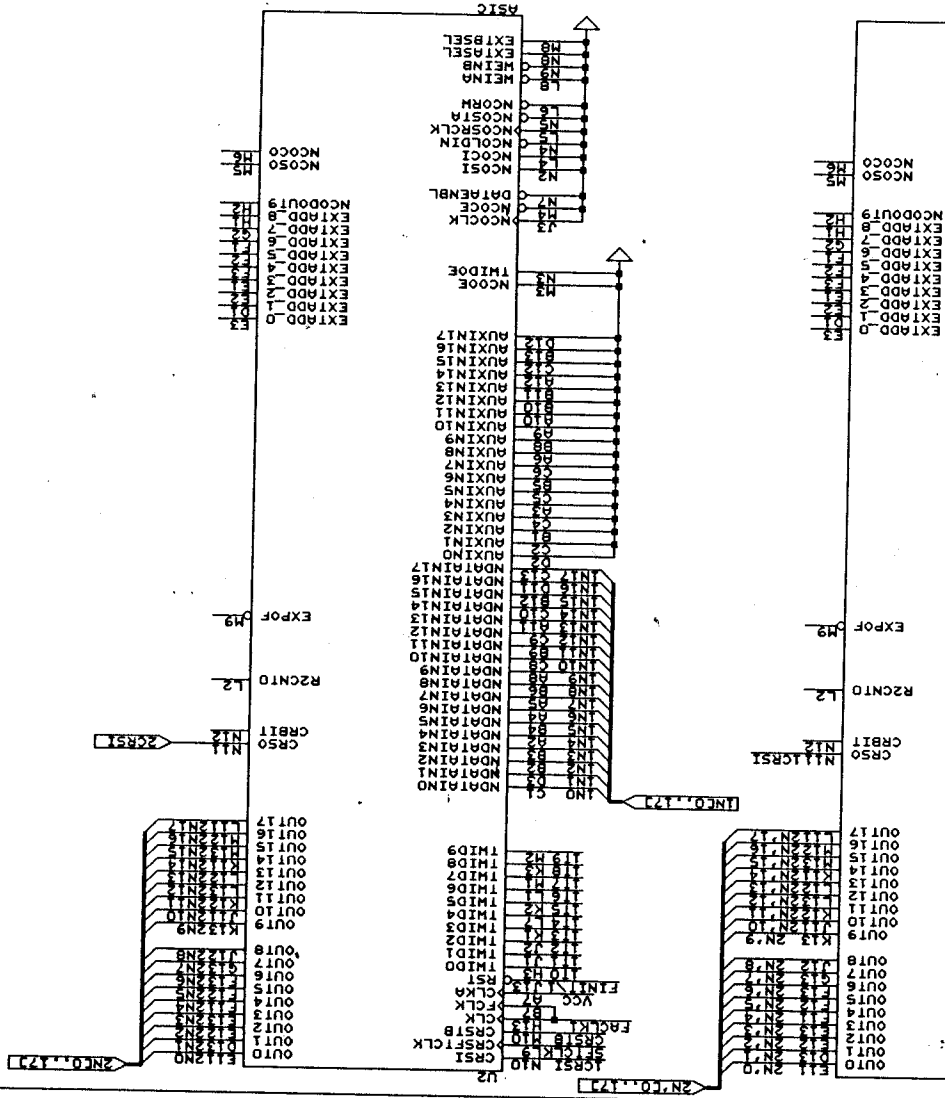
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ECLFCLK
ECLFCLK
ECLFCLK





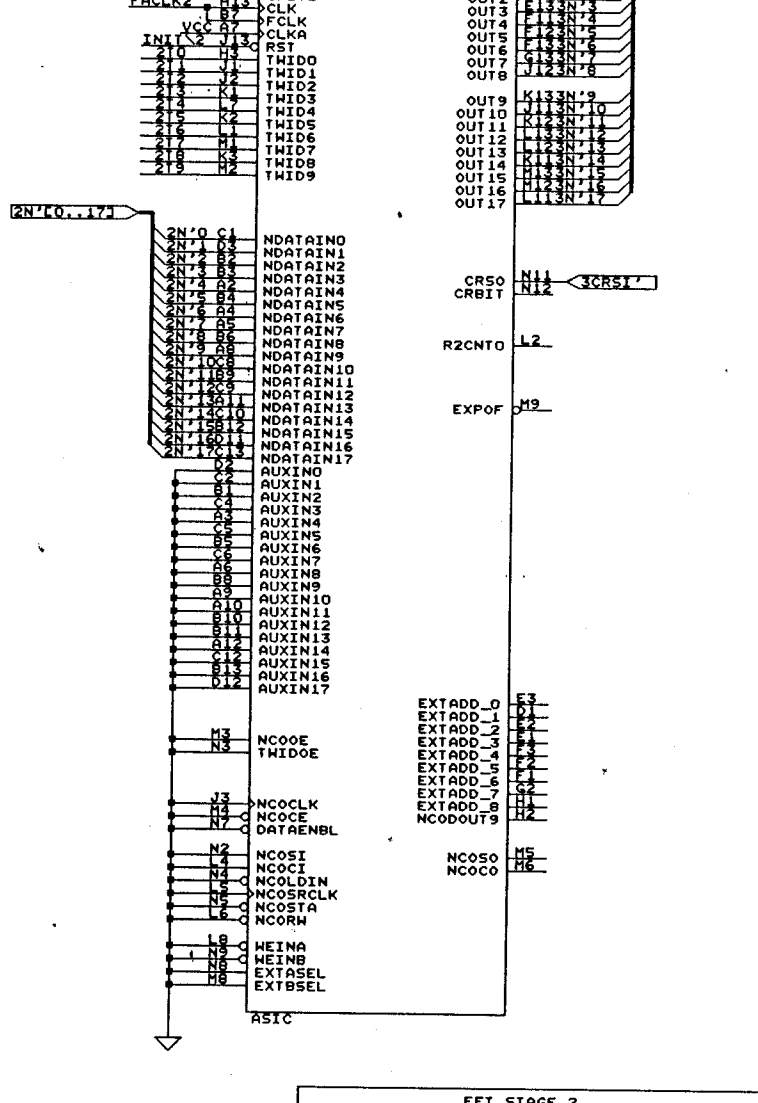
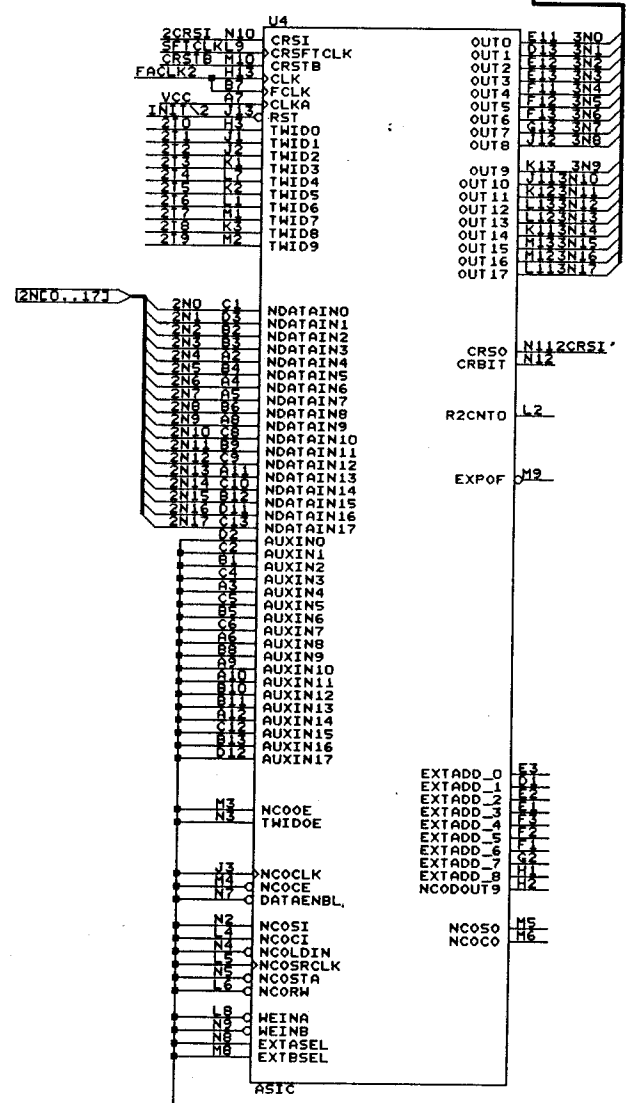


IN12
 IN11
 IN10
 IN9
 IN8
 IN7
 IN6
 IN5
 IN4
 IN3
 IN2
 IN1

2CRSI N10
 2CRSTB N10
 2SFTCLK N10
 2VCC N10
 2GND N10

VCC
 GND

VCC
 GND



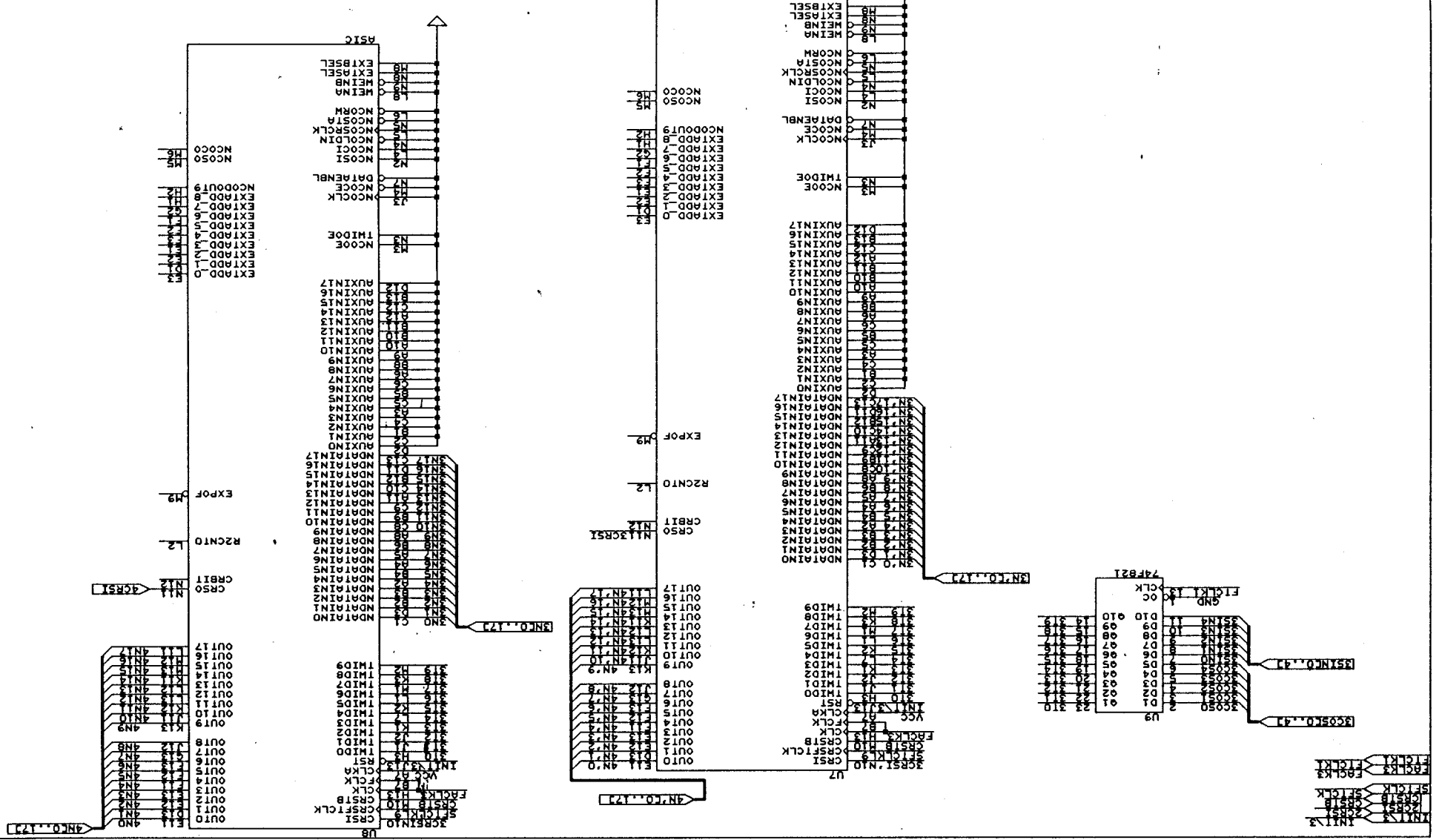


Fig. 13	Fig. 14	Fig. 15	Fig. 16	Fig. 17	Fig. 18	Fig. 19	Fig. 20	Fig. 21	Fig. 22	Fig. 23	Fig. 24	Fig. 25	Fig. 26	Fig. 27	Fig. 28	Fig. 29	Fig. 30	Fig. 31
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100

Fig. 32	Fig. 33	Fig. 34	Fig. 35	Fig. 36	Fig. 37	Fig. 38	Fig. 39	Fig. 40	Fig. 41
1	2	3	4	5	6	7	8	9	10
100	100	100	100	100	100	100	100	100	100

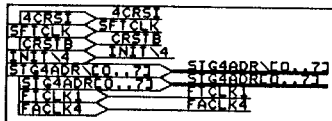
4N.O..171

4N.O..171

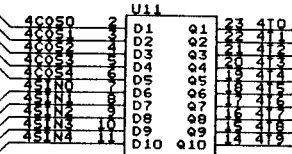
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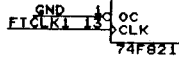
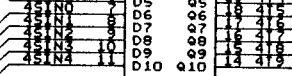
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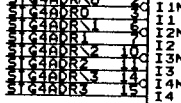
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4SIN0_4J

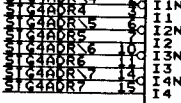


SIG4ADR0



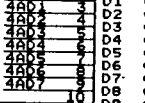
I0125_

SIG4ADR4

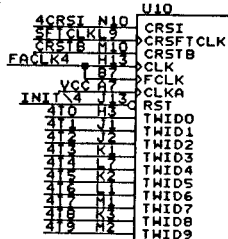
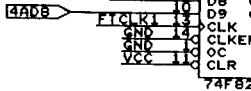


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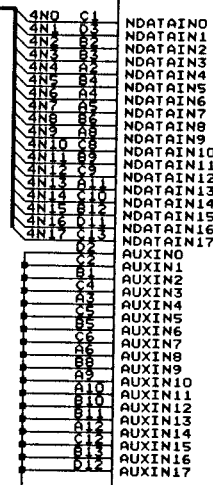
4AD0



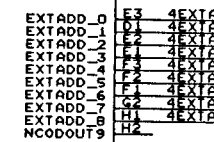
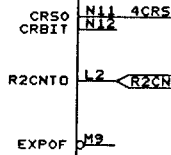
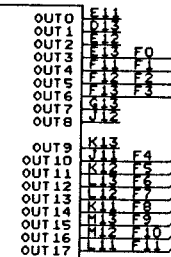
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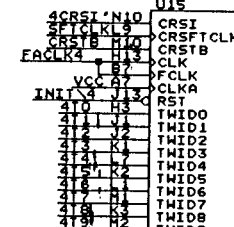


ASIC

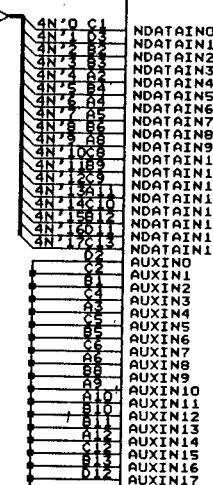


NCOS0
NCOCO

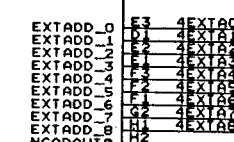
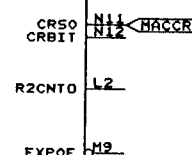
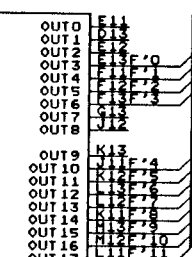
F10_11J



4N0_0J



ASIC

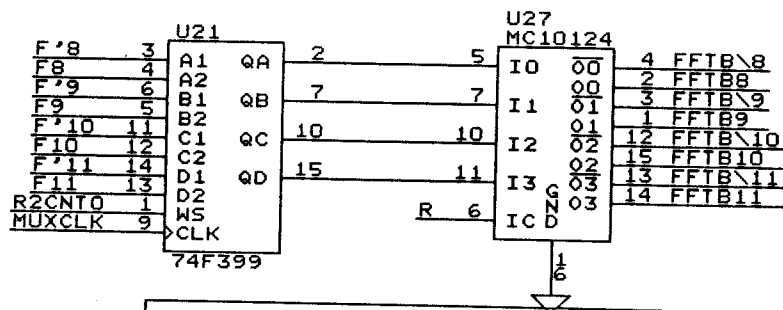
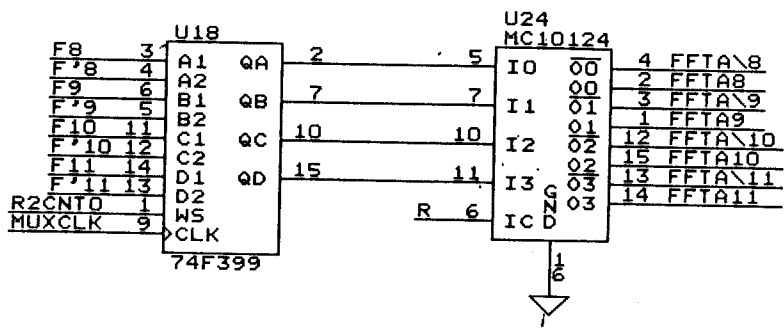
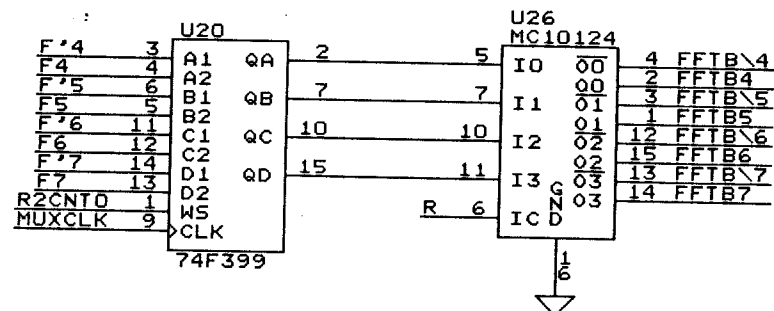
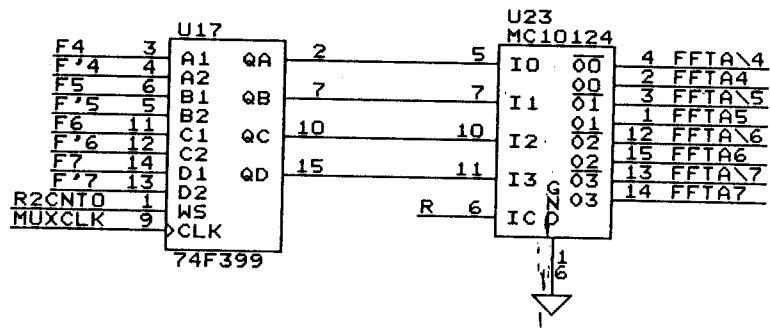
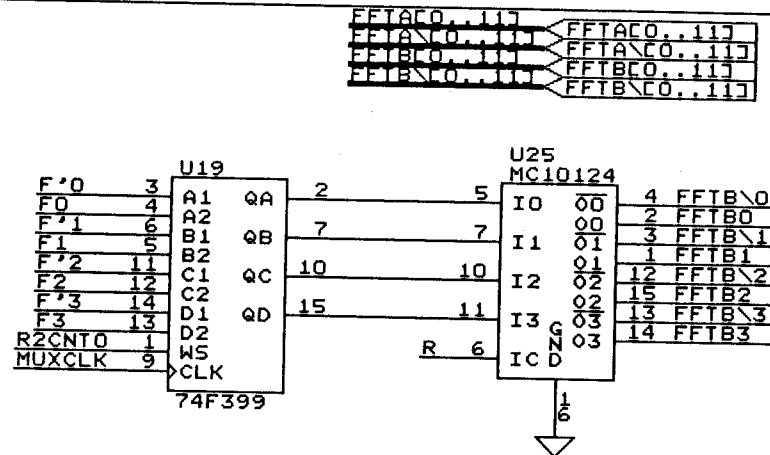
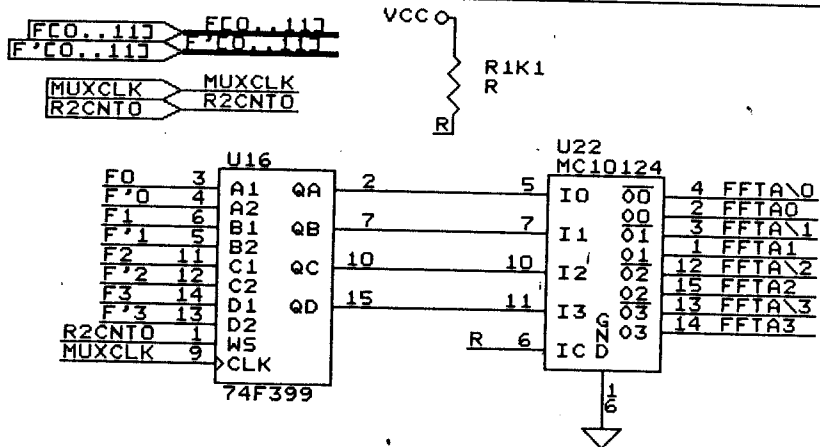


NCOS0
NCOCO

F10_11J

HACCRS1

VCC



FFT OUTPUT

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