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(Ref: rkm10/MACTRL/aug92)

MAC CONTROL: DESIGN AND IMPLEMENTATION

INTRODUCTION: Some tests related to the MAC Operation of the Correlator System have been performed with the Prototype MAC Control Card. In this report, I give the details of the Prototype Board as well as the Critical Timing Requirements so that one does not have to start struggling from scratch once again.

MAIN FEATURES: Main features which have been implemented in the Prototype Card are:

(i) Control Word Loading : any number of ASICs from One to Sixteen – User Selectable

(ii) Number of Accumulations : 256, 512, 1024, 2048 or 4096 – User Selectable

(iii) Number of ASICs to read the results from: 1 to 16 — User Selectable.

The number of options provided here is restricted by the amount of logic one can pack in 22V10s without having to use additional chips.

FUNCTIONs of VARIOUS CHIPS:

(i) **U10 :** Radix-516 Counter to Address the MAC SEQUENCER ROM U27. **When MAC is INTEGRATED with FFT, SEQRST can be used to synchronize the MAC Sequencing with respect to the FFT Output**

(ii) **U11 :** Integration Address Counter.

(iii) **U12 :** Readout Address Counter.

(iv) **U26B :** For BANK SWITCHING.

(v) **U17 :** Decides the number of accumulations to be performed depending on the DIP Switch settings of S4. The following options are available:

MODE=0 => 256 Accumulations

MODE=1 => 512 Accumulations

MODE=2 => 1024 Accumulations

MODE=3 => 2048 Accumulations

MODE=4 => 4096 Accumulations

(vi) **U16 :** Used for Decoding R0,1 and C0,1 to generate individual ASIC Chip-Selects. Here one can specify the actual number of ASICs to read thus ensuring no dummy readout operation. S4 is used for defining the number of ASICs between 1 and 16 (0 on the DIP Switches stands for 1 ASIC, 1 for 2 and so on). U16 suppresses the unwanted latching pulses (STOREX) to avoid dummy READOUTs.

The functioning of other chips is obvious from the schematics. CONTROL WORD LOADING Part (upto U9) has already been described in [1].

CRITICAL TIMINGs : Timing of the following inputs to the ASIC is extremely critical for the MAC Operation of the Chip :

MACINIT , MACWE , INTEGRATION ADDRESS, READOUT ADDRESS, CLRAC and BANK SWITCHING.

Timing of these signals at the ASIC input is shown in *Fig 1.* One **MUST** stick to these timings except may be in the case of CLRAC provided one has taken care of its timing with respect to MACWE .

The other signals, AUXOUT and STOREX are relatively harmless and are used for reading out the MAC Output. One only has to ensure that one doesn't try to Readout the Latched Data in the Clock Period when MACWE is asserted.

PRESENT CONFIGURATION:

(i) Presently, Jumper JP8 is connected to provide Trigger Pulse from the PUSH-BUTTON Switch on the PCB. However one can use JP7 instead of JP8 and use an external Trigger Pulse connected to EXTRGR on the connector.

(ii) With the present configuration, setting S3=5 shifts in Control Word for MACNP. This enables CRBITs in all the ASICs and CRSO Pins are alternately HIGH and LOW starting from HIGH at the first ASIC. The control word in HEX is:

29(or A9) , 02, 31,10

If someone wants to make some changes in the Control Word Data ROM U5, he must take into account the fact that MSB of the Byte coming out of the ROM gets shifted in first by the PISO U3. The above mentioned Control Word has taken this into account and it is written here the way it is stored in the ROM.

(iii) End of the CONTROL WORD Loading automatically brings the various components to appropriate Initial States and starts the MAC Operations. However, by using JP17 instead of JP18, one gets control over the start of MAC SEQUENCing in order to align it with respect to the FFT output. This pulse is expected to come from the FFT Control.

(iv) ROM U27 generates 16 pairs of STOREIN pulses per FFT Cycle with AUXOUT asserted 16 times. The STOREIN is suitably suppressed in U16 and U17 to meet the requirements of the User-Selectable Number of Accumulations and to avoid dummy read operations.

(v) STOREX from the MAC Control Card goes as STAREAD to the MAC Card.

(vi) For all the tests so far, Internal Address Generators in the ASIC have been utilized. This is sufficient for MACNP and Full Polarization Operation of the MAC. However with the timing of the Addresses clearly understood, it is a straightforward job to go for complete external control of the addresses. The space

available on the board can be utilized for this purpose. NRAO MAC Card can also be easily configured for external addresses.

(vii) The System Clock and the Shift Clock are being derived from the outputs of a Counter which is being driven by a Crystal. This addition was made later on after the Clocks from U6 were found to be unsatisfactory. However, after Integration with FFT, the System Clock has to be Common with the FFT System.

TEST PATTERNS: Since it would not be possible to list all the Test Patterns which were used for validating MAC, only a few of them are given here. Other patterns can be generated from the Software Simulator [2].

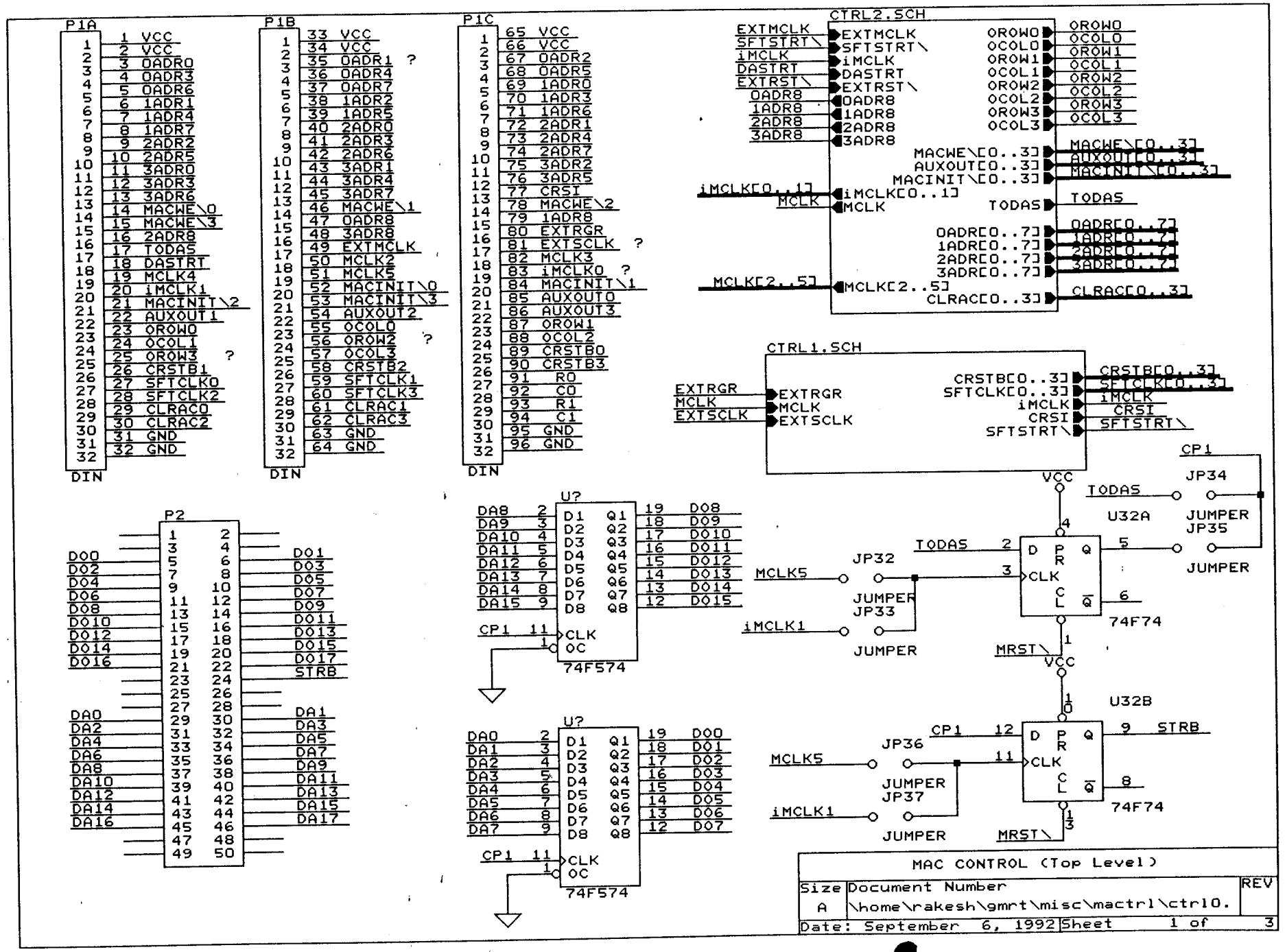
INPUT	No. of Accumulations	OUTPUT	
		(RAMA	RAMB)
F00 x F00	1	10000	20000
	256	10000	20000
F35 x F35	1	11100	20000
	256	0A200	28000
F28 x F28	1	10200	20000
	256	32000	20000
3BE x 3BE	1	11680	38000
	256	0AB00	00000

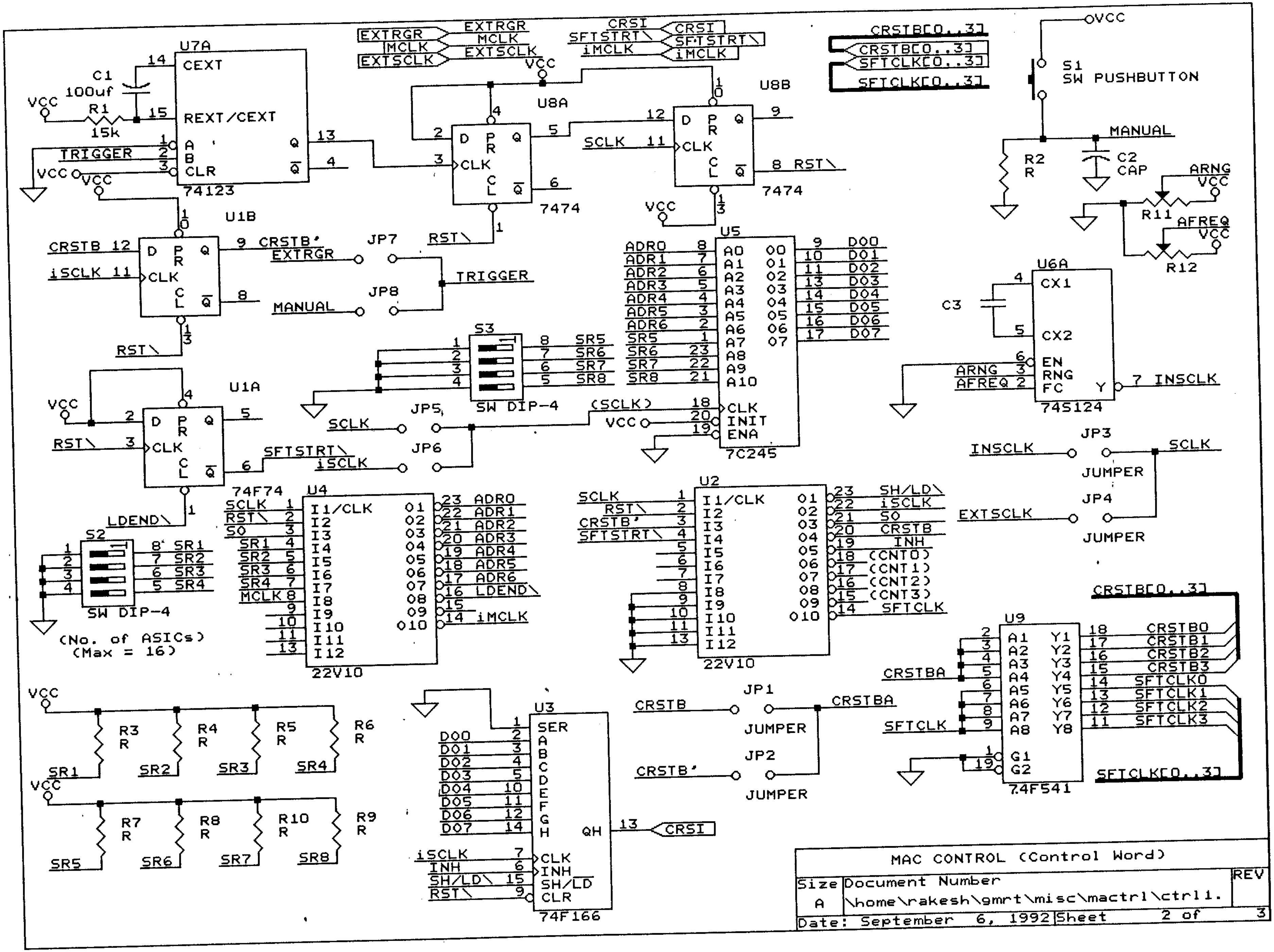
SUMMARY: Instead of a rigid ROM based logic, a flexible logic with various useful user selectable options has been implemented by properly utilizing the capabilities of GAL 22V10 Programmable Devices. Board outlook can be simplified further if we start using better EPLD's. We have reached a stage where we can freeze the specifications and implement the final design of the MAC Control as well as the MAC Card.

REFERENCES:

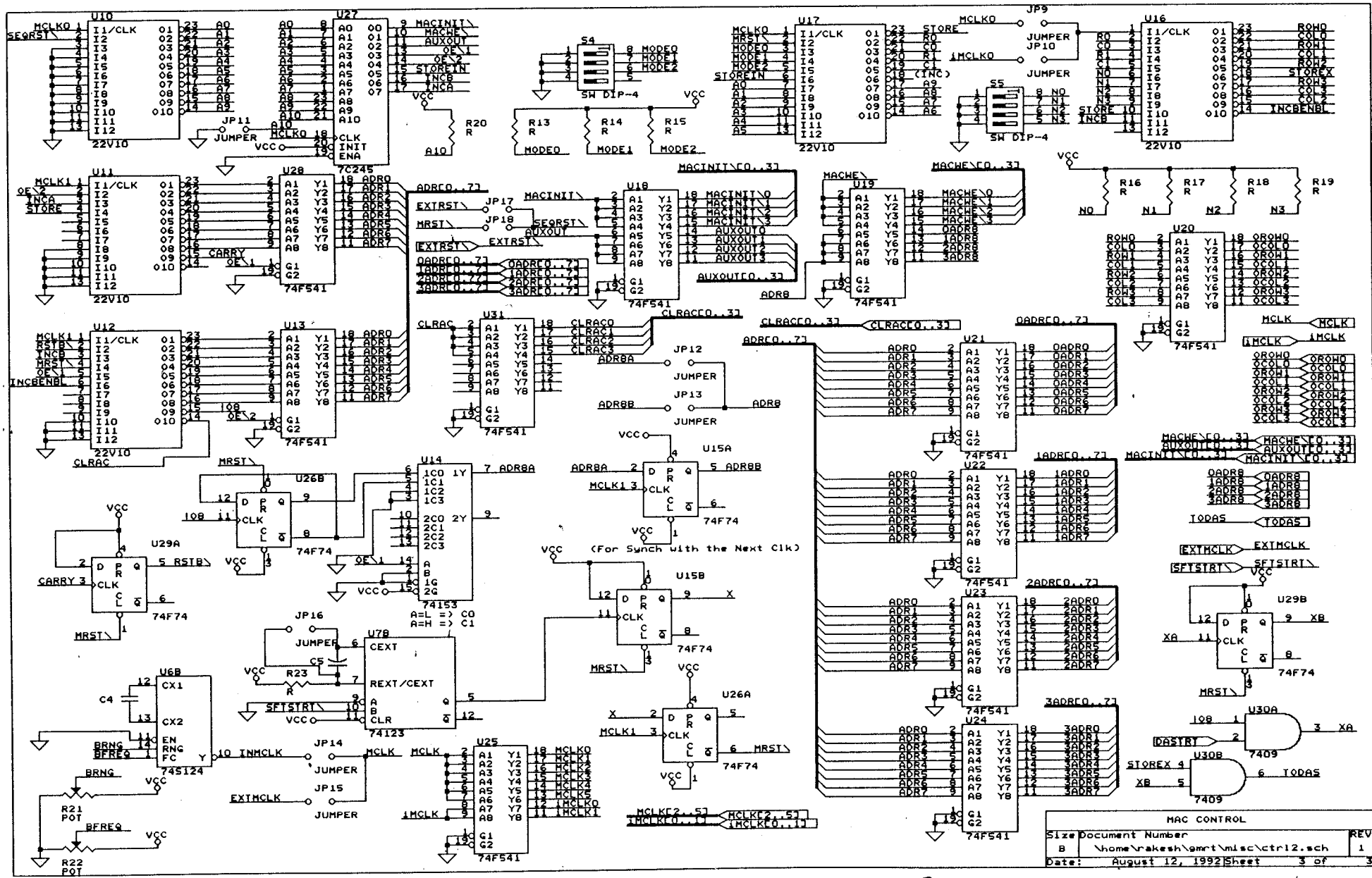
1. R.K.Malik, *" Control Word Loading in the FX-ASIC"*, rkm6/CTRL/july92.

2. R.K.Malik, *" Software Simulator for the ASIC (MAC Mode)"*, rkm9/MACSIM/sept92.


P1A
P1B
P1C
DIN
CTRL2.SCH
CTRL1.SCH
P2
U?
74F574
U32A
U32B
74F74
JP32
JP33
JP34
JP35
JP36
JP37
JUMPER
MAC CONTROL (Top Level)
Size A
Document Number \home\rakesh\gmrt\misc\mactrl\ctrl0.
REV
Date: September 6, 1992
Sheet 1 of 3



U7A
CEXT
REXT/CEXT
C1
100uf
R1
15k
VCC
TRIGGER
A
B
CLR
Q
74123
EXTRGR
MCLK
EXTSCLK
CRSI
SFTSTRT\
iMCLK
CRSTB[0..3]
SFTCLK[0..3]
S1
SW PUSHBUTTON
U8A
U8B
D
PR
CLK
CL
7474
SCLK
RST\
MANUAL
R2
R
C2
CAP
ARNG
AFREQ
R11
R12
U1B
CRSTB
iSCLK
CRSTB'
JP7
JP8
U5
ADR0
ADR1
ADR2
ADR3
ADR4
ADR5
ADR6
SR5
SR6
SR7
SR8
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
O0
O1
O2
O3
O4
O5
O6
O7
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
(SCLK)
INIT
ENA
7C245
S3
SW DIP-4
JP5
JP6
U6A
C3
CX1
CX2
EN
RNG
FC
Y
INSCLK
74S124
JP3
JP4
JUMPER
U1A
74F74
LDEND\
SFTSTRT\
S2
SR1
SR2
SR3
SR4
(No. of ASICs)
(Max = 16)
U4
I1/CLK
S0
22V10
U2
SH/LD\
INH
(CNT0)
(CNT1)
(CNT2)
(CNT3)
SFTCLK
U9
CRSTB0
CRSTB1
CRSTB2
CRSTB3
SFTCLK0
SFTCLK1
SFTCLK2
SFTCLK3
CRSTBA
G1
G2
74F541
JP1
JP2
R3
R4
R5
R6
R7
R8
R9
R10
U3
SER
QH
74F166
MAC CONTROL (Control Word)
Size
A
Document Number
\home\rakesh\gmrt\misc\mactrl\ctrl1.
REV
Date: September 6, 1992
Sheet 2 of 3


MAC CONTROL
Size B
Document Number \home\rakesh\smrt\misc\ctrl2.sch
REV 1
Date: August 12, 1992
Sheet 3 of 3

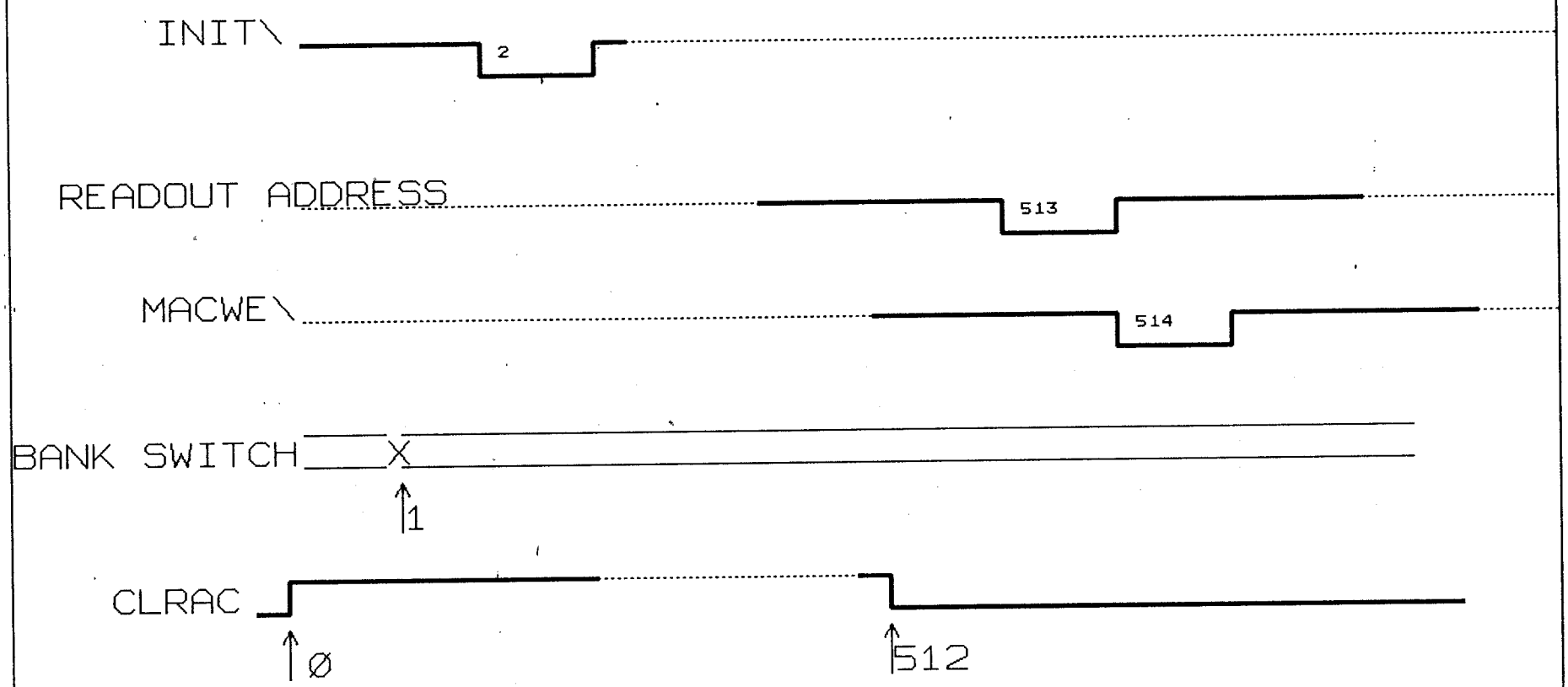


fig 1.

CRITICAL MAC TIMINGS		
Size A	Document Number \home\rakesh\gmrt\misc\mactrl\ctrl.t	REV
Date: September 6, 1992	Sheet of	

```
"/home/rakesh/gmrt/misc/mactrl/pal/U10.ABL"

module GAL_U10
title '516-clock Sequencer'

        U10     device                  'P22V10' ;

"INPUTS : "

        CLK                 PIN 1;
        RST                 PIN 2 ;

"OUTPUTS: "
        CNT0                PIN 23 ;
        CNT1                PIN 22 ;
        CNT2                PIN 21 ;
        CNT3                PIN 20 ;
        CNT4                PIN 19 ;
        CNT5                PIN 18 ;
        CNT6                PIN 17 ;
        CNT7                PIN 16 ;
        CNT8                PIN 15 ;
        CNT9                PIN 14 ;

"DEFINITIONS:"

        COUNT = [CNT9,CNT8,CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0] ;

"EQUATIONS :"

equations

WHEN (COUNT < 515) THEN COUNT := (COUNT + 1) & RST;

ELSE COUNT := 0;

end GAL_U10
```

```
"/home/rakesh/gmrt/misc/mactrl/pal/U11.ABL"

module GAL_U11
title 'Integration Address Counter'

        U11     device                  'P22V10' ;

"INPUTS : "

        CLK                 PIN 1;
        RST                 PIN 2 ;
        INCA                PIN 3 ;
        STORE               PIN 4;

"OUTPUTS: "
        CNT0                PIN 23 ;
        CNT1                PIN 22 ;
        CNT2                PIN 21 ;
        CNT3                PIN 20 ;
        CNT4                PIN 19 ;
        CNT5                PIN 18 ;
        CNT6                PIN 17 ;
        CNT7                PIN 16 ;
        CARRY               PIN 15 ;
        BUFWE                PIN 14 ;

"DEFINITIONS:"

        COUNT = [CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0] ;
        BUFWE ISTYPE 'COM' ;

"EQUATIONS :"

equations

         COUNT := (COUNT + 1) & RST & INCA
                # COUNT & RST & !INCA    ;
       CARRY := (COUNT == 255) & RST & INCA ;
       !BUFWE=STORE & !CLK;

end GAL_U11
```

```
"/home/rakesh/gmrt/misc/mactrl/pal/U12.ABL"

module GAL_U12
title 'READOUT ADDRESS COUNTER '

        U12     device                  'P22V10' ;

"INPUTS : "

        CLK             PIN 1;
        RST             PIN 2 ;
        INCB            PIN 3 ;
        ARST            PIN 4;
        OE1             PIN 5 ;
        INCBENBL        PIN 6 ;

"OUTPUTS: "
        !CNT0            PIN 23 ;
        !CNT1            PIN 22 ;
        !CNT2            PIN 21 ;
        !CNT3            PIN 20 ;
        !CNT4            PIN 19 ;
        !CNT5            PIN 18 ;
        !CNT6            PIN 17 ;
        !CNT7            PIN 16 ;
        BANK            PIN 15 ;
        CLRAC               PIN 14 ;
"DEFINITIONS:"

        COUNT = [CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0] ;
        BANK ISTYPE 'COM' ;
        CLRAC ISTYPE 'COM';

"EQUATIONS :"

equations

         COUNT := (COUNT + 1) & RST & INCB & INCBENBL
                # COUNT & RST & !INCBENBL
                # COUNT & RST & !INCB   ;
        BANK = !CNT7 & RST ;

        CLRAC = (COUNT == 0) & !OE1 & ARST  ;

end GAL_U12
```

```
ome/rakesh/gmrt/misc/mactrl/pal/U16.ABL"

ule GAL_U16
le 'ROW\-COL\ Decoding and Suppression of Dummy Readouts '

     U16    device              'P22V10' ;

PUTS : "

     R0              PIN 2;
     C0              PIN 3;
     R1             PIN 4;
     C1            PIN 5;
     N0               PIN 6;
     N1               PIN 7;
     N2               PIN 8;
     N3               PIN 9;
     STORE            PIN 10;
     INCB             PIN 11;

TPUTS: "
     ROW0             PIN 23 ;
     COL0             PIN 22 ;
     ROW1             PIN 21 ;
     COL1             PIN 20 ;
     ROW2             PIN 19 ;
     STOREOUT         PIN 18 ;
     ROW3             PIN 17 ;
     COL3             PIN 16 ;
     COL2             PIN 15 ;
     INCBENBL         PIN 14 ;

FINITIONS:"
     NASIC=[N3,N2,N1,N0];
     ASIC=[C1,R1,C0,R0];
     ROW0 ISTYPE 'COM';
     ROW1 ISTYPE 'COM';
     ROW2 ISTYPE 'COM';
     ROW3 ISTYPE 'COM';
     COL0 ISTYPE 'COM';
     COL1 ISTYPE 'COM';
     COL2 ISTYPE 'COM';
     COL3 ISTYPE 'COM';
     INCBENBL ISTYPE 'COM';

QUATIONS :"

uations
     !ROW0 = ( ASIC < 4 ) & ( NASIC >= 0 );
     !ROW1 = ( ASIC>= 4) & (ASIC < 8) & (NASIC >=4);
     !ROW2 = ( ASIC>= 8) & (ASIC < 12) & (NASIC >=8);
     !ROW3 = ( ASIC>= 12) & (ASIC < 16) & (NASIC >=12);

     !COL0 = ( ASIC==0) & (NASIC>=0)
             # (ASIC==4) & (NASIC>=4)
             # (ASIC==8) & (NASIC>=8)
             # (ASIC==12) & (NASIC>=12);

     !COL1 = ( ASIC==1) & (NASIC>=1)
             # (ASIC==5) & (NASIC>=5)
             # (ASIC==9) & (NASIC>=9)
             # (ASIC==13) & (NASIC>=13);

     !COL2 = ( ASIC==2) & (NASIC>=2)
             # (ASIC==6) & (NASIC>=6)
             # (ASIC==10) & (NASIC>=10)
             # (ASIC==14) & (NASIC>=14);

     !COL3 = ( ASIC==3) & (NASIC>=3)
             # (ASIC==7) & (NASIC>=7)
             # (ASIC==11) & (NASIC>=11)
             # (ASIC==15) & (NASIC>=15);

     STOREOUT:=STORE & (ASIC<=NASIC);
     INCBENBL=(ASIC==0) ;

d GAL_U16
```

```
ome/rakesh/gmrt/misc/mactrl/pal/U17.ABL "
ule GAL_U17
le 'Selection of the Number of Accumulations'

     U17    device                'P22V10' ;

PUTS : "

     CLK              PIN 1;
     RST              PIN 2 ;
     MODE0            PIN 3 ;
     MODE1            PIN 4;
     MODE2            PIN 5;
     STOREIN          PIN 6;
     A0               PIN 7;
     A1               PIN 8;
     A2               PIN 9;
     A3               PIN 10;
     A4               PIN 11;
     A5               PIN 13;
     A6               PIN 14;
     A7               PIN 15;
     A8               PIN 16;

TPUTS: "
     STORE           PIN 23;
     R0               PIN 22;
     C0               PIN 21;
     R1               PIN 20;
     C1               PIN 19;
     INC             PIN 18;

EFINITIONS:"
     C=.C.;

     MODE  = [MODE2,MODE1,MODE0];
     COUNT = [A8,A7,A6,A5,A4,A3,A2,A1,A0] ;
     CNT=[A4,A3,A2,A1,A0];
     STORENBL=[A8,A7,A6,A5];
     ASIC=[C1,R1,C0,R0];

RE ISTYPE 'COM' ;

UATIONS :"

ations

.C=CLK;

     INC  :=   RST & (CNT==4)
             & (((!MODE0 & !MODE1 & !MODE2)
                #(MODE0 & !MODE1 & !MODE2 & !A5)
                #(!MODE0 & MODE1 & !MODE2 & !A5 & !A6)
                #(MODE0 & MODE1 & !MODE2 & !A5 & !A6 & !A7)
                #(!MODE0 & !MODE1 & MODE2 & !A5 & !A6 & !A7 & !A8)) ;

     ASIC:= (ASIC+1) & RST & INC
             # ASIC & RST & ! INC ;

RE  =  STOREIN & RST & (MODE == 4) & !A8 & !A7 & !A6 & !A5
     # STOREIN & RST & (MODE == 3) & !A7 & !A6 & !A5
     # STOREIN & RST & (MODE == 2) & !A6 & !A5
     # STOREIN & RST & (MODE == 1) & !A5
     # STOREIN & RST & (MODE == 0) ;
```

```
************************************************************************
DATA FILE FOR U27. ("/home/rakesh/gmrt/misc/mactrl/rom/MAC.DAT")
************************************************************************

 $A0000,
17 B7 12 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93

$A0080,
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93

$A0100,
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93

$A0180,
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93
17 B7 13 B3 13 93 13 93 13 93 13 93 13 93 13 93
13 93 13 93 13 93 13 93 13 93 13 93 13 93 13 93

$A0200,
0B 0B 09 4B 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
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