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ref : rkm8/FFT/aug92

Aug 5, 1992

FFT IMPLEMENTATION IN HARDWARE WITH FX-ASICs

(ALGORITHM)

INTRODUCTION: 512 Point FFT Algorithm that we are going to implement with the NRAO FX-ASICs is given here.

REQUIREMENTS: The conventional DFT Formula can be manipulated in many possible ways to implement FFT. However, the primary requirement for us is to make it compatible with the ASIC Chip Architecture. As has already been pointed out quite often, the ASIC can perform either RADIX-2 or RADIX-4 FFT and it operates on 4-Complex input numbers simultaneously. Therefore we are cascading 5-ASICs to perform 512-point FFT with the Chips configured in the following sequence:

Radix-4, Radix-4, Radix-4, Radix-4, Radix-2

The details are worked out in the following section.

ALGORITHM: Consider the conventional DFT expression for 512-Point Fourier Transform –

$$F(k) = \Sigma_{n=0}^{n=511} f(n) W_{512}^{nk} \text{ —— [1]}, \qquad k = (0,1.....511)\ ; \quad (W_N^{ab} = e^{-j\frac{2\pi}{N}ab})$$

With a little effort one can easily see that if one writes :

$$n = 128r + 32s + 8t + 2u + v$$

$$k = a + 4b + 16c + 64d + 256e$$

[1] can be written in the form —

$$F(a+4b+16c+64d+256e) = [\{\Sigma_v[\{\Sigma_u[\{\Sigma_t[\{\Sigma_s[\{\Sigma_r f(128r + 32s + 8t + 2u + v) W_4^{ra}\} W_{16}^{sa}] W_4^{sb}\} W_{64}^{(a+4b)t}]. W_4^{tc}\} W_{256}^{(a+4b+16c)u}] W_4^{ud}\} W_{512}^{(a+4b+16c+64d)v}] W_2^{ve}\} \text{ —— [2]}$$

where

$$r,s,t,u = (0,1,2,3);\ v = (0,1);$$

$$a,b,c,d = (0,1,2,3);\ e = (0,1);$$

Each of the five Σ's corresponds to one of the stages in the cascaded ASIC Pipeline. In each stage, the ASIC performs Radix-4 or Radix-2 FFT as the case may be but from [2] it is clear that some other multiplicative factors (underlined one's) —- called Twiddle Factors — are also required at each stage before performing Radix-4(or 2) FFT in the chip (there is no Twiddle Factor at Stage-0 as is obvious from [2]).

Appendix A gives the address generation sequences for various stages.

COMMENTS: One must check up with CRS for the exact Twiddle Factors Bit Patterns.

ACKNOWLEDGEMENTS: I thank CRS for going through some of the details mentioned herein.

REFERENCES:

1. VLBA1 SCHEMATIC, 84 PAGES TOTAL

2. Brigham, "Fast Fourier Transform and its Applications".

APPENDIX-A

BIT ORDER FOR VARIOUS STAGES:

INTERNAL ADDRESSES: Internal 9-Bit Address Counters have their bits arranged as in the following to generate Address Sequences .

STAGE 0 — 8 7 6 5 4 3 2 0 1

STAGE 1 — 8 7 6 5 4 0 1 3 2

STAGE 2 — 8 7 6 0 1 5 4 3 2

STAGE 3 — 8 0 1 7 6 5 4 3 2

STAGE 4 — 1 8 7 6 5 4 3 2 0