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ref: rkm5/DAQ/july92

July 20, 1992

## DATA-ACQUSITION SYSTEM FOR DEBUGGING CORRELATOR HARDWARE

ABSTRACT: For debugging any FX ASIC based hardware, a need was felt to have a Data-Acquisition System which would be compatible with the format in which one gets output from the ASIC and then store the data on to a PC Hard-Disk for further analysis later on in order to verify the hardware – be it FFT or MAC – and fine tune it accordingly. To meet this requirement, since otherwise it was not at all possible to monitor 16-18 output bits simultaneously on an Oscilloscope, a Data Acquisition card was built around the 8251 USART Chip to provide a temporary memory-buffer for the ASIC output and then transfers the data to a PC on a Simplex Serial-Link. The serial-link has been successfully used at a band rate of 9.6k.

**REQUIREMENTS:** Output of the ASIC is in the form of 18-bits. For debugging the Hardware, its necessary to have available the bit-pattern that appears at the output with each clock-edge. Even after leaving the 2 LSB's, the Data-Acquistion has to have the capability of accepting 16-Bits simultaneously.

Moreover, after acquiring the data, one would also like to search for any repetitive error patterns in the output and that requires the memory buffer to have sufficient depth to store o/p's of a few FFT Cycles in one go.

IMPLEMENTATION: Keeping these requirements in mind, the circuit which has been implemented consists of two 7C185 RAMs in parallel which provide a buffer size of (8k X 16). Chip 8251 provides a Simplex Serial interface with a PC. 8k data points of width 16 each get written into this buffer and after that 8251 transfers the data to a PC – one Byte at a time. IC 1488 Driver Chip provides necessary output voltage levels for RS232 interface.

Necessary intelligence required in the circuit to generate various control signals has been implemented

in GAL22V10 and PAL16L8. This includes, among other things, logic to load Mode Word and Command word to initialize 8251, selection of appropriate clock etc.

Mode-word and the Command-word can be set through two 8-bit DIP Switches available on the board. For this Simplex link, one has to load these two Bytes only once.

Address generator for the RAM's has been implemented in EPLD - EPM5032D which we had got from RRI.

**OPERATION:** Each data-acquisition sequence starts with pressing a Push-Button on the board. This initializes various components to a known initial state, RESETs 8251, loads Mode and Command Words in this sequence.

For 16-bit data to get written to the RAM, the users should provide an active-low WE pulse of minimum 20ns duration after the data to be input is stable.

Once the 8k X 16 buffer is filled, all further Write operations are disabled and 8251 reads one Byte at a time and sends it to the PC bit by bit.

INSTRUCTIONS FOR USERS: A user needs to be aware of the following things only:

- (i) Location of the Push-Button: since there is only one on the board, it would be extremely difficult to miss that.
- (ii)Data Inputs: 16 data inputs can be used by plugging in 16-single-strand wires into the Single Inline Sockets made available on the board. They are numbered D0 to D15 from left to right.
- (iii) WE Input: this must be plugged in at the pin-2 of PAL 16L8 (ref. USART15).
- (iv) Output: Serial output is available on a 25pin D-Type connector which must be connected to a PC.
- (v) An active Low RST pulse which starts the operation is available for any usage OFF the CARD.
- (v) Location of the Board itself: any Correlator-Group person may be contacted for that.

## Encl.:

(i) OrCAD Schematic

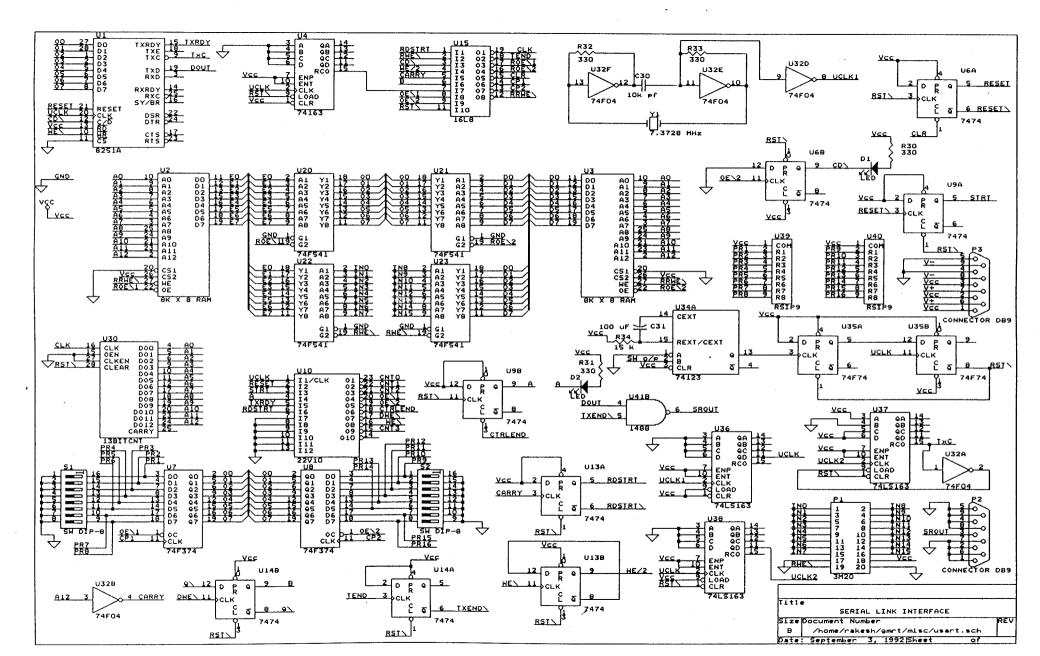
(ii) ABEL Program for PAL 16L8

(iii) ABEL Program for GAL 22V10

(Note: The Schematic was updated to include connectors etc also in order to make a proper PCB.

Acquisition System and these few later additions may be ignored for the General Purpose Board which is presently available in the Lab)

Acknowledgements: Thanks to Madhura for providing her acquisition Program. Datta's and Vivek's involvement in design/debugging is also acknowledged. Many many thanks to Rajendran for wiring the PCB.



```
USRT10
                   device
                                         'P22V10';
 "INPUTS : "
         CLK
                         PIN 1;
         RESET
                         PIN 2 ;
                                   "Active High"
         STRT
                         PIN 3;
         Α
                         PIN 4;
         TXRDY
                         PIN 5;
         RDSTRT
                         PIN 6;
         WE
                         PIN 7;
                                   Active Low"
 "OUTPUTS: "
         CNTO
                         PIN 23 ;
         CNT1
                         PIN 22 ;
         CNT2
                         PIN 21 :
         OE1
                         PIN 20 ;
         OE2
                         PIN 19 ;
         CTRLEND
                        PIN 18 ;
        DWE
                        PIN 17 :
        WE
                        PIN 16 ;
        CNT3
                        PIN 15 ;
"DEFINITIONS:"
COUNT = [CNT3, CNT2, CNT1, CNT0];
"EQUATIONS :"
equations
[CNT3, CNT2, CNT1, CNT0].CLK = CLK;
OE1.CLK = CLK;
OE2.CLK = CLK;
CTRLEND.CLK = CLK;
WE.CLK = CLK;
DWE.CLK = CLK;
COUNT := (COUNT + 1) & !RESET & A;
     := STRT & (COUNT < 3) & A & !RESET ;
     := STRT & A & !RESET & ( COUNT>8) & (COUNT<12);
!CTRLEND := (COUNT == 13);
          !OE1 & (COUNT==1) & !RESET
        # !OE2 & (COUNT ==10 ) & !RESET
        # TXRDY & (WE==1) & RDSTRT & !RESET;
!DWE := !WE & !RESET;
"TEST VECTORS :"
test vectors
                ([CLK,STRT,RESET,A,COUNT] -> [COUNT,OE1,OE2,CTRLEND,WE])
                 [.c., 0 , 1
                               ,.x.,.x.] -> [
                                                0,1,1,1
                                                                   , 1];
                       1,
                 [.c.,
                             0
                                ,1, 0 ] -> [
                                                 1,0,
                                                          1, 1
                                                                   , 1];
                       1 ,
                 [.c.,
                            0
                               ,1, 1 ] -> [
                                                 2,0,
                                                          1, 1
                                                                   , 0];
                 [.c., 1, 0
                                   2
                                ,1,
                                        ] -> [
                                                 3,0,
                                                          1, 1
                                                                   , 1];
                 [.c., 1, 0]
                                ,1, 3
                                       ] -> [
                                                 4 , 1 ,
                                                          1, 1
                                                                     1]
                 [.c.,
                       1,0
                               ,1, 4
                                        ] -> [
                                                 5,1,
                                                          1, 1
                                                                     1]
                      1,
                 [.c.,
                            0
                               ,1,
                                        ] -> [
                                    5
                                                          1, 1
                                                                    1];
```

JSRT10

erīal Link Interface'

```
,1,
                                                                , 1];
                [.c., 1, 0, 1, 8] \rightarrow [ 9, 1, 1, 1
                                                                , 1];
               ...[.C.,
                     1, 0,1, 9 ] -> [
                                             10 , 1 , 0, 1
                                                                , 1];
                [.c.,
                           0 ,1, 10 ] -> [ 11 , 1 ,
                                                                , 0];
                                                       0, 1
                [.c.,
                           0 ,1, 11 ] -> [ 12 , 1 ,
                                                       0, 1
                                                                , 1];
                [.c., 1, 0, 1, 12] \rightarrow [ 13, 1, 1, 1
                                                                , 1];
                     1 , 0 ,0, 13 ] -> [ 0 , 1 , 1, 0
                [.c.,
                                                                , 1];
                              ,0, .x. ] \rightarrow [ 0, 1,
                                                                , 1];
test vectors
               ([CLK,OE1,OE2,TXRDY,RDSTRT,WE] -> [WE])
                [.c., 0 , 1 , 1 , 1 ,
                                      0] -> [0] ;
                [.C., 1, 1, 1, 1, 1, 0] \rightarrow [1];
                [.c., 0, 1, 1, 1, 1] \rightarrow [0];
                [.c., 1 , 0 , 1 , 1 ,
                                      1] -> [1];
                [.C., 1, 1, 0, 1, .X.] \rightarrow [1];
                [.c., 1, 0, 1, 0]
                                     1] -> [1];
end GAL USRT10
```

```
Fol Logic for Serial Interface!
         USRT15
                device
                                           'P16L8';
  PUTS : "
         RDSTRT
                          PIN 1;
         RWE
                          PIN 2;
         CD
                          PIN 3;
         WE2
                          PIN 4;
         CARRY
                          PIN 5;
         В
                          PIN 6;
        NCLR
                          PIN 7;
         OE1
                          PIN 8;
         OE2
                          PIN 9;
        RST
                          PIN 11;
"OUTPUTS: "
        CLK
                          PIN 19 ;
        TEND
                          PIN 18 ;
        ROE1
                          PIN 17 ;
        ROE2
                         PIN 16
        CLR
                          PIN 15
        CP1
                          PIN 14 :
        CP2
                         PIN 13 ;
        RRWE
                         PIN 12 ;
"EQUATIONS :"
equations
        CLK = (!CD & WE2 & RDSTRT & RST) # (RWE & !RDSTRT & RST) ;
        TEND = CARRY & RDSTRT ;
        ROE1 = B \# !RDSTRT ;
        ROE2 = !B # !RDSTRT ;
        CLR = !NCLR;
        CP1 = !OE1;
        CP2 = !OE2;
       !RRWE= !RWE & !RDSTRT ;
"TEST VECTORS:"
test vectors ([RDSTRT,RWE,CD,WE2,RST] -> [CLK])
                0 ]
                       , 1, X., X., 1  -> [1];
                       , 0 ,.X.,.X., 1 ] -> [0];
                 0
                [ 1
                       , .X., 0 , 1 , 1 ] \rightarrow [1];
                       , X., 0, , 0, 1 ] \rightarrow [0];
                  1
                ſ.X.
                       , X., X., X., 0  -> [0];
end PAL USRT15
```