National Centre for Radio Astrophysics

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Technical Report on
Radio Frequency Control and Monitoring Module
(RFCM Card)

BY

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Giant Metrewave Radio Telescope,

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We are very much thankful for all those who helped in completing the assignment successfully. We wish to express our sincere gratitude to all our front-end colleagues.

Abstract

The purpose of this report is to re-design the Radio Frequency Control and Monitoring Module and to make this card unified for all the frequency bands of GMRT. Presently two versions of RFCM card are being used in GMRT Front-End systems. 50 MHz, 150 MHz, 233 MHz, 325 MHz and 610 MHz Front-End boxes have similar RFCM card whereas RFCM for the L-band is different from the above mentioned GMRT bands. It has additional provision of filter selection and monitoring in it. This report describes the functionality of RFCM card and covers the design of the RFCM card along with its entire functionality, application in GMRT front end system and design details.

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1. Introduction:

Giant Meter wave Radio Telescope (GMRT) has been designed to operate at six frequency bands centred at 50 MHz, 150 MHz, 235 MHz, 327 MHz, 610 MHz, and L-Band extending from 1000 MHz to 1450 MHz. The L-band further split into four sub-bands centred at 1060 MHz, 1170 MHz, 1280 MHz and 1390 MHz, each with bandwidth of 120 MHz. The 150 MHz, 235 MHz and 327 MHz bands have about 40 MHz bandwidth and 610 MHz band has a bandwidth of 60 MHz. Lower frequency bands from 150 MHz to 610 MHz have dual circular polarization channels (Right Hand Circular and Left Hand Circular) which have been conveniently named as CH1 and CH2 respectively.

The RFCM card used in the front-end boxes is for controlling various functionalities and monitoring of various parameters for these particular front-end systems. Each FE-Box has its own dedicated RFCM card which is being controlled and monitored by the command sent from telescope control room on common bus (RS485) through the Monitoring and Control Module (MCM-5) card that sits in the common box in the front end system. At any given time only one front-end box i.e. only one frequency band is selected and rest of the front-end boxes are kept off. The basic functionalities of the RFCM card are RF on/off, Noise level selection, Walsh Switching, Filter Selection and providing supply voltages to different RF devices that sits in the respective front-end boxes.

The RFCM card was originally designed by M/S Raman Research Institute (RRI), Bangalore before more than 15 years. Unfortunately no details regarding schematic design, layout, etc. were available with the group. Even films required for PCB fabrication were not available. Therefore it was very difficult to maintain the front end systems with RFCM card failure. The spare cards were not enough to maintain five different front end systems on each of the 30 GMRT antennas. Therefore it was decided to go ahead with re-designing of the RFCM card and make it unified for the front end systems for all the GMRT bands. Also the new RFCM card is incorporated with the additional monitoring facility along with the TTL filter selection outputs.

2. Radio Frequency Control and Monitoring Card:

RFCM stands for Radio Frequency Control and Monitoring. It is basically a digital PCB used in each of the frontend boxes for control and monitoring purpose. It is used for controlling the various functionalities of the frontend box like RF on/off, Filter selection, Noise on/off and controlling the Noise level (Extra High Cal, High Cal, Medium Cal, and Low Cal). It is also used for monitoring the temperature and RF power level of each of the frontend boxes with the help of temperature sensors and RF power detector respectively.

RFCM card receives 8 bits of control data from the MCM-05 and generates 0V & -7V complimentary analog signals from these TTL inputs for driving the GaAs FET switches used for noise level settings, RF ON/OFF and filter select. Currently, the filter select option is utilized only for L-Band, but now in up-gradation of GMRT bands this facility of filter selection will be available in each band. The noise ON/OFF, Walsh function WF1 and WF2 are received through the MCM Interface card. The noise ON/OFF line is used as the control signal for the bits corresponding to the middle two switches (S2 & S3) in the noise generator. This is achieved through a combination of Ex-Or gates. The Walsh function data are level shifted to +/- 10 V for driving the mixer in the post amplifier. This New RFCM card is also incorporated with the monitoring facility. Eight monitoring points are available on the MUX IC. These monitoring points are used for monitoring the power and temperature of the each of the front-end boxes. Fig.1 shows various inputs and outputs on the RFCM card.
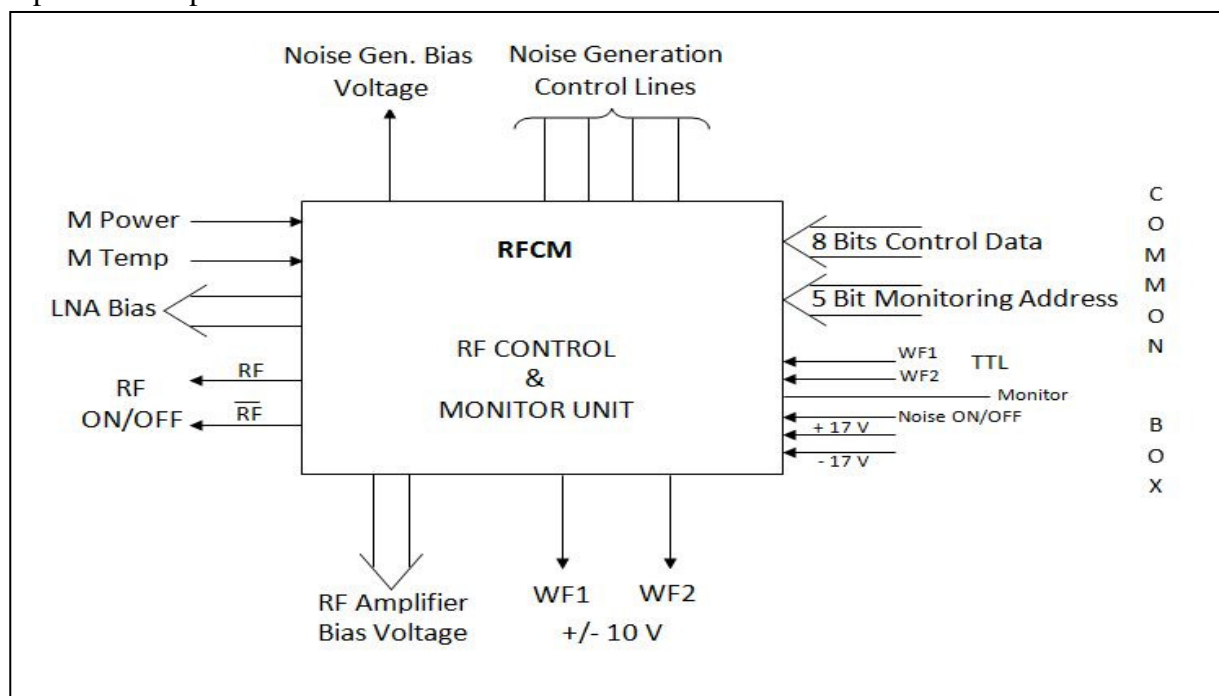

Fig.1 Inputs and Outputs of the RFCM cards

3. Schematic Diagram of RFCM card:

Fig.2 (a & b) shows the Schematic diagram of an Old RFCM card (Existing) and New RFCM card respectively. The RFCM card has a 25 pin input D-Type connector. The input for the RFCM card is received from the common box. As shown in the fig. 1 RFCM card receives the 8 bit data lines (D0-D7), 5 bits address lines (A0-A4), digital ground, noise ON/OFF, and Walsh switching bits (WF1 & WF2). The 8 bits data lines include 4 bits of noise selection (NS0-NS3), 2 bits of filter selection (FS0-FS1), one spare bit along with the RF ON/OFF bit. All these data bits are TTL inputs (0V & +5V) that are converted into -7V & 0V complementary analog signals with the help of a comparator IC (LM339) for controlling the GaAs FET switches. The Walsh function bits are level shifted from 0V/5V to +/- 10V using an op-amp (OP-37). The RFCM card also has a monitoring facility and it can monitor 8 external voltages (M1-M8) along with the other internal voltages. The two 16:1 multiplexer IC's (ADG506A) are used for this purpose and 5 bit address lines are used to select only one input at a time. Along with all these functionalities RFCM cards also provide power supply to the RF components that are present in the front-end box. For this it has four voltage regulators which convert +/- 17V into +/- 12V and +/- 5V.
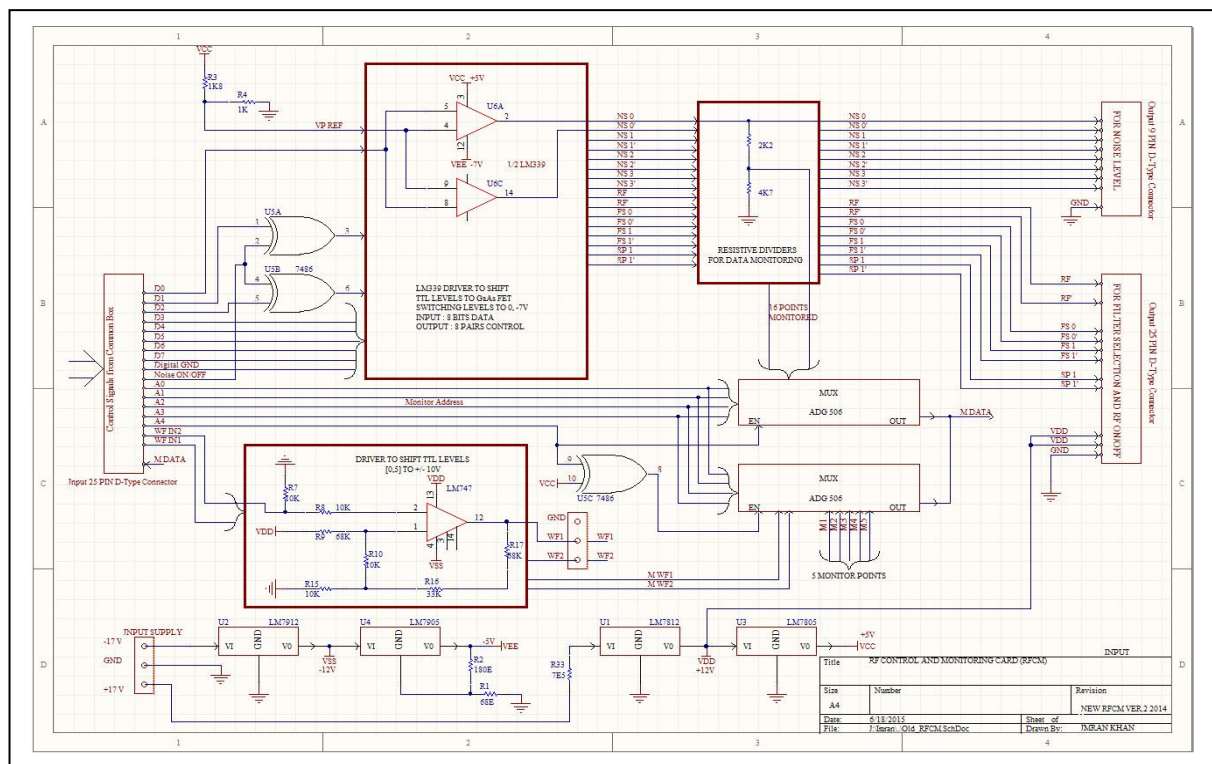
Fig.2 (a) Block Diagram of Old RFCM card (Existing)

The New RFCM card along with the following function explained earlier has additional 8 point monitoring facility along with the 3 TTL outputs (J11) for the filter selection. These two facilities have brought on the relemate connectors as shown in the schematic diagram of New RFCM card fig.2 (b).

TTL Outputs for Filter Selection
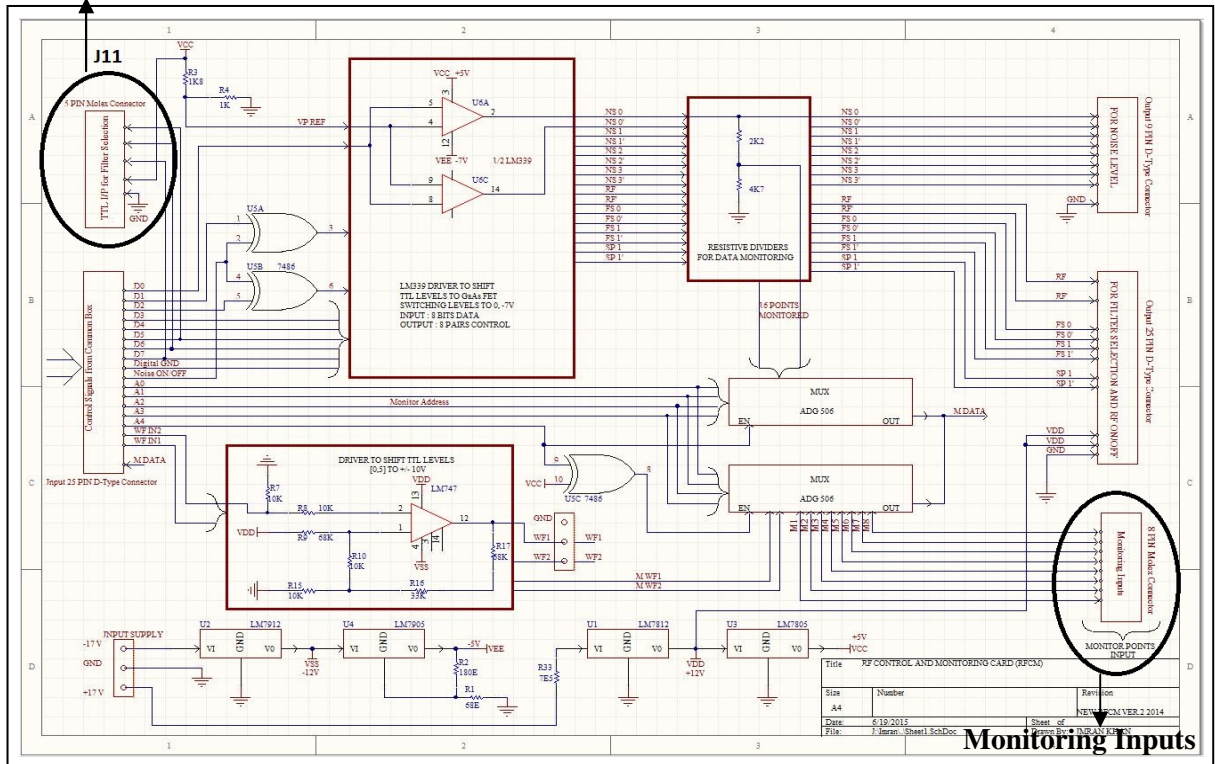
Fig.2 (b) Block Diagram of New RFCM card (Modified)

4. Re-Designing of RFCM card:

This section elaborates more about re-designing of the RFCM card. Complete reverse engineering was done to obtain the circuit schematic diagram from the available PCB for the existing RFCM card which is used in L-Band front end system for control and monitoring purpose and by thoroughly understanding the logic and signal flow. This was the toughest part in the entire designing process and we had to put lot of time and efforts to trace back the circuit successfully. Then the layout was designed using Altium PCB designing software.
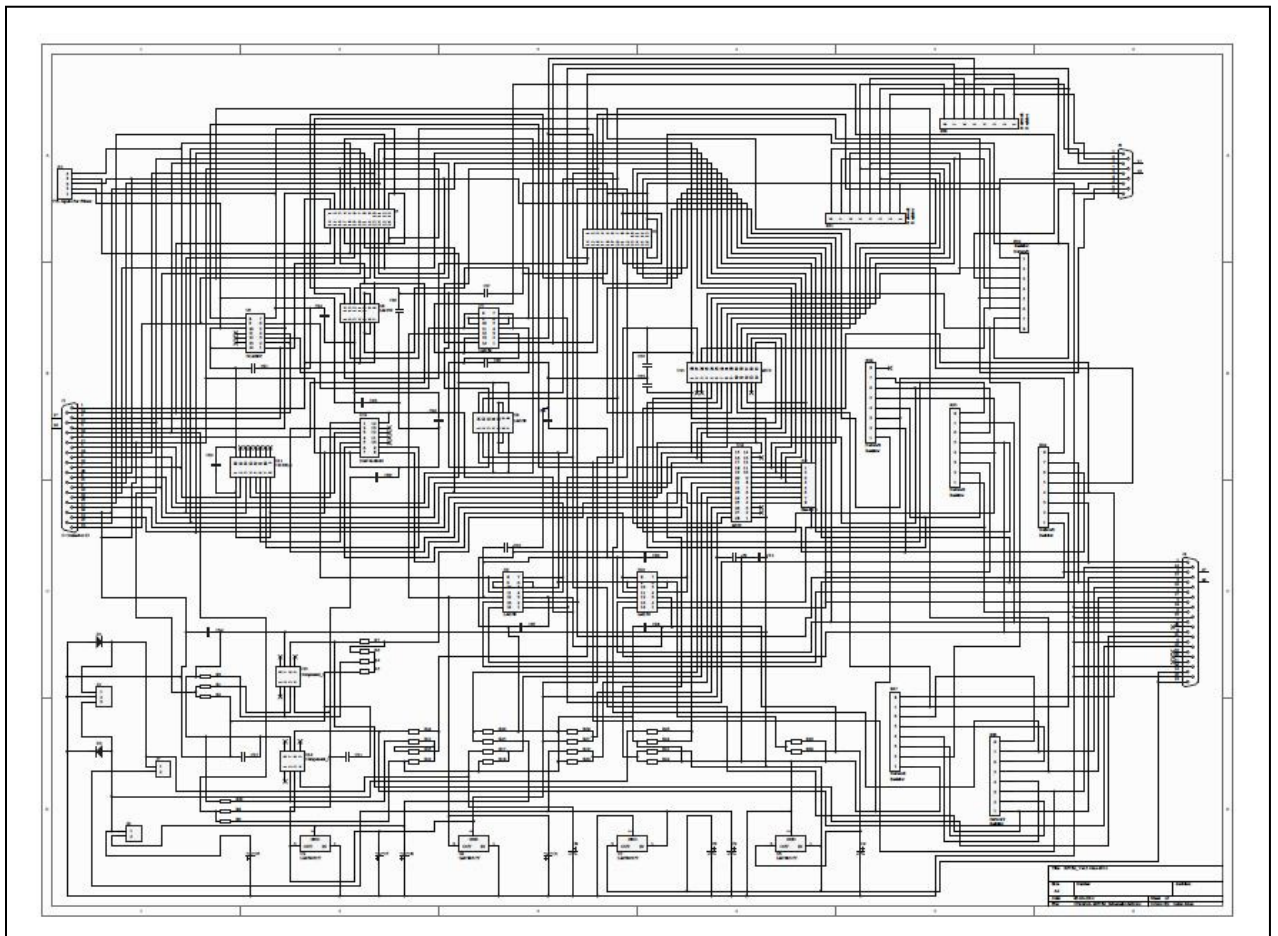
Fig.3 Schematic Diagram of RFCM card Ver.1

To start with the re-designing, first all point to point connections were traced from the existing PCB using a multi-meter in order to understand the signal flow. Using the datasheets for all the IC's on the board and the signal flow, the logic was verified at each and every pin on the IC's and I/O connectors. Based on this study a schematic was re-drawn using Altium Software as shown in fig.3. The schematic was analysed in detail for all the functionalities. Then the layout was designed by

importing this schematic into the PCB design studio in Altium. Proper footprints for some of the components that were not available in library were designed manually. Using appropriate track widths for Signal, Power and Ground connections the PCB design was completed. This was the first prototype called, RFCM Card Ver.1. Then the Gerber files were generated and sent to PCB manufacturer for fabrication. After receiving the PCB, the components were assembled on the card. The assembled card is shown below in fig. 4 (a & b).
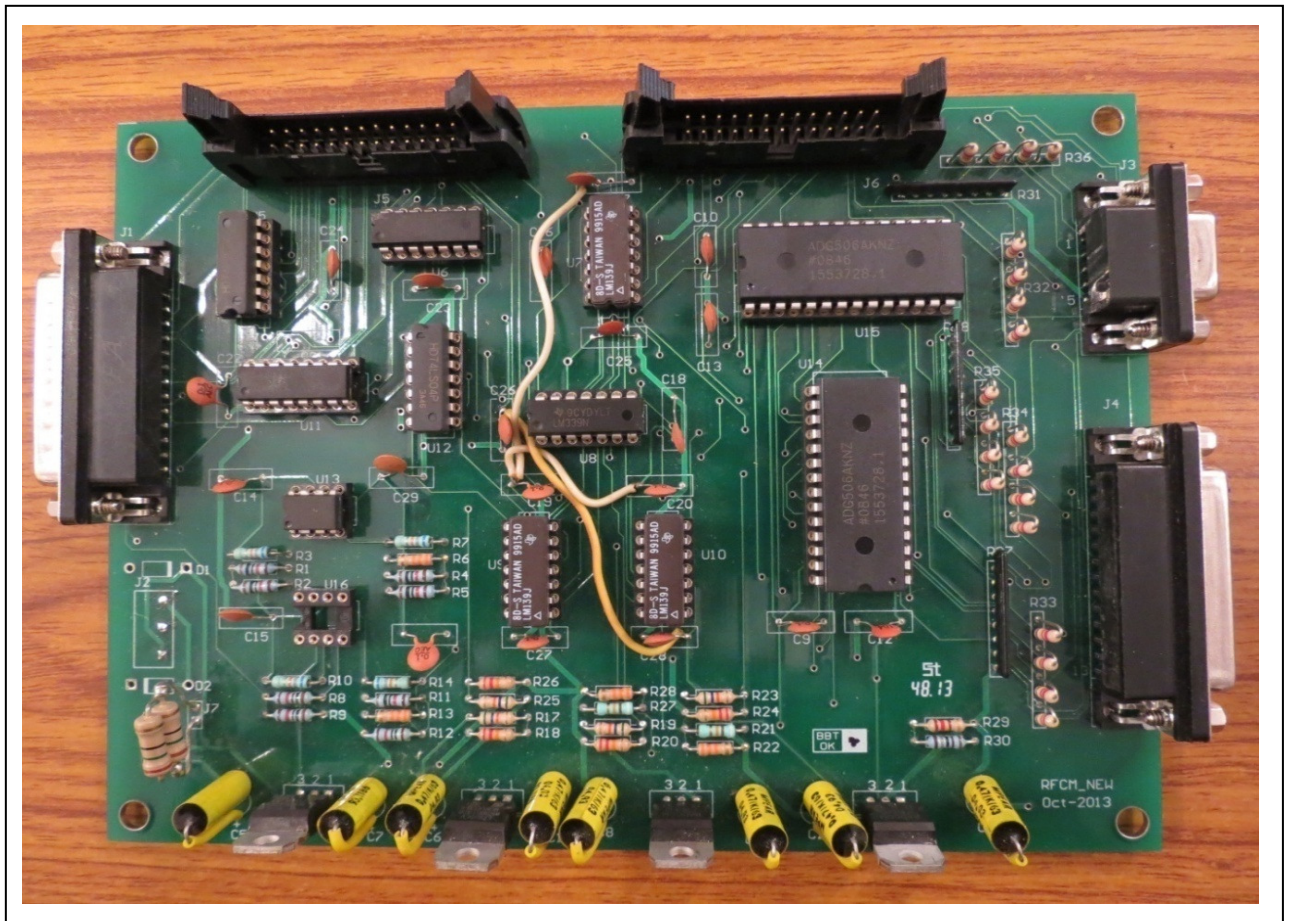
Fig.4 (a) Assembled RFCM card Ver.1 Top View.

The assembled card was tested in the lab for its complete functionality. During testing it was found that some of the connections are missing in the fabricated PCB. So jumpers were used for proper connectivity as shown in fig. 4 (a & b). With this modification the card was tested and found to be functioning properly.
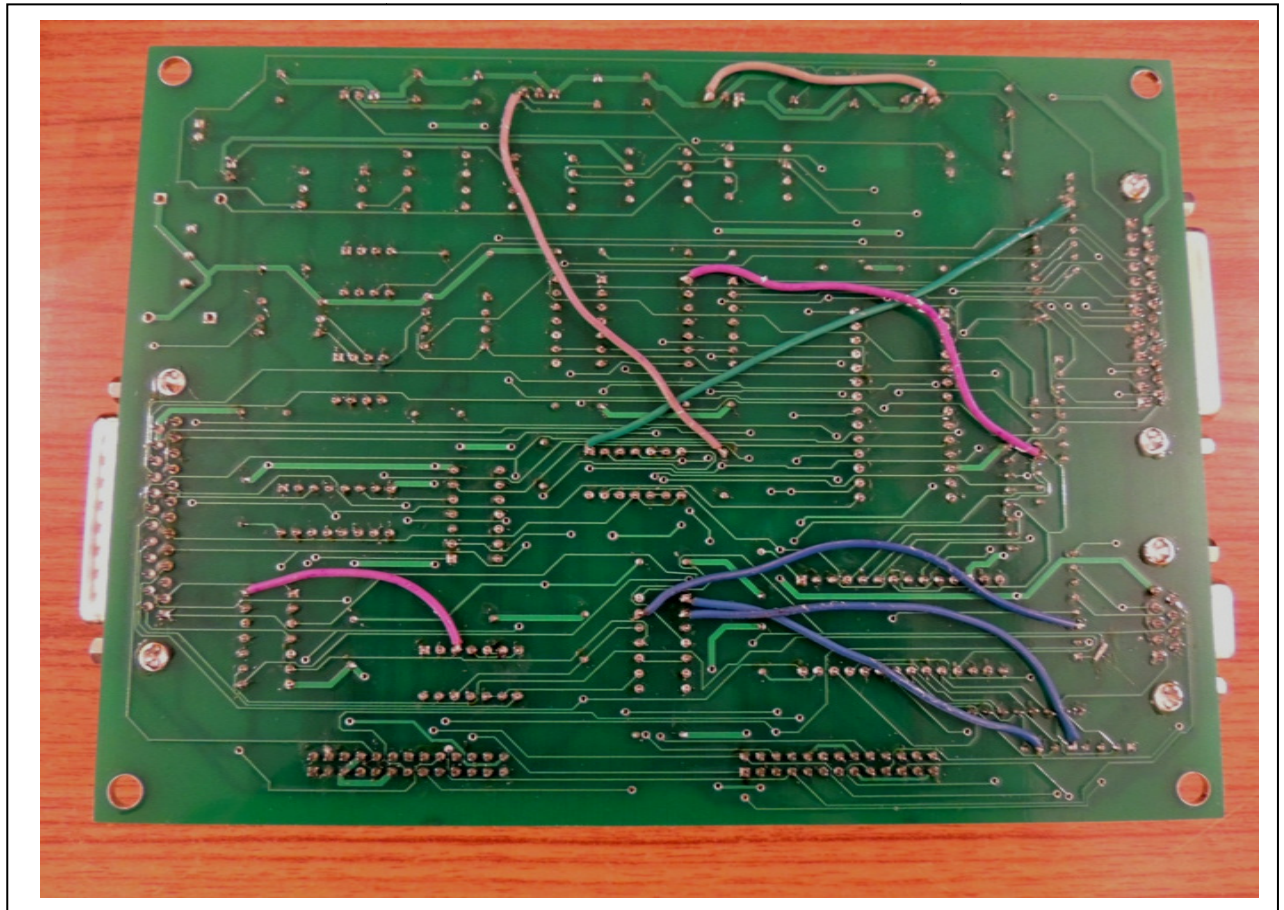
Fig.4 (b) Assembled RFCM card Ver.1 Bottom View.

Fig.5 shows the assembled RFCM Card Ver. 2. The card was found to be working satisfactorily for all the functionalities. But in this version of the card, only five monitoring points were available as spare to monitor five external inputs. These monitoring points had to be soldered directly on the multiplexer IC. Also, the card did not have provision for TTL inputs used for filter selection which is required in existing L band front end as well as other bands in upgraded GMRT. In order to overcome these shortcomings and to meet the requirement of upgraded GMRT, it was decided to modify this card to support all the existing front ends as well as upgraded GMRT front ends and have one unified control and monitoring card for all the GMRT front end systems.
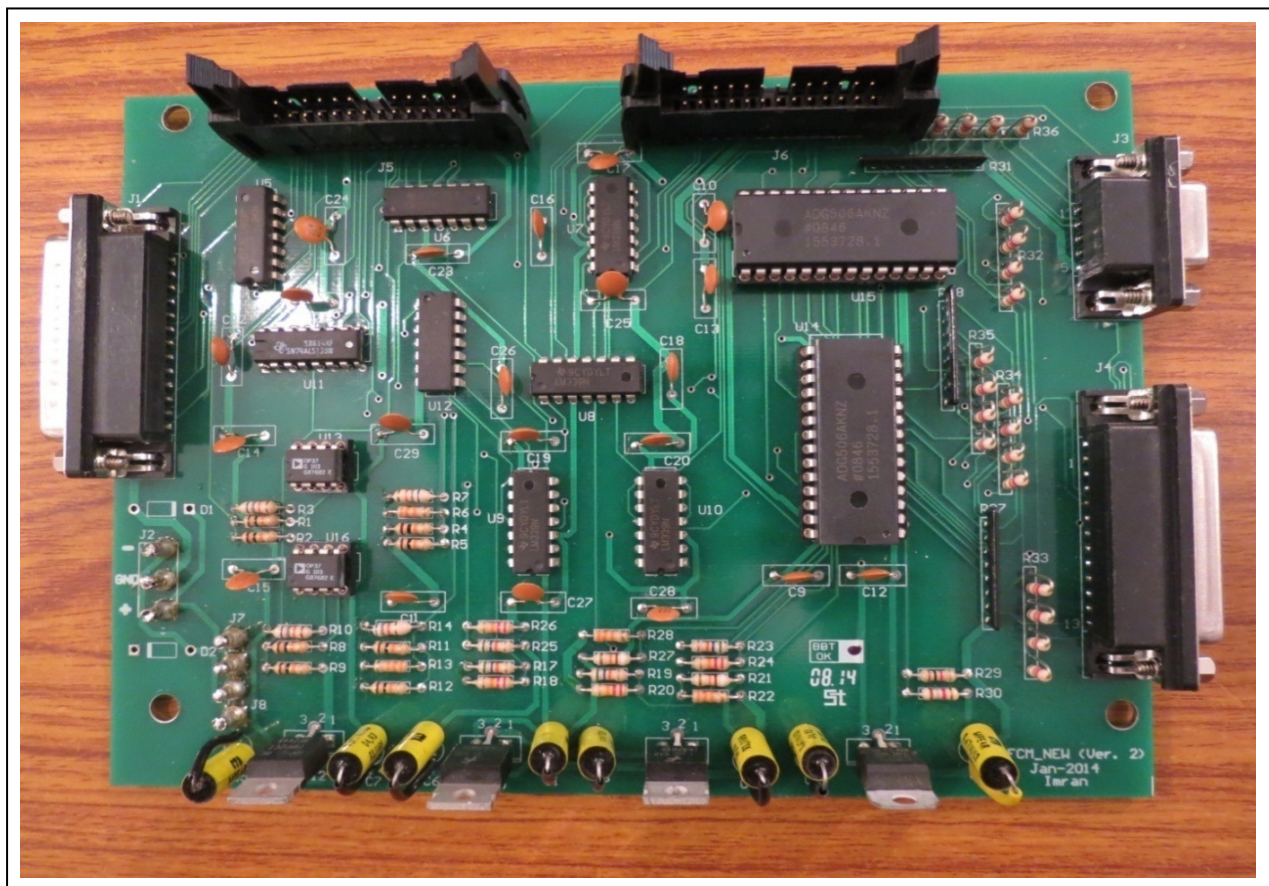
Fig.5 Assembled RFCM card Ver.2

The schematic and layout was modified to accommodate all the control and monitoring requirements of front end systems and the PCB was re-designed. This was the final version of the card, referred as RFCM Card Ver.3. This version of the card has 8 monitoring inputs and TTL inputs for filter selection. Provision was made to make all these control and monitoring points available on a 5 pin and 8 pin Jalex connector respectively.

The PCB was fabricated and then the card was assembled and tested thoroughly in lab for all the functionalities. It was found to work satisfactorily for all the GMRT front end systems, both old as well as upgraded. Fig. 6 shows the PCB layout of RFCM card Ver.3 and fig. 7 (a & b) shows the assembled RFCM Card Ver.3 along with the additional hardware added to the card.

TTL Outputs for Filter Selection
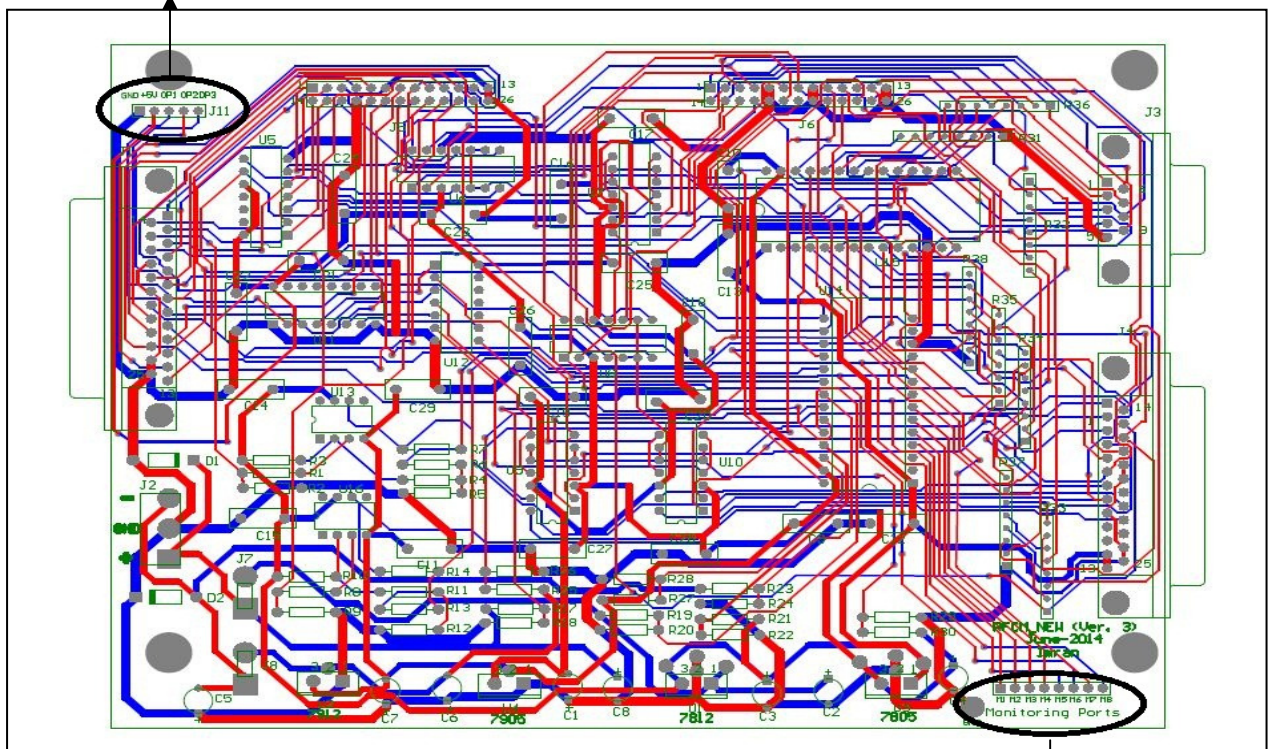
Fig.6 PCB layout of RFCM Card Ver.3.   **Monitoring Inputs**

TTL Outputs for Filter Selection
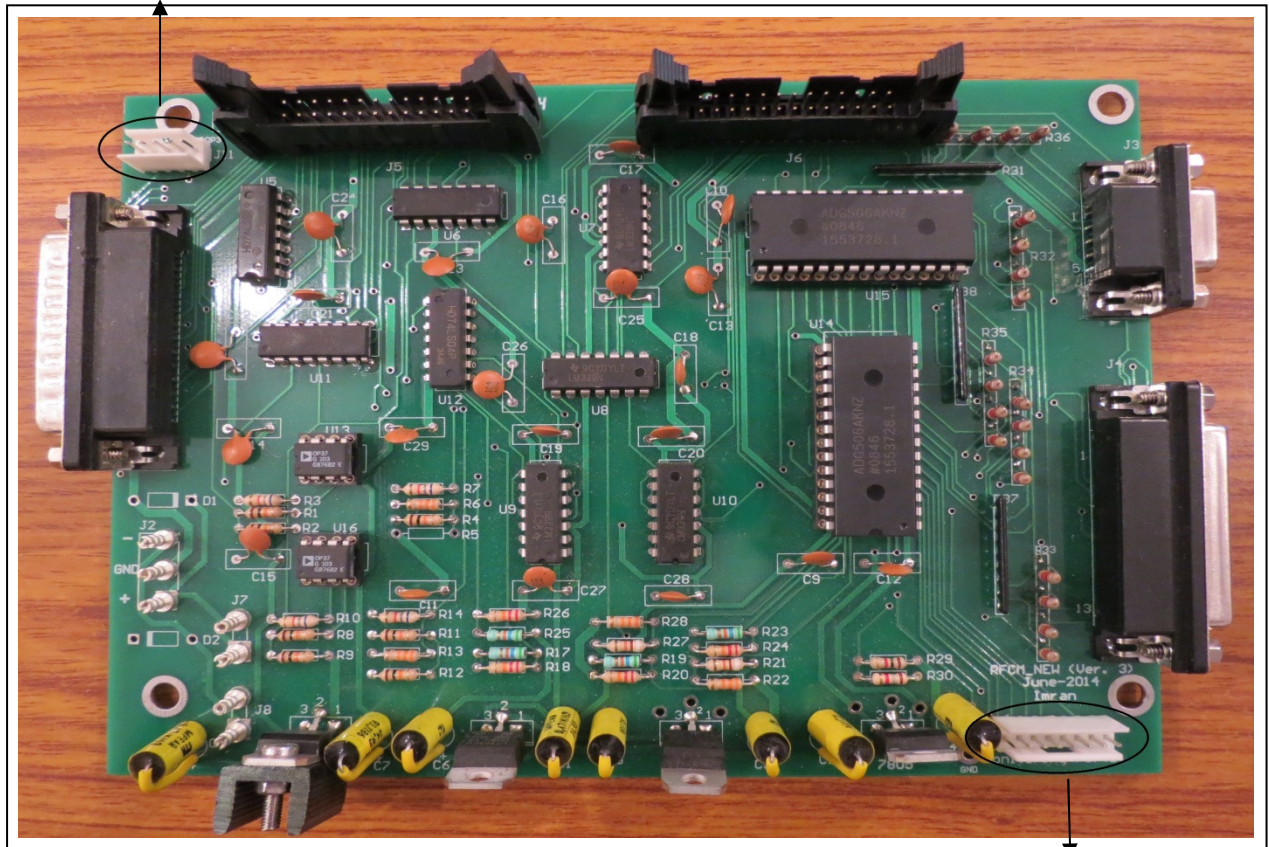
Fig.7(a) Assembled RFCM card Ver.3 Top View   **Monitoring Inputs**
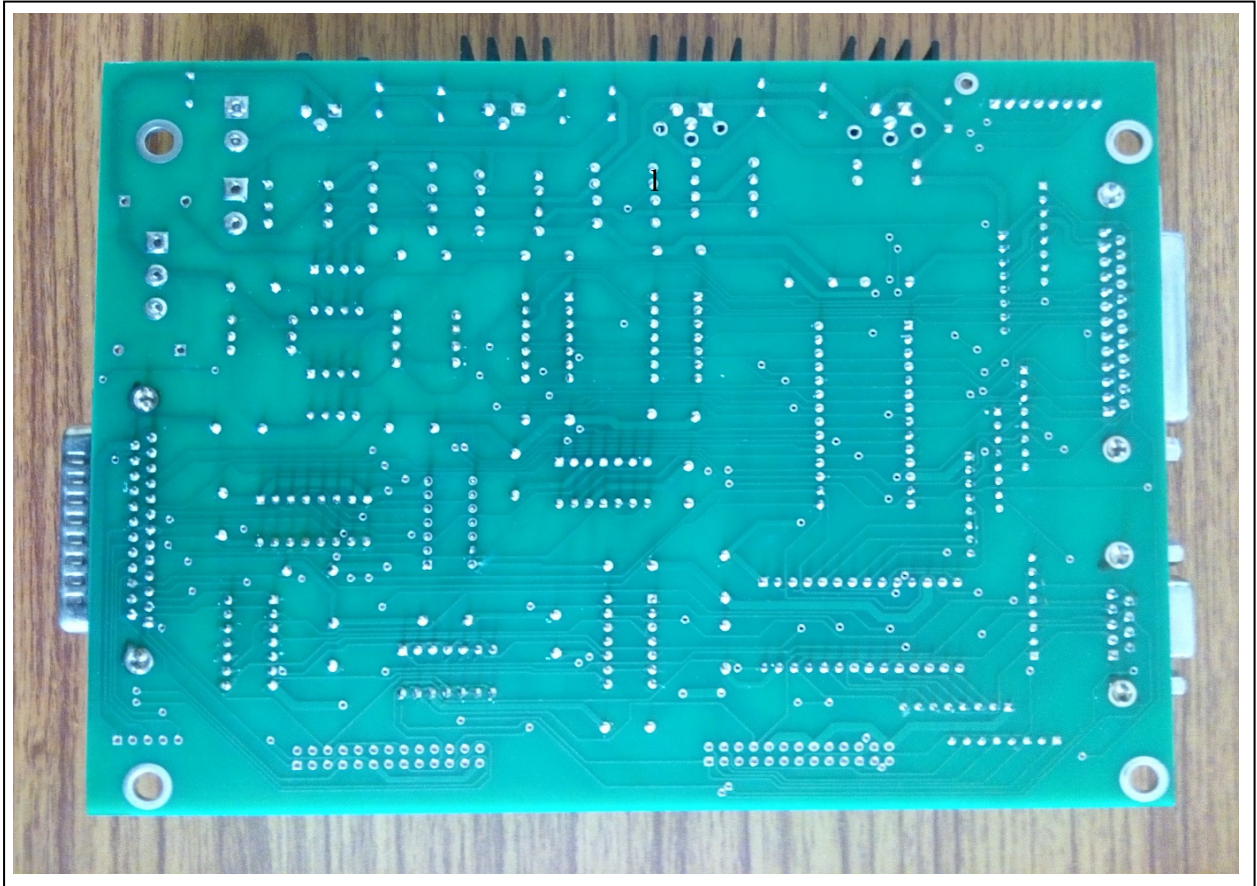
Fig.7(b) Assembled RFCM card Ver.3 Bottom View

5. Pin Configuration of Input / Output Connectors on RFCM card:

As shown in the figures above the RFCM card has one 25 pin D-type i/p connector (J1) and two 9 pin and 25 pin D-type o/p connectors (J3 and J4 respectively). Along with this it also has 5 pin and 8 pin Jalex connector for TTL input Filter Selection and for Monitoring purpose respectively. The RFCM card receives the inputs from the common box through a 25 pin round shell connector. The pin configuration for which is shown in the figure given below.
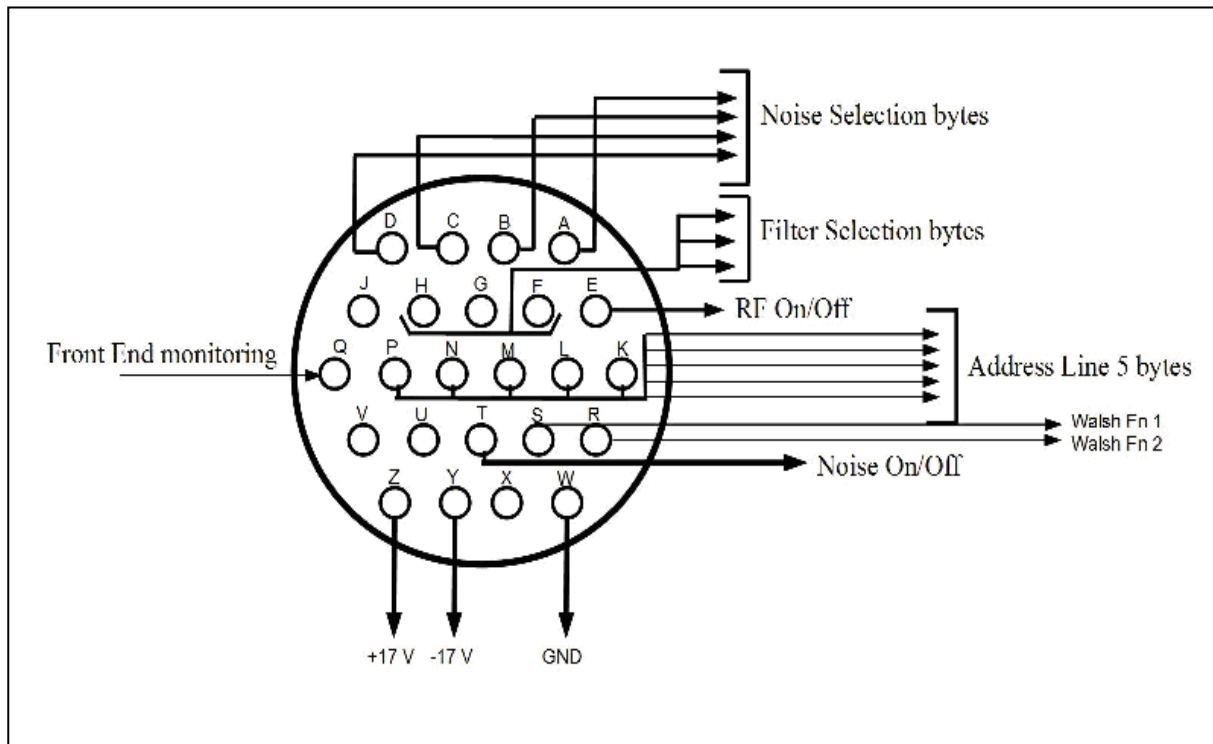
Fig. 8 Round Shell Connector Pin Configuration

The pin description for the 25 pin input connector is described below:

S. No.	Round Shell Connector	25 pin input D-type Connector (J1)	Pin configuration	Remark
1	A	1	NS0	
2	B	2	NS1	4 bits
3	C	3	NS2	Noise Selection
4	D	4	NS3	

5	E	5	D4	RF ON/OFF
6	H	6	Spare	Spare bit
7	G	7	FS1	Filter
8	F	8	FS0	Selection
9	K	9	A0	
10	L	10	A1	5 Bits
11	M	11	A2	Monitoring Address
12	N	12	A3	
13	P	13	A4	
14	T	14	Noise On/Off	Noise On/OFF
15	R	15	WF1	Walsh Switching
16	S	16	WF2	
17	J	17	GND	Ground
18	Q	18	M-Data	Monitoring Data
19		19	NC	Not Connected
20		20	NC	Not Connected
21		21	NC	Not Connected
22		22	NC	Not Connected
23		23	NC	Not Connected
24		24	GND	Ground
25		25	GND	Ground

The pin configuration of the output connector is as follows:

1. **25 Pin D-type connector (J4):**

Pin No.	Pin Configuration	Remark
1	Filter Selection	Two filter selection bits from the input get decoded into four bits and then level shifted into 0 V and -7 V. The four bits and there complement makes the 8 bits available for the filter selection.
2	Filter Selection	
3	Filter Selection	
4	Filter Selection	
5	Filter Selection	
6	Filter Selection	
7	Filter Selection	
8	Filter Selection	
9	GND	Ground
10	NC	Not Connected
11	NC	Not Connected
12	+12 V	Supply to Phase Switch/Post Amplifier
13	+12 V	Supply to Phase Switch/Post Amplifier
14	CP1	RF ON/OFF
15	CP2	
16	SP	Filter selection bits for by-pass mode selection
17	$\overline{SP}$	
18	GND	Ground
19	GND	Ground

Pin No.	Pin Configuration	Remark
20	NC	Not Connected
21	WF1	Walsh Switching +/- 10 V.
22	WF2	
23	NC	Not Connected
24	GND	Ground
25	GND	Ground

2. 9 Pin D-Type Connector (J3):

Pin No.	Pin Configuration	Remark
1	NS0	Four bits for Noise level selection.
2	NS1	
3	NS2	
4	NS3	
5	GND	Ground
6	$\overline{NS0}$	Complimentary four bits for Noise Level Selection.
7	$\overline{NS1}$	
8	$\overline{NS2}$	
9	$\overline{NS3}$	

3. 8 Pin Molex Connector (Monitoring Ports) J10:

Pin No.	Pin Configuration	Remark
1	M1 (Monitoring Port)	Spare
2	M2 (Monitoring Port)	Spare
3	M3 (Monitoring Port)	Spare
4	M4 (Monitoring Port)	Spare
5	M5 (Monitoring Port)	CH1 Power Monitoring
6	M6 (Monitoring Port)	CH2 Power Monitoring
7	M7 (Monitoring Port)	LNA Temp. Monitoring
8	M8 (Monitoring Port)	FE-Box Temp. Monitoring

4. 5 Pin Molex Connector (Filter Selection) J11:

Pin No.	Pin Configuration	Remark
1	GND	Ground
2	+5 V	Supply Voltage
3	OP1	FS0 Bit
4	OP2	Spare Bit
5	OP3	FS1 Bit

6. Conclusion:

The RFCM card is re-designed successfully to cater the control and monitoring requirements of all the GMRT front end systems. The prototype card is fabricated, assembled and tested successfully for all the functionalities with front end systems for L-band as well as some of the other bands like, existing 327 MHz and upgraded 250-500 MHz. It gives a unified solution for control and monitoring of existing as well as upgraded front-end systems.

7. Bill of materials:

S No.	Component Name	Description	Value
1	J1	D-Type Connector (Male)	25 Pin
2	J2	Sliver Twigs	3 Pin
3	J3	D-Type Connector (Female)	9 Pin
4	J4	D-Type Connector (Female)	25 Pin
5	J5	Jalex Connector (Male)	26 Pin
6	J6	Jalex Connector (Male)	26 Pin
7	J7-J8	Silver Twigs	2 Pin
8	J10	Molex Connector (Male)	8 Pin
9	J11	Molex Connector (Male)	5 Pin
10	U1	Voltage Regulator	7812
11	U2	Voltage Regulator	7912
12	U3	Voltage Regulator	7805
13	U4	Voltage Regulator	7905
14	U5	2 I/P Ex-Or 14 Pin IC	74LS86
15	U6-U10	Comparator 14 Pin IC	LM339
20	U11	Decoder 16 Pin IC	74LS139
21	U12	Hex Inverter 14 Pin IC	75LS04N
22	U13	Op-Amp 8 Pin IC	OP37
23	U14-U15	Multiplexer 28 Pin IC	ADG506A

25	U16	Op-Amp 8 Pin IC	OP37
26	C1-C8	Capacitors	0.47 uF
27	C9-C29	Ceramic Capacitors	0.1 uF
28	R1,R2,R4,R5,R8,R9,R11, R12	Resistors	10 k
29	R3,R7,R10,R14	Resistors	68 k
30	R6,R13,R22,R28	Resistors	33 k
31	R17,R19,R23,R25	Resistors	5 k
32	R18,R20,R24,R26	Resistors	22 k
33	R21,R27	Resistors	91 k
34	R29	Resistor	1 k
35	R30	Resistor	1.8 k
36	R31,R37,R38	Resistive Network (Series)	4.7 k
37	R32,R33,R34,R35,R36	Resistive Network (Parallel)	2.2 k
38	PCB Material	FR4 Substrate	1.6 mm Thick

8. Reference:

1. http://www.analog.com/media/en/technicaldocumentation/datasheets/ADG506A_507A.pdf
2. https://www.fairchildsemi.com/datasheets/LM/LM2901.pdf
3. http://www.cs.smith.edu/~thiebaut/270/datasheets/sn74ls86rev5.pdf
4. http://pdf.datasheetcatalog.com/datasheet/motorola/SN54LS139J.pdf
5. http://pdf.datasheetcatalog.com/datasheet/motorola/SN54LS04.pdf
6. http://www.analog.com/media/en/technical-documentation/data-sheets/OP37.pdf

9. Annexure:

1. Schematic Diagram:

MOTOROLA

QUAD 2-INPUT EXCLUSIVE OR GATE

SN54/74LS86

QUAD 2-INPUT
EXCLUSIVE OR GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ   Ceramic
SN74LSXXN   Plastic
SN74LSXXD   SOIC

TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

Symbol	Parameter			Min	Typ	Max	Unit
V$_{CC}$	Supply Voltage	54		4.5	5.0	5.5	V
		74		4.75	5.0	5.25	
T$_A$	Operating Ambient Temperature Range	54		−55	25	125	°C
		74		0	25	70	
I$_{OH}$	Output Current — High	54, 74				−0.4	mA
I$_{OL}$	Output Current — Low	54				4.0	mA
		74				8.0	

FEATURES
44 V Supply Maximum Rating
V_{SS} to V_{DD} **Analog Signal Range**
Single/Dual Supply Specifications
Wide Supply Ranges (10.8 V to 16.5 V)
Extended Plastic Temperature Range
(−40°C to +85°C)
Low Power Dissipation (28 mW max)
Low Leakage (20 pA typ)
Available in 28-Lead DIP, SOIC, PLCC, TSSOP and LCCC
Packages
Superior Alternative to:
DG506A, HI-506
DG507A, HI-507

FUNCTIONAL BLOCK DIAGRAM
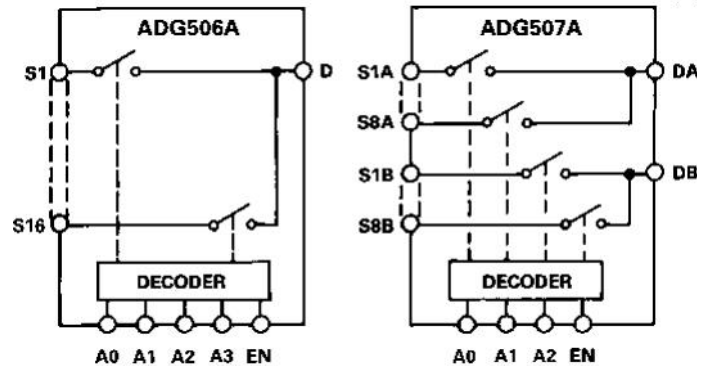
GENERAL DESCRIPTION

The ADG506A and ADG507A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels, respectively. The ADG506A switches one of 16 inputs to a common output, depending on the state of four binary addresses and an enable input. The ADG507A switches one of eight differential inputs to a common differential output, depending on the state of three binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic compatible digital inputs.

The ADG506A and ADG507A are designed on an enhanced LC²MOS process, which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can operate comfortably anywhere in the 10.8 V to 16.5 V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance
   The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.

2. Extended Signal Range
   The enhanced LC²MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.

3. Break-Before-Make Switching
   Switches are guaranteed break-before-make so input signals are protected against momentary shorting.

4. Low Leakage
   Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG506AKN	−40°C to +85°C	N-28
ADG506AKR	−40°C to +85°C	R-28
ADG506AKP	−40°C to +85°C	P-28A
ADG506ABQ	−40°C to +85°C	Q-28
ADG506ATQ	−55°C to +125°C	Q-28
ADG506ATE	−55°C to +125°C	E-28A
ADG507AKN	−40°C to +85°C	N-28
ADG507AKR	−40°C to +85°C	R-28
ADG507AKP	−40°C to +85°C	P-28A
ADG507AKRU	−40°C to +85°C	RU-28
ADG507ABQ	−40°C to +85°C	Q-28
ADG507ATQ	−55°C to +125°C	Q-28
ADG507ATE	−55°C to +125°C	E-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices' *Military/Aerospace Reference Manual* (1994) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.3" Small Outline IC (SOIC); RU = Thin Shrink Small Outline Package (TSSOP).

REV. C

Dual Supply (V_{DD} = +10.8 V to +16.5 V, V_{SS} = –10.8 V to –16.5 V unless otherwise noted)

Parameter	ADG506A ADG507A K Version +25°C	ADG506A ADG507A K Version –40°C to +85°C	ADG506A ADG507A B Version +25°C	ADG506A ADG507A B Version –40°C to +85°C	ADG506A ADG507A T Version +25°C	ADG506A ADG507A T Version –55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	-10 V $\leq V_S \leq$ +10 V, I_{DS} = 1 mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	V_{DD} = 15 V ($\pm$10%), V_{SS} = –15 V ($\pm$10%)
	300	400	300	400	300		Ω max	V_{DD} = 15 V ($\pm$5%), V_{SS} = –15 V ($\pm$5%)
					300	400	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	-10 V $\leq V_S \leq$ +10 V, I_{DS} = 1 mA
R_{ON} Match	5		5		5		% typ	-10 V $\leq V_S \leq$ +10 V, I_{DS} = 1 mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = $\pm$10 V, V2 = $\mp$10 V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = $\pm$10 V, V2 = $\mp$10 V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = $\pm$10 V, V2 = $\mp$10 V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	V1 = $\pm$10 V, V2 = $\mp$10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = $\pm$10 V, V2 = +10 V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 7 V rms, f = 100 kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8 V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		µA typ	V_{IN} = V_{IN} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTES

[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Single Supply $(V_{DD} = +10.8 \text{ V to } +16.5 \text{ V}, V_{SS} = \text{GND} = 0 \text{ V unless otherwise noted})$

Parameter	ADG506A ADG507A K Version +25°C	−40°C to +85°C	ADG506A ADG507A B Version +25°C	−40°C to +85°C	ADG506A ADG507A T Version +25°C	−55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	500 700	1000	500 700	1000	500 700	1000	Ω typ Ω max	$0 \text{ V} \leq V_S \leq +10 \text{ V}, I_{DS} = 0.5 \text{ mA; Test Circuit 1}$
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	$0 \text{ V} \leq V_S \leq +10 \text{ V}, I_{DS} = 0.5 \text{ mA}$
R_{ON} Match	5		5		5		% typ	$0 \text{ V} \leq V_S \leq +10 \text{ V}, I_{DS} = 0.5 \text{ mA}$
I_S (OFF), Off Input Leakage	0.02 1	50	0.02 1	50	0.02 1	50	nA typ nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A Only)		25		25		25	nA max	V1 = +10 V/0 V, V2 = 0 V/ +10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	$V_{IN} = 0 \text{ to } V_{DD}$
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300 450	600	300 450	600	300 450	600	ns typ ns max	V1 = +10 V/0 V, V2 = +10 V; Test Circuit 6
t_{OPEN}[1]	50 25	10	50 25	10	50 25	10	ns typ ns min	Test Circuit 7
t_{ON} (EN)[1]	250 450	600	250 450	600	250 450	600	ns typ ns max	Test Circuit 8
t_{OFF} (EN)[1]	250 450	600	250 450	600	250 450	600	ns typ ns max	Test Circuit 8
OFF Isolation	68 50		68 50		68 50		dB typ dB min	$V_{EN} = 0.8 \text{ V}, R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_S = 3.5 \text{ V rms, f} = 100 \text{ kHz}$
C_S (OFF)	5		5		5		pF typ	$V_{EN} = 0.8 \text{ V}$
C_D (OFF)								
ADG506A	44		44		44		pF typ	$V_{EN} = 0.8 \text{ V}$
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	$R_S = 0 \text{ }\Omega, V_S = 0 \text{ V; Test Circuit 9}$
POWER SUPPLY								
I_{DD}	0.6	1.5	0.6	1.5	0.6	1.5	mA typ mA max	$V_{IN} = V_{INL} \text{ or } V_{INH}$
Power Dissipation	10	25	10	25	10	25	mW typ mW max	

NOTES
[1]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Truth Table (ADG506A)

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table (ADG507A)

A2	A1	A0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

–3–

ADG506A/ADG507A

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS} .... 44 V
V_{DD} to GND .... 25 V
V_{SS} to GND .... –25 V
Analog Inputs[2]
Voltage at S, D .... V_{SS} – 2 V to V_{DD}
.... + 2 V or
.... 20 mA, Whichever Occurs First
Continuous Current, S or D .... 20 mA
Pulsed Current S or D
  1 ms Duration, 10% Duty Cycle .... 40 mA
Digital Inputs[2]
  Voltage at A, EN .... V_{SS} – 4 V
  .... to V_{DD} + 4 V or
  .... 20 mA, Whichever Occurs First

Power Dissipation (Any Package)
  Up to +75°C .... 470 mW
    Derates above +75°C by .... 6 mW/°C
Operating Temperature
  Commercial (K Version) .... –40°C to +85°C
  Industrial (B Version) .... –40°C to +85°C
  Extended (T Version) .... –55°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) .... +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause perma-
nent damage to the device. This is a stress rating only; functional operation of the
device at these or any other conditions above those indicated in the operational
sections of this specification is not implied. Exposure to absolute maximum rating
conditions for extended periods may affect device reliability.
[2]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited
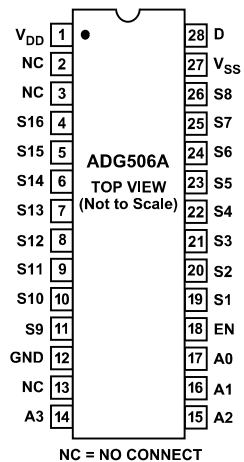to the Maximum Rating above.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
accumulate on the human body and test equipment and can discharge without detection.
Although the ADG506A/ADG507A feature proprietary ESD protection circuitry, permanent
damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper
ESD precautions are recommended to avoid performance degradation or loss of functionality.
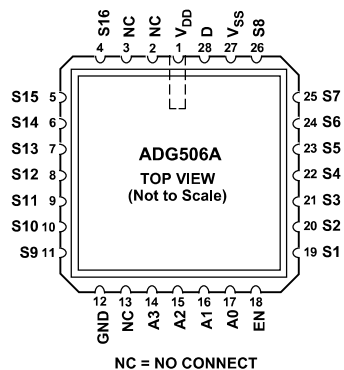
WARNING!
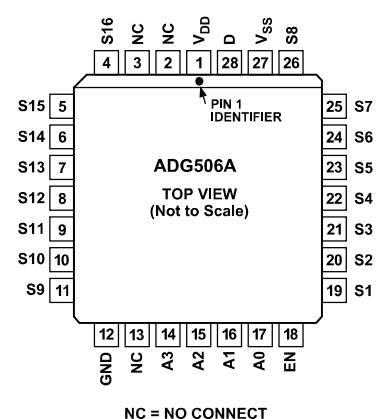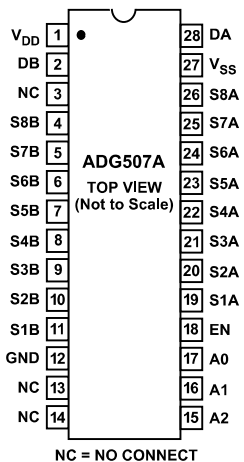ESD SENSITIVE DEVICE

PIN CONFIGURATIONS

DIP, SOIC

ADG506A TOP VIEW (Not to Scale)

Pin	Signal		Pin	Signal
1	V_{DD}		28	D
2	NC		27	V_{SS}
3	NC		26	S8
4	S16		25	S7
5	S15		24	S6
6	S14		23	S5
7	S13		22	S4
8	S12		21	S3
9	S11		20	S2
10	S10		19	S1
11	S9		18	EN
12	GND		17	A0
13	NC		16	A1
14	A3		15	A2

NC = NO CONNECT

LCCC

ADG506A TOP VIEW (Not to Scale)

Top pins (4–28): S16(4), NC(3), NC(2), V_{DD}(1), D(28), V_{SS}(27), S8(26)
Left pins: S15(5), S14(6), S13(7), S12(8), S11(9), S10(10), S9(11)
Right pins: S7(25), S6(24), S5(23), S4(22), S3(21), S2(20), S1(19)
Bottom pins (12–18): GND(12), NC(13), A3(14), A2(15), A1(16), A0(17), EN(18)

NC = NO CONNECT

PLCC

ADG506A TOP VIEW (Not to Scale)
PIN 1 IDENTIFIER

Top pins (4–28): S16(4), NC(3), NC(2), V_{DD}(1), D(28), V_{SS}(27), S8(26)
Left pins: S15(5), S14(6), S13(7), S12(8), S11(9), S10(10), S9(11)
Right pins: S7(25), S6(24), S5(23), S4(22), S3(21), S2(20), S1(19)
Bottom pins (12–18): GND(12), NC(13), A3(14), A2(15), A1(16), A0(17), EN(18)

NC = NO CONNECT

DIP, SOIC, TSSOP

ADG507A TOP VIEW (Not to Scale)

Pin	Signal		Pin	Signal
1	V_{DD}		28	DA
2	DB		27	V_{SS}
3	NC		26	S8A
4	S8B		25	S7A
5	S7B		24	S6A
6	S6B		23	S5A
7	S5B		22	S4A
8	S4B		21	S3A
9	S3B		20	S2A
10	S2B		19	S1A
11	S1B		18	EN
12	GND		17	A0
13	NC		16	A1
14	NC		15	A2

NC = NO CONNECT

LCCC

ADG507A TOP VIEW (Not to Scale)

Top pins (4–28): S8B(4), NC(3), DB(2), V_{DD}(1), DA(28), V_{SS}(27), S8A(26)
Left pins: S7B(5), S6B(6), S5B(7), S4B(8), S3B(9), S2B(10), S1B(11)
Right pins: S7A(25), S6A(24), S5A(23), S4A(22), S3A(21), S2A(20), S1A(19)
Bottom pins (12–18): GND(12), NC(13), NC(14), A2(15), A1(16), A0(17), EN(18)

NC = NO CONNECT

PLCC

ADG507A TOP VIEW (Not to Scale)
PIN 1 IDENTIFIER

Top pins (4–28): S8B(4), NC(3), DB(2), V_{DD}(1), DA(28), V_{SS}(27), S8A(26)
Left pins: S7B(5), S6B(6), S5B(7), S4B(8), S3B(9), S2B(10), S1B(11)
Right pins: S7A(25), S6A(24), S5A(23), S4A(22), S3A(21), S2A(20), S1A(19)
Bottom pins (12–18): GND(12), NC(13), NC(14), A2(15), A1(16), A0(17), EN(18)

NC = NO CONNECT

REV. C
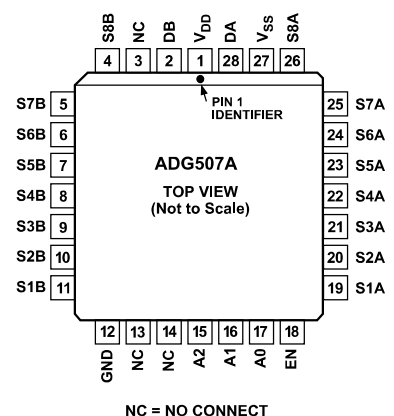
LM339/LM339A, LM239A, LM2901

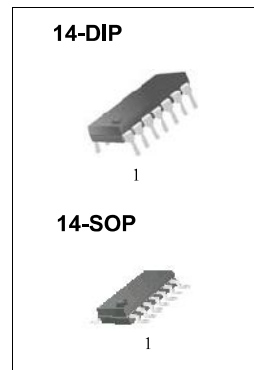## Quad Comparator

Features
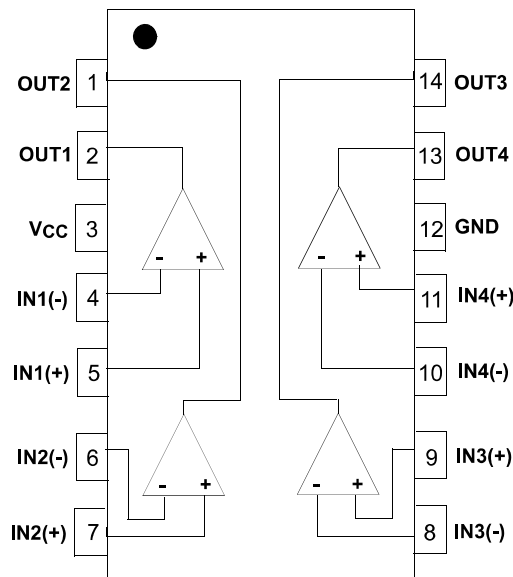
- Single or Dual Supply Operation
- Wide Range of Supply Voltage
  LM2901, LM339/LM339A, LM239A: 2 ~ 36V (or ±1 ~ ±18V)
- Low Supply Current Drain 800μA Typ.
- Open Collector Outputs for Wired and Connectors
- Low Input Bias Current 25nA Typ.
- Low Input Offset Current ±2.3nA Typ.
- Low Input Offset Voltage ±1.4mV Typ.
- Input Common Mode Voltage Range Includes Ground.
- Low Output Saturation Voltage
- Output Compatible With TTL, DTL and MOS Logic System

Description

The LM339/LM339A ,LM239A, LM2901 consist of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

14-DIP

1

14-SOP

1

Internal Block Diagram

Pin	Signal
1	OUT2
2	OUT1
3	Vcc
4	IN1(-)
5	IN1(+)
6	IN2(-)
7	IN2(+)
8	IN3(-)
9	IN3(+)
10	IN4(-)
11	IN4(+)
12	GND
13	OUT4
14	OUT3

Rev. 1.0.5

ANALOG DEVICES

Low Noise, Precision, High Speed Operational Amplifier (A$_{VCL}$ ≥ 5)

OP37

FEATURES
Low Noise, 80 nV p-p (0.1 Hz to 10 Hz)
3 nV/√Hz @ 1 kHz
Low Drift, 0.2 μV/°C
High Speed, 17 V/μs Slew Rate
63 MHz Gain Bandwidth
Low Input Offset Voltage, 10 μV
Excellent CMRR, 126 dB (Common-Voltage @ 11 V)
High Open-Loop Gain, 1.8 Million
Replaces 725, OP-07, SE5534 In Gains > 5
Available in Die Form

GENERAL DESCRIPTION
The OP37 provides the same high performance as the OP27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17 V/μs and gain-bandwidth product to 63 MHz.

The OP37 provides the low offset and drift of the OP07 plus higher speed and lower noise. Offsets down to 25 μV and a maximum drift of 0.6 μV/°C make the OP37 ideal for precision instrumentation applications. Exceptionally low noise (e_n= 3.5 nV/ @ 10 Hz), a low 1/f noise corner frequency of 2.7 Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of 10 nA and offset current of 7 nA are achieved by using a bias-current cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to 20 nA and 15 nA respectively.

The output stage has good load driving capability. A guaranteed swing of 10 V into 600 Ω and low output distortion make the OP37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.
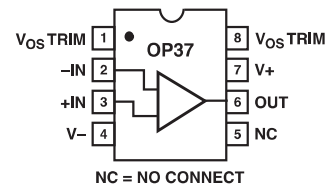
The OP37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tapehead, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.
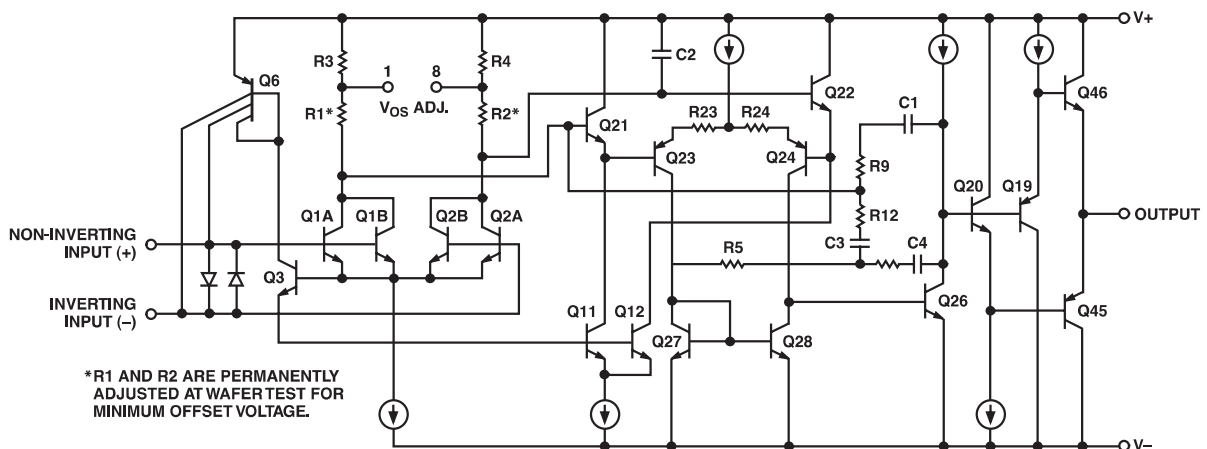
PIN CONNECTIONS

8-Lead Hermetic DIP
(Z Suffix)

Epoxy Mini-DIP
(P Suffix)

8-Lead SO
(S Suffix)

NC = NO CONNECT

SIMPLIFIED SCHEMATIC

*R1 AND R2 ARE PERMANENTLY
ADJUSTED AT WAFER TEST FOR
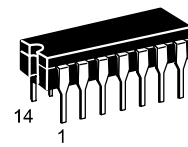MINIMUM OFFSET VOLTAGE.

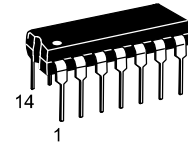REV. B

MOTOROLA
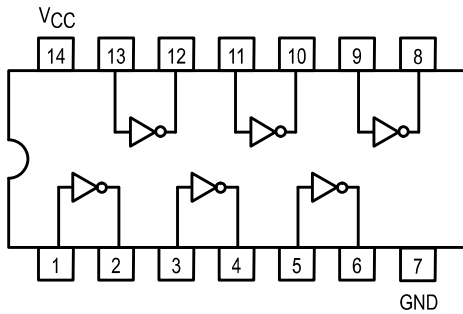
HEX INVERTER
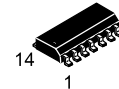
SN54/74LS04

HEX INVERTER
LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

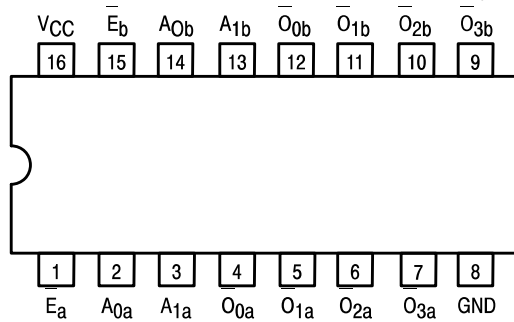| Symbol	Parameter			Min	Typ	Max	Unit
V$_{CC}$	Supply Voltage	54		4.5	5.0	5.5	V
		74		4.75	5.0	5.25	
T$_A$	Operating Ambient Temperature Range	54		−55	25	125	°C
		74		0	25	70	
I$_{OH}$	Output Current — High	54, 74				−0.4	mA
I$_{OL}$	Output Current — Low	54				4.0	mA
		74				8.0	

MOTOROLA

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The LSTTL/MSI SN54/74LS139 is a high speed Dual 1-of-4 Decoder/De-multiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

| 16 V_{CC} | 15 $\overline{E}_b$ | 14 A_{0b} | 13 A_{1b} | 12 $\overline{O}_{0b}$ | 11 $\overline{O}_{1b}$ | 10 $\overline{O}_{2b}$ | 9 $\overline{O}_{3b}$ |

| 1 $\overline{E}_a$ | 2 A_{0a} | 3 A_{1a} | 4 $\overline{O}_{0a}$ | 5 $\overline{O}_{1a}$ | 6 $\overline{O}_{2a}$ | 7 $\overline{O}_{3a}$ | 8 GND |

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

|		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
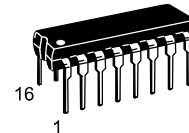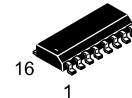
LOGIC DIAGRAM

V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS
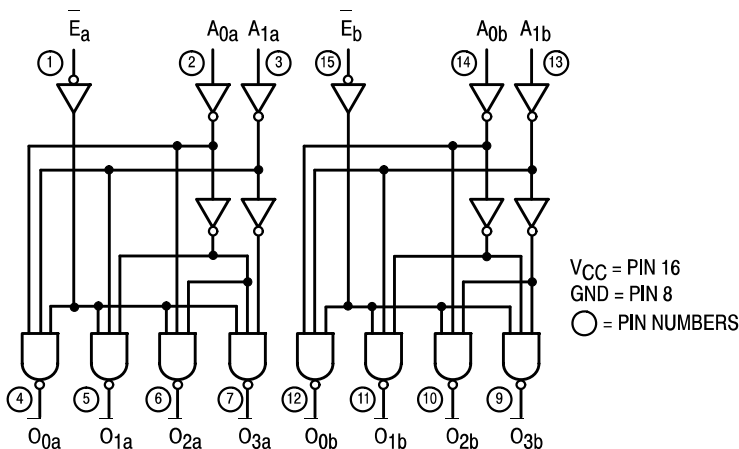
SN54/74LS139

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY
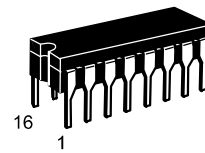
J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
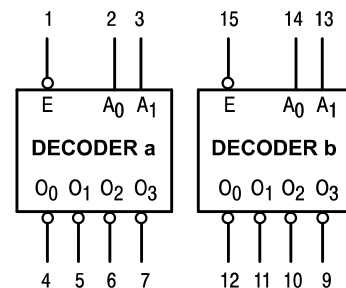PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL

V_{CC} = PIN 16
GND = PIN 8