CORRELATOR CLOCK - SOME COMMENTS.

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ABSTRACT : Correlator System for GMRT Receiver needs two highly stable clock signals one at 32 MHz and the other at 32.25 MHz which will be used to sample baseband signal at 16 MHz bandwidth. Shri Puneet Chopra has worked out three schemes in consultation with Mr. Ramkumar of RRI and presently working on one of the schemes. This report evaluates various schemes of his and suggestes alternate schemes better performance and needs less hardware.

DESCRIPTION: I understand from Shri Chopra's report that the basic time referance was assumed to be 10 MHz which is unfortunately not correct. We are certainly not going to have a separate time and frequency standard for correlator system. It was clearly mentioned in several occasions and in various reports that GMRT will have a 5 MHz time and frequency standard either from a Rubidium source or from an Oscilloquartz. So all his schemes have to be modified taking this into consideration.

Let us go through his schemes one by one. In the first scheme two PLL's are proposed. Instead of single loop direct synthesis, a complicated harmonic locking technique is used which asks for sharp cut-off filters and usage of mixers. The 2nd PLL uses mixer technique which also needs sharp cutt-off filter at 32.25 MHz, frequency dividers, amplifiers etc. It is almost impossible to put active filters at this frequency because of frequency limitations of op-amps. Passive filters are quite bulky at this low frequency and it needs a lot of tuning elements. Scheme one as it is mentioned in Shri Puneet's report is not that good because of the above mentioned reasons. But I certainly don't agree with him on the points he has listed in his report as the major drawback for scheme one. It says that phase lock loop will introduce phase noise - that's not true. Here the requirement is a low phase noise stable clock signal. Within the loop bandwidth the phase noise of a PLL is very close to the referance signal. So, PLL does not really degrades phase noise performance, it improves instead. It is also reported that tracking between two PLLs' will be difficult. If the PLLs' are locked to the same referance frequency, they are no longer independent and there is no question of any problem of tracking. Moreover synchronous counting does not necessarily means it has to be binary division. I don't see any reason why divide by 40 will give any phase discripency if divided synchronously. I feel the scheme was worked out with a particular kind of commercially available PLL chip in mind which requires 50% duty cycle signals for proper operations (like NE564 etc.) and for that non binary synchronous divion wont work as it will not give 50% duty cycle. Discrete PLL won't have this problem.

Scheme two looks more cumbersome. It has three mixers and number of filters are also more than previous scheme. Phase noise won't improve but can get degraded in this scheme from the previous scheme if the filters are not designed properly. It will introduce unwanted intermodulation products which will be very difficult to avoid by filtering.

Let us now have a close look at scheme three which was finally accepted. This particular scheme was chosen as 'no active components are involved' - the report says. Digital counters are active devices. So, active devices are present but less in number. In this scheme 10 MHz TTL signal is generated from Rubidium source using a Schmitt Trigger. The third harmonic is filtered out to get 30 MHz sinusoidal signal. Power content of that will be quite low. 2 MHz sinusoidal signal is generated by dividing 10 MHz by 5 and then filtering. This two are mixed to get 32 MHz signal in an active mixer - I presume - nothing is mentioned about the type of mixer used. A 32 MHz BPF is used to reject lower side band as well as 30 MHz signal. It needs a high roll off filter - it means high order

filter which effectively means more no. of tunning elements. Any change in the tunning elements will change the filter response drastically and since the performance of the circuit heavily depends on the filter performance the scheme certainly is not a reliable one.

32.25 MHz is generated mixing 2 MHz with 250 KHz and mixing this output to 30 MHz generated previously. The performance of this circuit is also solely dependent on the filter performances. This scheme uses three mixers. Mixers are non linear devices and it will produce a lot of intermodulation products. And due to some practical limitions (mainly because of bulkyness) high roll off filters will be very difficult to achieve (Roll off of a filter depends on the type of filter used; like Butterworth, Chebychev etc. and also on the order of the filter. Elliptiic type of filters generally gives maximum roll off, but no. of tunning elements are quite high in elliptic kind of filter. One 6th oder elliptic BPF which has moderate roll off needs 8 tunnuing elements !). As a result of which the spectrum will be full of unwanted lines which will give a very poor RMS phase noise performance (though the main requirement is a good close in phase noise performance, poor RMS phase noise will certainly degrade long term clock performance.). Moreover no PLL is involved in this sscheme. So any varition due to temperature will manifest itself as error in the phase variatiion of the clock. Schmitt triggers, active mixers and amplifiers will certainly generate phase delay and there is no way it can be corrected. There is a high probability of phase asynchronism in the two clocks of 32 MHz and 32.25 MHz due to this delays.

SUGGESTED SCHEME : Keeping in mind the low phase noise requirements for the clocks, two schemes are suggested. Scheme 1 and 2 uses the same technique to generate 32 MHz clock. So 32 MHz clock generation will be described as a common scheme and two seperate schemes will be described for 32.25 MHz generation.

Figure 1. shows the block diagram for 32 MHz clock generation. In this scheme 1 MHz is generated from 5 MHz rubidium dividing it by 5 and this 1 MHz is used as the referance to the phase frequency detector. The required clock is generated by multiplying 1 MHz by 32. The phase noise performance will get degraded by 16 to 18 dB from the phase noise of Rubidium source. At 1 KHz offset from the carrier 32 MHz will have Phase noise of around -120 dBc/Hz. It will be better to go for discrete PLL instead of going for commercially available PLL chip like NE 564. One does not have much control over various loop parameters in NE 564 kind of PLL chip. I feel it will be best to use MC4044 phase detector with 74S124 VCO (TTL) and 74HCT163 synchronous programmable counter. Total no. of chip needed is 6 only and 2"x2.5" card size will be adequate.

GENERATION OF 32.25 MHz CLOCK : Two schemes are suggested for this. Fig.2 shows the block diagram for scheme 1. In this scheme 1 MHz (which was generated from 5 MHz for 32 MHz clock) is divided by 4 to get 250 KHz. VCO output is mixed with 32 MHz (which was generated previously) and 250 KHz is filtered out using a Low Pass filter and is compared with 250 KHz ref. signal. This scheme is quite simple. Only problem that may arise that the VCO may get locked to 31.75 MHz instead of 32.25 MHz; one has to take care about that while choosing VCO's free running frequency components, and since mixer is used some intermodulation products will be present but it can be suppressed a lot by designing loop bandwidth properly. Close in Phase noise performance for this clock will be as good as the performance of 32 MHz clock. Component requirement is also not much. Filter (250 KHz LPF) could be an active filter with 741 IC and the mixer could be active or passive. The card size will be around 3"x3".

Fig.3 shows the block diagram for scheme 2. 1 MHz is divided by 4 to get 250 KHz. VCO output is synchronously divided by 129 and is compared with 250 KHz in the phase frequency detector of the PLL. Phase noise performance will be of the same order of 32 MHz's clock. No of component is not many and and the card size will be almost 3"x3".

CONCLUSION : Since all the above schemes use Phase Locked Loop and are locked to the same

Rubidium source, there is no question of phase asynchronism or phase ambiguity. There are no tunning elements present and the system is not bulky either. Phase noise will be around -120 dBc/Hz at 1 KHz offset and I feel it is more than sufficient for the correlator clock requirement.

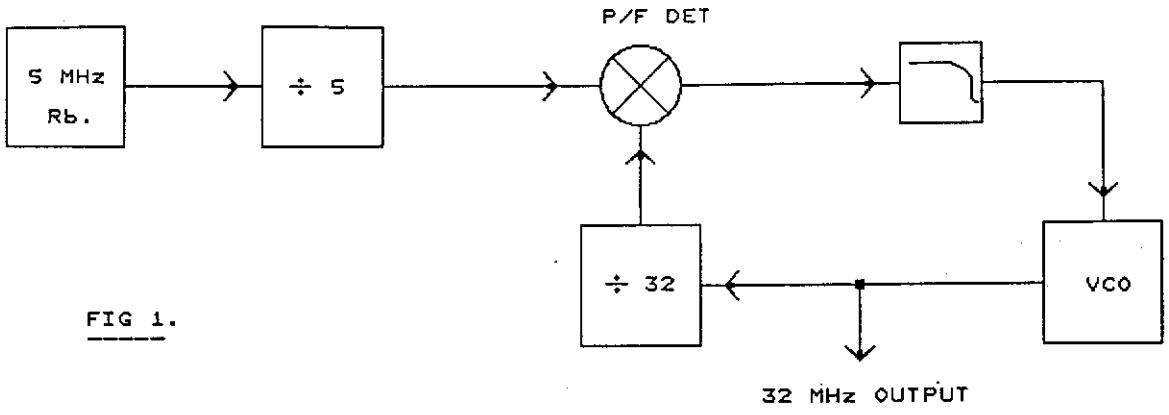

FIG 1.

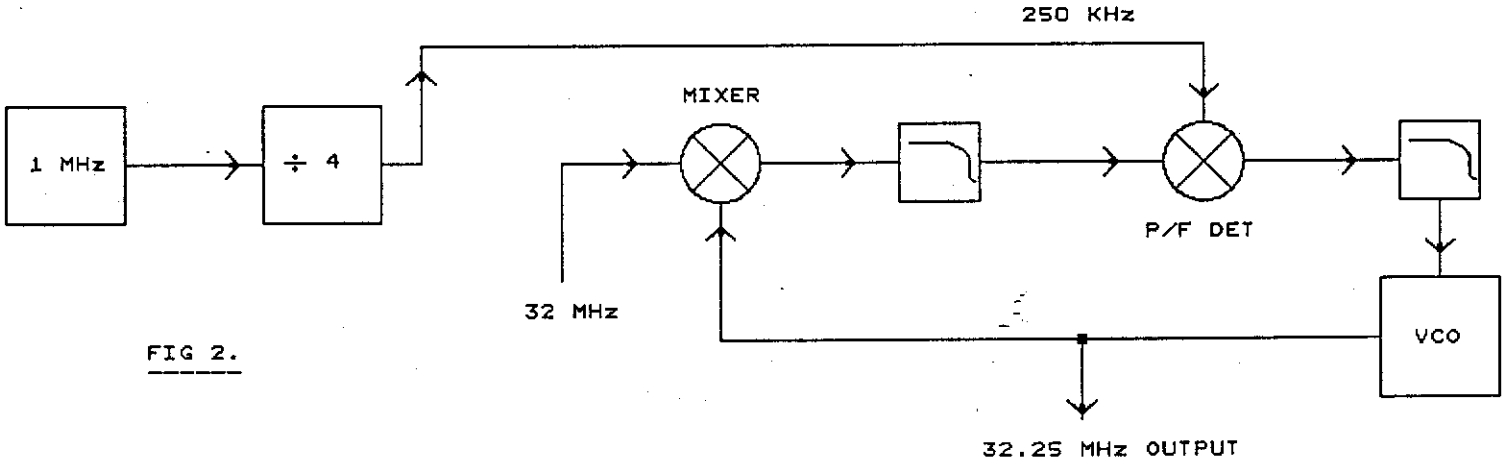

FIG 2.

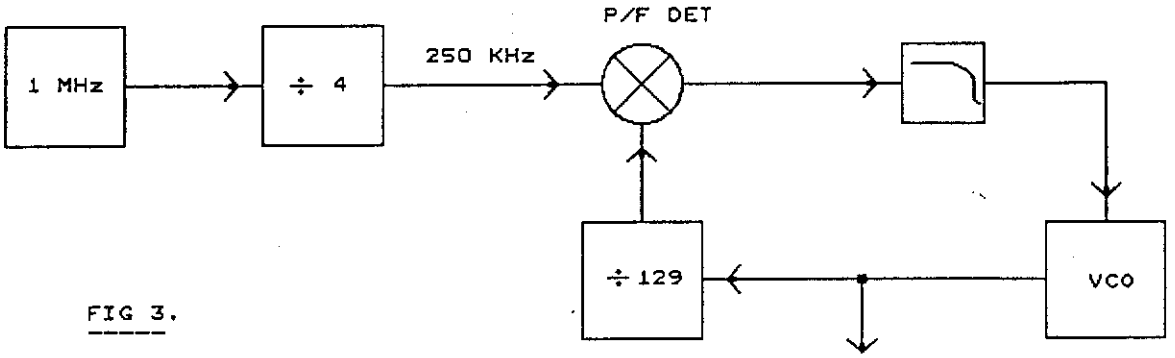

FIG 3.