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(Ref: rkm1/MAC/march)

MULTIPLIER ACCUMULATOR CARD–Configuration and Control

Certain changes in the original Correlator System for VLBA have been made to suit our requirements. Fig 1.1 gives the Block Diagram of the Correlator System for GMRT. First three blocks —– Quantizer, Data Preparation Card (DPC) and the FFT Card have already been described elsewhere (ref. CRS's reports on the Corr. System). This report describes the design of the Multiplier Accumulator Card (MAC) and the control card for the MAC. VLBA ASIC chip is at the core of the MAC system (the same chip,in a different mode, is being used for FFT also).

1. REQUIREMENTS: Conceptually the job of the MAC is to multiply two incoming complex numbers, add the result to the appropriate accumulation and store the sum back again. It is required to correlate signals from all the 30 antennas in one of the follwing modes :

(a) Non Polarization

(b) Polarization I (only two correlations - RR,LL)

(c) Polarization II (all four correlations - RR,RL,LR,LL)

(d) Dual Frequency

How these modes are realized is described in a later section.

2. INPUTS SIGNALS to MAC: Complex numbers to be multiplied and accumulated in the MAC come from the outputs of the FFT cards. Each antenna has one FFT Card which consists of four FFT engines (or pipelines). These four engines are divided into two blocks. Each block processes one 16 MHz(max) Baseband — with the two engines in a block independently processing Right (R) and Left (L) Circular Polarizations respectively. The two blocks can be used to process USB and LSB (total BW of

32MHz(max)) in mode (a) and (b) or only one Sideband but full polarization in mode (c) or two single 16 MHz(max) bands of two different observation frequencies in mode (d).

Figs. 2.1 through 2.4 depict these four modes and the Bandwidths available in each mode alongwith the final FFT outputs which are to be correlated by the MAC. As is shown in these figures, the two channels of a block in the FFT Card are Multiplexed to get an output rate of 32 Ms/sec which is the required input rate for the subsequent Multiplier stages.(o/p of the FFT engine is at half the input rate because of a reduction in the numbers of outputs by a factor of two.)

3. MAC CONFIGURATION : N point FFT gives N/2 channels at the output. One channel from a given antenna is to be correlated with the identical channel from all the 30 antennas (including auto-correlation). This requires $30(30+1)/2 = 465$ multipliers for obtaining all the correlations for one 16MHz (max) baseband. Since there are two Basebands per antenna, the no. of the ASIC chips required for Multiplication and Accumulation is 930. One simple arrangement that would do the job for one baseband is shown in Fig 3.1. However practical considerations do not allow one to place 930 chips on one card and the configuration that we are going to use is as shown in Fig 3.2. There will be 32 MAC cards each having a maximum of 32 chips. 16 of these cards will be for one baseband and the remaining 16 for the other. These 32 chips on a card will be arranged in two blocks of (4 X 4) each. Out of the 32 (4 X 4) blocks required for one baseband, 21 will have 16 multiplier chips each, 7 will have 15 chips each and the remaining 4 only 6 chips each. This asymmetry in the number of multipliers per card comes in order to avoid redundancy in the correlations.

With this configuration, each card in general will have 16 inputs. Since the FFT output is in the format 4,4,4 and the signals are ECL differential, a total of 384 pins are required on each card. However the space available on the Card allows only 192 pins (ie. two 96-pin connectors). Therefore instead of converting the ECL differential signal to TTL unipolar on the Multiplier board as is being done in the VLBA MAC, we will be doing ECL Diff. to TTL Unipolar translation on the backplane itself just before feeding the signals to the MAC. This conversion will be done by using ECL-to-TTL Translators (MC10125).

Also, in this configuration each FFT output goes to eight MAC's. Since ECL Differential outputs allow a maximum Fan-out of 3 only, each FFT output will be input to a 1:9 ECL Clock Driver (MC 100E111)

thus enabling one to have nine identical outputs.

4. MAC CARD-ARRANGEMENT: All the 32 cards will be placed in four chassis – each chassis containing 8 MAC Cards. In addition to that ,there will be one MAC Controller Cards in each chassis. Each Controller Card will take care of 8 MAC Cards. Fig 4.1 shows the contents of two chassis C1 and C2 for one baseband. Some of the inputs which are common to both the chassis ,will be taken from one chassis to the other resulting in a requirement of ten 96-pin connectors per chassis.

5. MAC OPERATION :Basic MAC operation is depicted in Fig 5.1. Two (4,4,4) complex points enter the ASIC chip at a rate of 32 Ms/sec via the Normal Port and the Twiddle Factor Port, they are multiplied and added to the complex accumulation obtained from the on chip RAM and the 36-bit result (Format: 15,15,6) is stored back in the RAM. The on-chip 512 X 36 bit RAM actually consists of two physically separate 512 X 18 bit RAMs (These two 512 X 18 bit RAMs are used for double buffered inputs for performing FFT). One may note here that these RAMs are not dual port RAMs and therefore in one clock-cycle, one can perform only one operation — either READ or WRITE. 512 X 36 bit RAM is split into two logical blocks of 256 X 36 bit each. While accumulation takes place in one half, accumulated data is read from the other half.

Another thing that must be noted in order to understand the MAC operation is that all internal chip operations use a clock of 32.25 MHz and the 32MHz clock that has been talked of so often is being used only by the sampler and DPC onwards, the clock used is always 32.25MHz One FFT cycle consists of 516 clock cycles. During the first 512 clock cycles, incoming data is integrated (multiplication and accumulation) and the results corresponding to different channels are stored in different memory locations in one half (because max no of channels is 256) of the RAM. The four additional clock-cycles available are used to read out one 36 bit word from that half of the RAM which is not being currently used for accumulation.Thing to be noted here is that READOUT rate is $32.25/2 = 16.125$ MHz and the output bus is 18 bit wide, hence it takes four internal clock cycles to readout one full 36 bit word. Therefore to read out all the 256 locations (36 bit wide), it takes 256 FFT cycles which is approximately 4 ms. However there are 32 ASICs to be read from one card and only one 18 bit o/p bus is available on each card and therefore to read one full card it takes approximately 128ms. This is the time resolution that one can get without losing any input data when the

baseband is 16 MHz wide.

However there will be situations when the baseband is less than 16 MHz wide. For example lets say the baseband is only 8 MHz wide. For this the Nyquist sampling rate will be 16 MHz. However our system doesn't allow luxuries of different sampling rates for different bandwidths and the sampling will always be at a rate of 32 MHz. This means that two consecutive 512 point input sequences will have a 50 percent overlap and only alternate input sequences will be non-overlapping. One question that may be asked at this stage is whether it is feasible to read the data out during alternate FFT cycles so that one may improve the time resolution. The answer is yes and for this example, four FFT cycles will be required to readout one full ASIC. Of these four FFT cycles,accumulation does not take place for the two cycles during which readout operation is being done.Since there are 32 chips, time resolution possible with this scheme is 2ms of which actual accumulation takes place for only 1ms and the data in the remaining 1ms is lost (though it does not hurt in this example because of oversampling by a factor of two).

Apart from this, there may be cases where one would like to have a selectable time resolution may be at the cost of reduction in the bandwidth or loss of a fraction of data if it doesn't hurt the sensitivity. Such luxuries which don't exist in the VLBA design will be provided in the GMRT Correlator System. The time resolution options available to the user will be:

2ms, 4ms, 8ms ,16ms, 32ms, and 64ms apart from the regular mode of 128ms resolution.

Apart from the 128ms resolution mode, in all the other modes actual integration time is 1ms less than the values mentioned for the time resolution as that much time is required for the Readout Operation.

Readout operation starts with the assertion of a signal STAREAD which remains High (or Low) for two clock cycles. How exactly it is done will be explained in the section on MAC Control card.

5.1 MAC OPERATION in NON-POLARIZATION MODE : Lets take as an example two antennas 'X' and 'Y' as shown in Fig 5.2 .

In the Non-Pol. mode, outputs p* and q* from one block of two FFT Engines of one antenna correspond to USB while r* and s* correspond to LSB. Timing diagrams for the Multiplication- Accumulation and the Readout operations are shown in Fig 5.1.1. Two complex numbers to be multiplied enter the Multiplier at the rising edge of the clock, one RAM location is read, the two points multiplied and added to the

accumulation obtained from the RAM and at the next rising edge of the clock, the result is stored back in the same RAM location. The next clock cycle fetches data corresponding to the next Frequency channel and the operations already mentioned are performed and the result stored back in the next memory location of the on chip RAM. Since in the Non-Pol. mode p* and q* are supposed to be identical,the output of the MUX corresponding to a given channel does not change for two clock cycles (even if it changes, who bothers about it in Non-Pol. mode anyway !!).Thus it takes two clock cycles to perform integration on one channel. With the availability of 512 clock cycles in one FFT Cycle, one gets a max. of 256 channels in this mode. Since both the USB and the LSB are processed simultaneously, one can get a maximum Bandwidth of 32 MHz (2 X 16 MHz).

256 RAM locations are used to store the 256 channels. When STAREAD is asserted, data is read from the other half of the 512 X 36 RAM. One rising edge of the STAREAD signal results in reading out of 18 bits of a word. Therefore it takes two STAREAD pulses (or four clock cycles) to read one full 36 bit word as shown in Fig 5.1.1. Once 256 locations are readout, the emptied half of the RAM is used for accumulation and the data is read out from the other half and the same story repeats once again.

5.2. MAC OPERATION in POLARIZATION MODE I: Refer again to Fig 5.2 . In the Polarization mode , two FFT Engines of one block on one antenna perform FFT on Right (R) and Left (L) Circularly polarized signals of the same baseband (max 16MHz). Let's say p* and r* are (R) and q* and s* are (L) signals. Since MUXing is done at the rate of 32.25 MHz , with each clock pulse l* and m* change from (R) to (L) and vice versa.

Timing diagrams along with the various operations in this mode are shown in Fig 5.2.1. In one clock cycle, two (R) components from two antennas are clocked in, one RAM location that stores (RR) results corresponding to that channel is read, the two incoming points are multiplied and added to the number obtained from the RAM and the result is temporarily stored in an on-chip register. Next clock cycle, the input points are (L) and (L) from the two antennas and the same process is repeated and the result is stored in a different register. In the next clock cycle, two (R) components are multiplied together , added to the value stored in the first temporary register and the result is written back to the RAM. Similarly the (LL) result is written to the RAM in the fourth clockcycle. (RR) and (LL) results are stored in adjacent memory

locations. Since it takes four clock cycles to obtain one (RR) or (LL) product ,two adjacent channels are merged together and therefore the maximum number of channels that one can obtain is 128. However both the sidebands are processed simultaneously and therefore the maximum bandwidth that can be processed is still 32 MHz. Data readout operation is same as in the previous case.

5.3. MAC OPERATION in POLARIZATION MODE II: In this mode all the four correlations are to be obtained ie.— RR, RL, LR and LL. As for as the FFT outputs l* and m* are concerned, this mode is similar to Pol. Mode I. Output timings along with the necessary operations required to obtain the four correlations are shown in Fig 5.3.1 . In one clock cycle, two (R) inputs are multiplied together and added to the accumulation obtained from the RAM and the result is stored temporarily in a register. However this is where the similarity of this mode with the previous one ends. In the next cycle, to get the cross product, one of the inputs (say lx) is retained for one extra cycle. This retention of one input for an additional clock cycle is done internally by the ASIC chip specifying a proper control word at the start of the observation. Therefore in the next cycle, (R) from ANT 'X' gets multiplied with (L) from the ANT 'Y',added to (RL) accumulation obtained from the RAM and stored in a different register. Next cycle one gets (RR) and the result is written back in the RAM location from which (RR) was read two clock cycles ago. Next clock cycle, (RL) result is stored in the next RAM location and the story continues. This however gives only (RR) and (RL). Simultaneously the (LR) and (LL) products for the same baseband are accumulated in the second multiplier which was, in the previous modes, being used for a different baseband. Therefore in this mode, apart from loosing half the number of channels as in the Pol. I mode, maximum bandwidth that can be processed also reduces by a factor of 2 to 16 MHz (ie. only one 16 MHz baseband instead of two). Data readout is same as in the Non- Pol. mode.

5.4 MAC OPERATION IN DUAL-FREQUENCY MODE : In dual frequency mode ,the only change that takes place is that the two basebands (max 16 MHz) are from different obs. frequencies instead of being the USB and the LSB of the same obs. frequency. In this mode one cannot obtain all four polarization correlations. In Non-Pol. one gets 256 (max) channels while in Pol. I ,the maximum number of channels is 128. There is no change in the data readout operation.

6.MAC CONTROL CARD : MAC Control Card will be an interface between the Master Control

Card on one end and the MAC's on the other as shown in Fig 6.1. One MAC Control card will control eight MAC's. Apart from performing the control tasks, the MAC Control Card will also have buffers to store accumulated data which is readout from the ASIC's. This data will be later read out by LTA (Long Term Accumulator) for further integration.

6.1 TASKS TO BE PERFORMED BY THE CONTROL CARD :

(a) Mode selection at the start of the observations.

(b) RAM address generation for accumulation

(c) Generation of appropriate STAREAD pulses for reading out the accumulated data.

(d) RAM address generation for READOUT operation

(e) Address generation for self-test

(f) Generation of other control signals like

(i) RESET signals for various chips

(ii) various CHIP SELECT signals

(iii) MACWE for the ASIC in order to be able to write to the internal RAM during integration

(iv) AUXOUT for reading out the accumulated data from the ASIC

(iii) card select, array select, row, col (for accessing a particular ASIC at a particular location in a given array (or 4 X 4 block) of a particular card)

6.2 INPUTS TO THE CONTROL CARD : At the start of the observation, the Control card will get a 32 bit word from the Master Control card which defines the mode of observation and initializes the ASICs . These 32 bits will be clocked in serially into the ASICs by using PISO registers. One pin CRSFTCLK is available on the ASIC for clock input to input these 32 bits one by one.Four additional bits will come from the Master Control Card for selecting the appropriate time resolution.

Other two inputs to the Control Card from the Master Control are

(i) FFTINIT —-at the start of each FFT cycle

(ii) CLOCK

6.3 ADDRESS GENERATION : Address generation for Integration/STAREADOUT is quite straightforward. For 512 RAM locations, we require 9 address lines ie. 8 bits for 256 addresses and 1 bit for

selecting one of the two logically split memory banks. Addresses are stored in 512 X 8 PROMS (one PROM for Integration and the other one for READOUT). PROM address generation is through PALs (22V10).Ninth address bit comes from another PAL (16R8) which is used for generating some other control signals like MACWE ,Clear Acc., 16.125MHz clock etc also. All the address lines go to the same bus where the appropriate address is latched using 74ALS377 (octal FFs with tristated o/p).

6.4 STAREAD GENERATION : There are two possibilities :

(i) standard 128ms integration mode

(ii) non-standard user selectable time resolution modes (2ms, 4, 8, 16, 32 and 64ms).

For 128ms integration time, appropriate bit pattern to generate STAREAD will be stored in a PROM. Only one output bit is required to generate the required STAREAD pulses. This bit will remain LOW for first 512 clock cycles of an FFT Cycle and in the next 4 clock cycles, it will toggle to give two STAREAD pulses. Again the PROM is read by generating appropriate addresses through a PAL.

Non-standard mode requires generation of 16.125 MHz Clock which will be ANDed with appropriate time window to generate 256 STAREAD pulses continuously during the first 512 clock cycles of an FFT Cycle. Time Window will be implemented in a PAL input to which will be 3 bits corresponding to one of the Integration times mentioned in (ii) above . Another input to the PAL will be the 16.125MHz clock which will be ANDed with the Time Window. This ANDing will be implemented within the PAL. The clock input to this PAL will be FFTINIT pulse.

These two outputs will go to a MUX. MUX output will be selected by specifying a bit at the beginning of the observations.This bit tells whether the integration time is 128ms or one of the other six possibilities. This bit along with the three bits for selecting one of the six integration time in the non-standard mode will come from the Master Control Card. MUX will also be implemented in the PAL.

6.5 DATA STORAGE : There will be 144 line Data Bus for the eight MACs in a Chassis. Eight 18 bit wide RAMs will be available to store simultaneously the 18bits (half the word) coming at a time from each of the eight cards in one chassis. Memory bank corresponding to each card will have capacity to store

32 X 256 = 8k full words (36bit wide)

which are readout during one integration cycle. RAM size required for this is 16k X 18. Since 18bit wide

RAMs are not readily available,two 9bit wide RAMs will be combined to get a RAM width of 18bits.

Well, the story ends here and the following section summarises all that the GMRT Correlator System has to offer.

WHAT TO EXPECT FROM THE GMRT CORRELATOR SYSTEM :

1.Non-Polarization Mode : 32MHz Bandwidth 2 X 256 Frequency Channels.

2.Polarization I (RR,LL): 32MHz Bandwidth 2 X 128 Frequency Channels.

3.Pol. II (RR,RL,LR,LL) : 16MHz Bandwidth 1 X 128 Frequency Channels.

4.Dual Frequency Mode : 16MHz BW (each) 256(or 128) Frequency Channels (Mode 1.(or Mode 2.)).

5.Time Resolution : 2ms or 4ms or 8ms or 16ms or 32ms or 64ms or 128ms.

for time resolution less than 128ms , actual integration will be 1ms less than the time resolution values mentioned above

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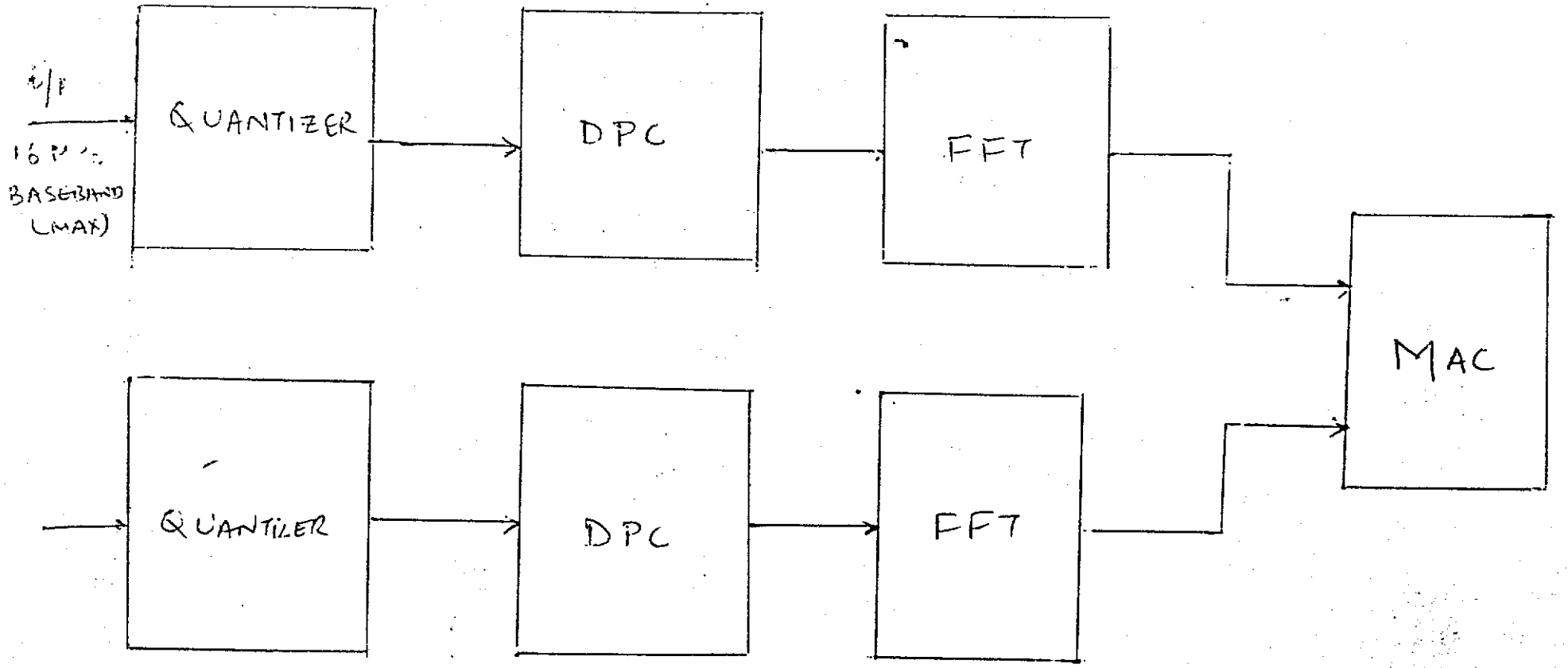


FIG. 1.1

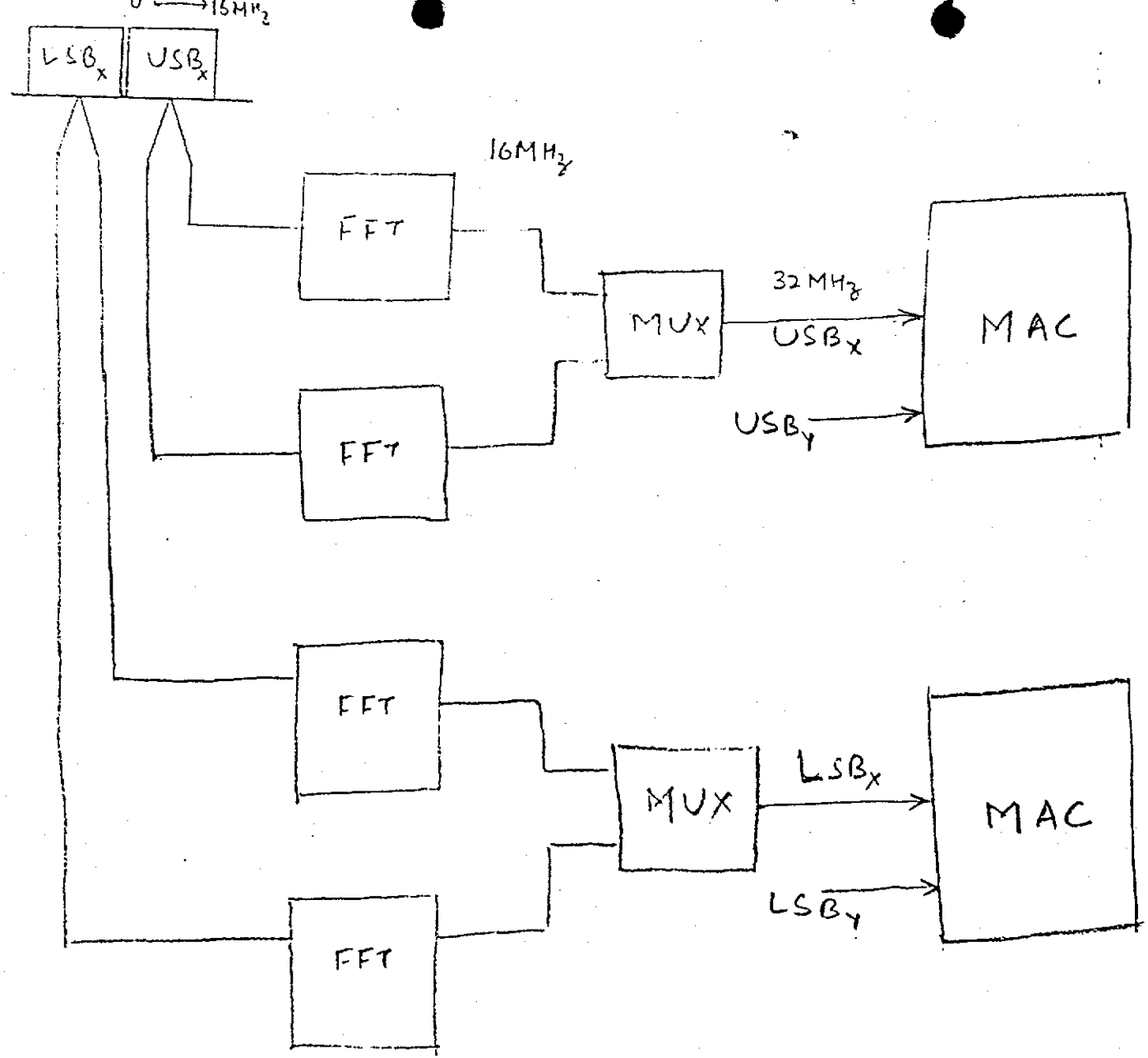

0 → 15MHz
LSB_x
USB_x
16MHz
FFT
FFT
MUX
32 MHz
USB_x
USB_y
MAC
FFT
FFT
MUX
LSB_x
LSB_y
MAC

FIG. 2.1

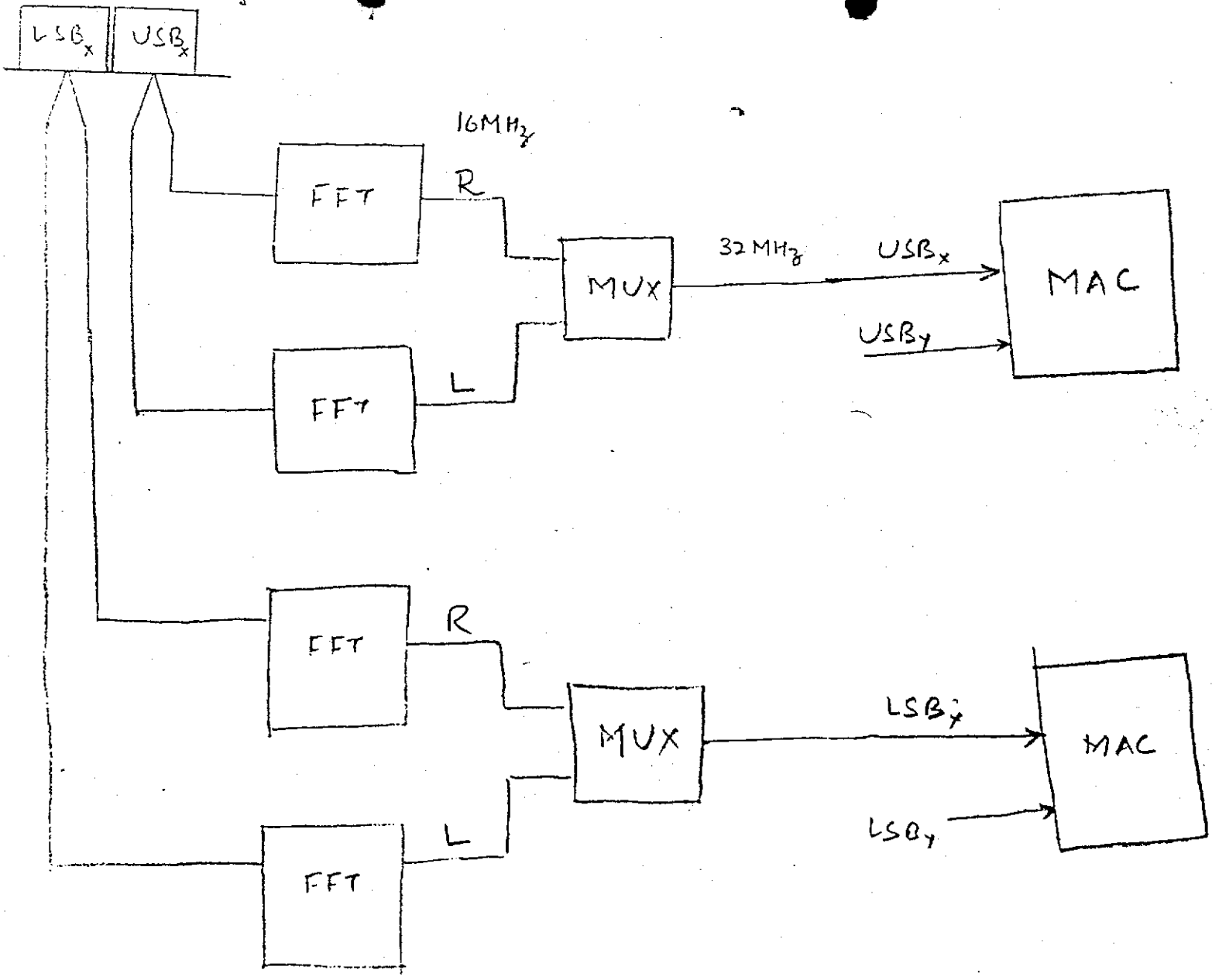

LSB$_x$
USB$_x$
16MHz
FFT
R
FFT
L
MUX
32 MHz
USB$_x$
USB$_y$
MAC
FFT
R
FFT
L
MUX
LSB$_x$
LSB$_y$
MAC

FIG 2.2

$R_x/L_x \Rightarrow$ Right Pol. in Clock & Left Pol. in the next from Antenna "X".

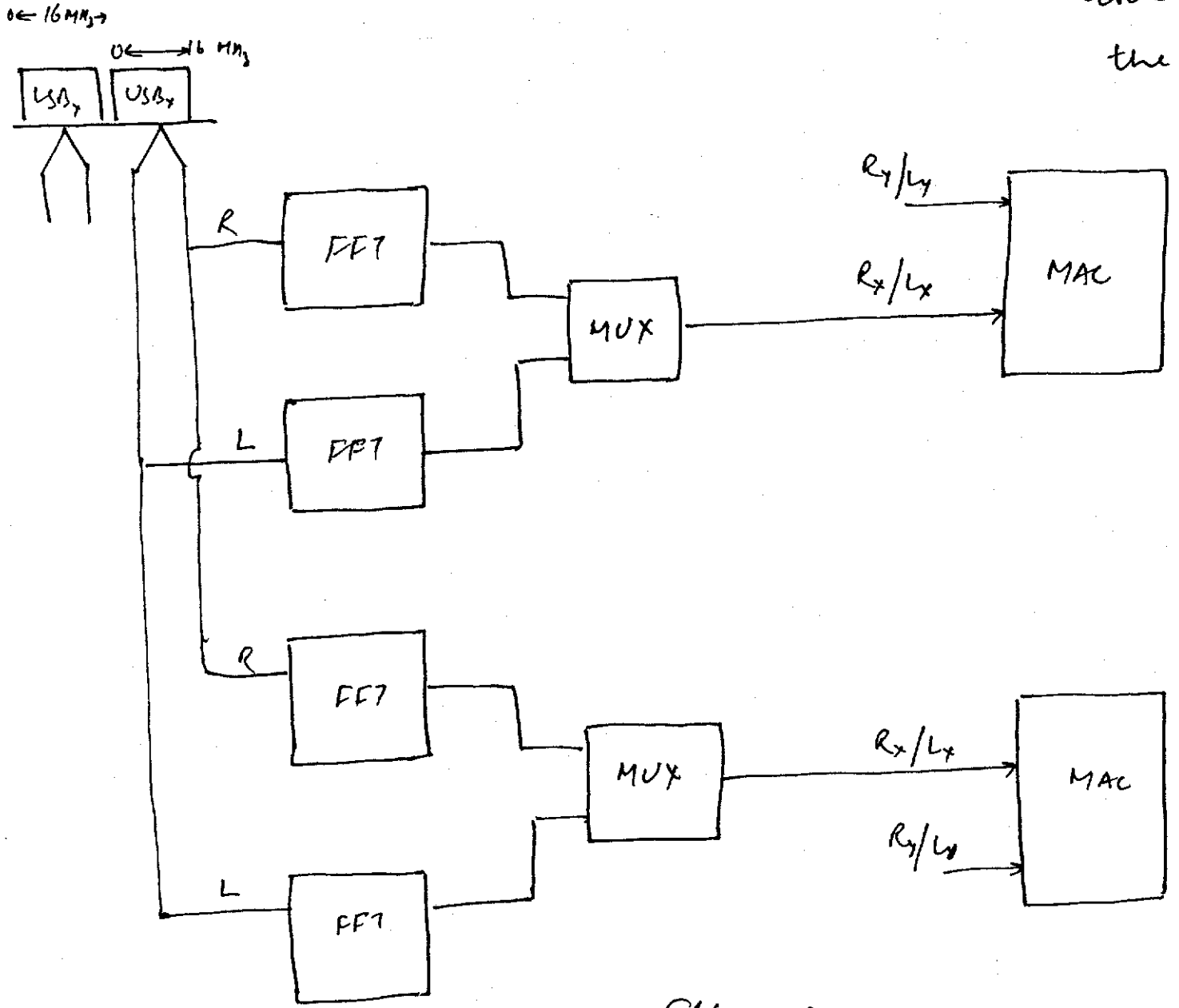


FIG. 2.3

f_1 AND f_2 ARE THE TWO OBS. FREQUENCIES

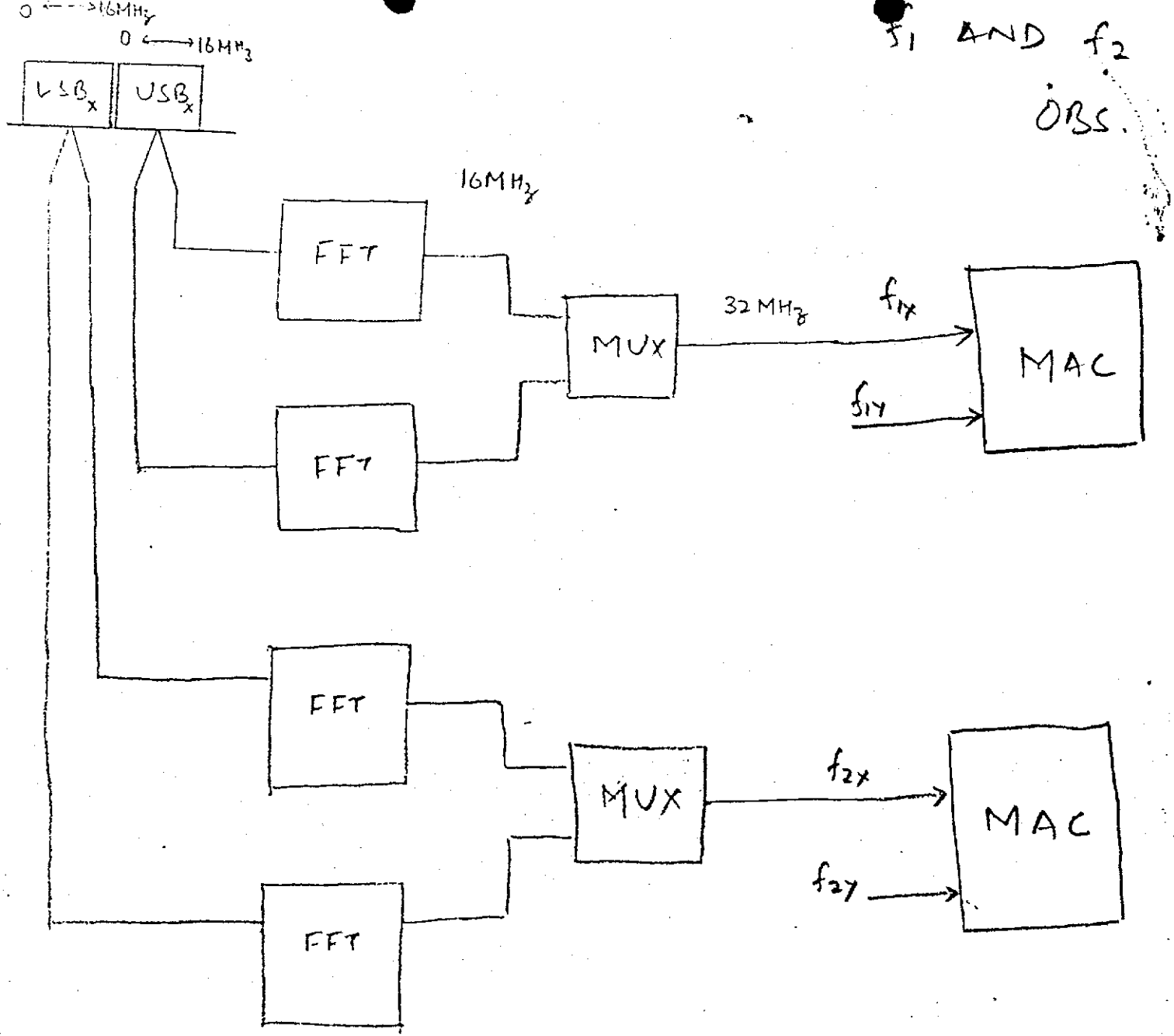


FIG 2.4

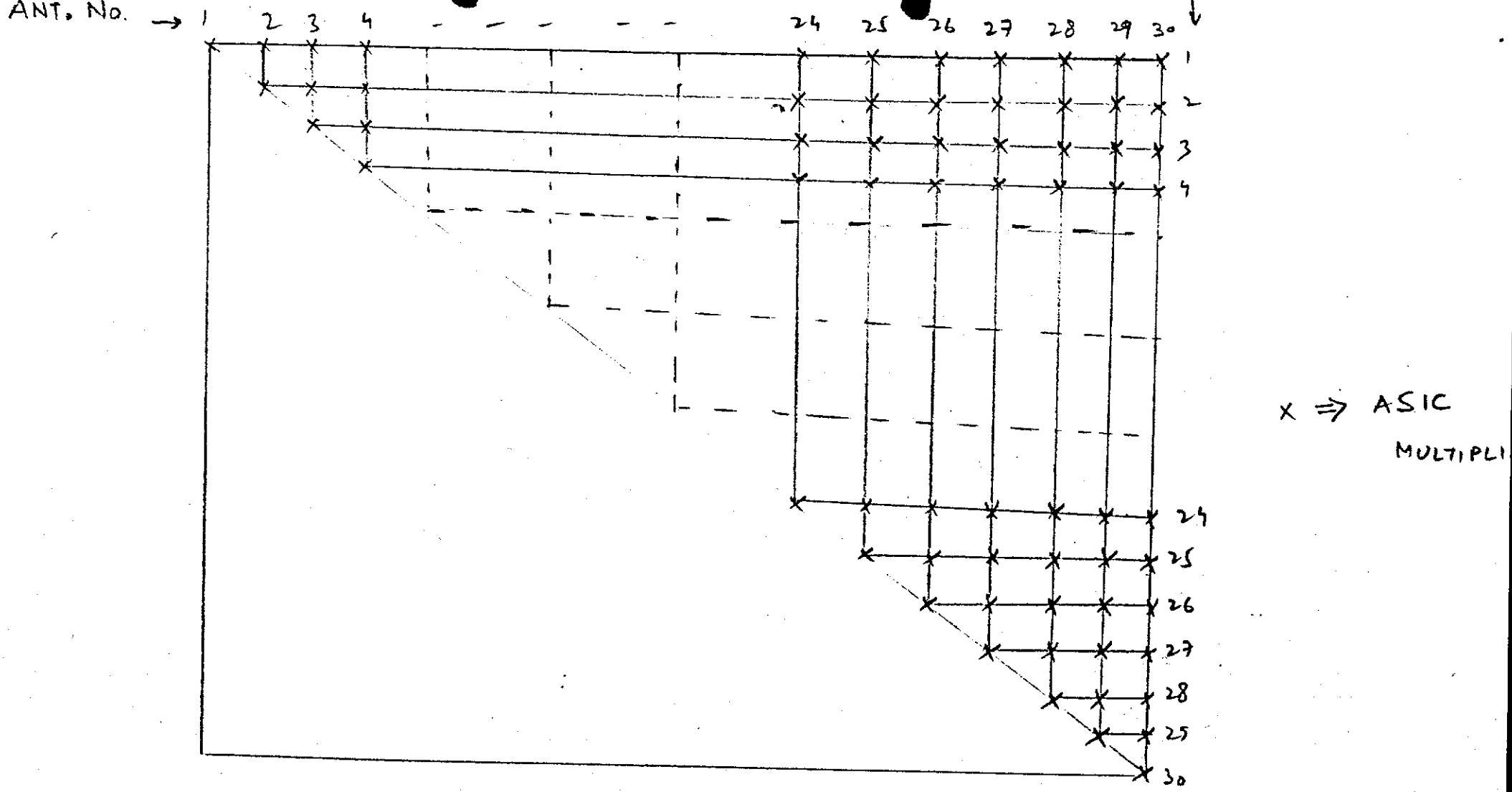
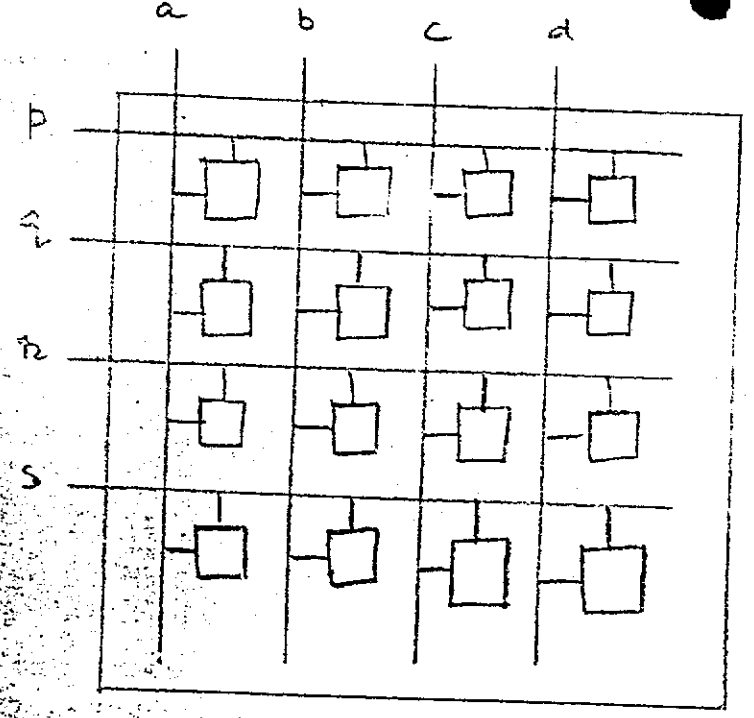

ANT. No. →
1 2 3 4 24 25 26 27 28 29 30
1 2 3 4 24 25 26 27 28 25 30
x ⇒ ASIC
MULTIPLI

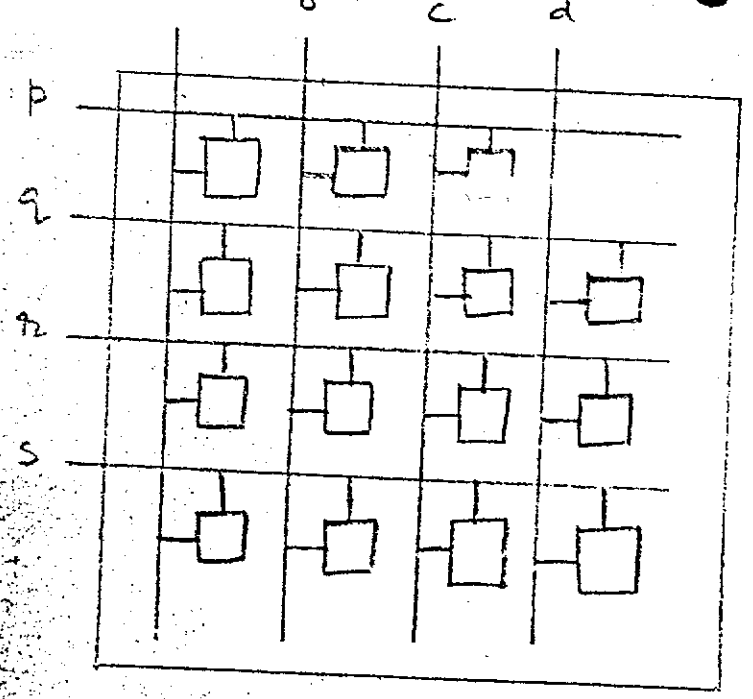
FIG. 3.1



TOTAL OF 21 CARDS WITH 2X16 ASIC's EACH

FIG 3.2(a)

CARD No.	ANT. (a)	ANT. (b)	ANT. (c)	ANT. (d)	ANT. (p)	ANT (q)	ANT. (r)	ANT. (s)
1	5	6	7	8	1	2	3	4
2	9	10	11	12	1	2	3	4
3	13	14	15	16	1	2	3	4
4	17	18	19	20	1	2	3	4
5	21	22	23	24	1	2	3	4
6	25	26	27	28	1	2	3	4
7	9	10	11	12	5	6	7	8
8	13	14	15	16	5	6	7	8
9	17	18	19	20	5	6	7	8
10	21	22	23	24	5	6	7	8
11	25	26	27	28	5	6	7	8
12	13	14	15	16	9	10	11	12
13	17	18	19	20	9	10	11	12
14	21	22	23	24	9	10	11	12
15	25	26	27	28	9	10	11	12
16	17	18	19	20	13	14	15	16
17	21	22	23	24	13	14	15	16
18	25	26	27	28	13	14	15	16
19	21	22	23	24	17	18	19	20
20	25	26	27	28	17	18	19	20
21	25	26	27	28	21	22	23	24

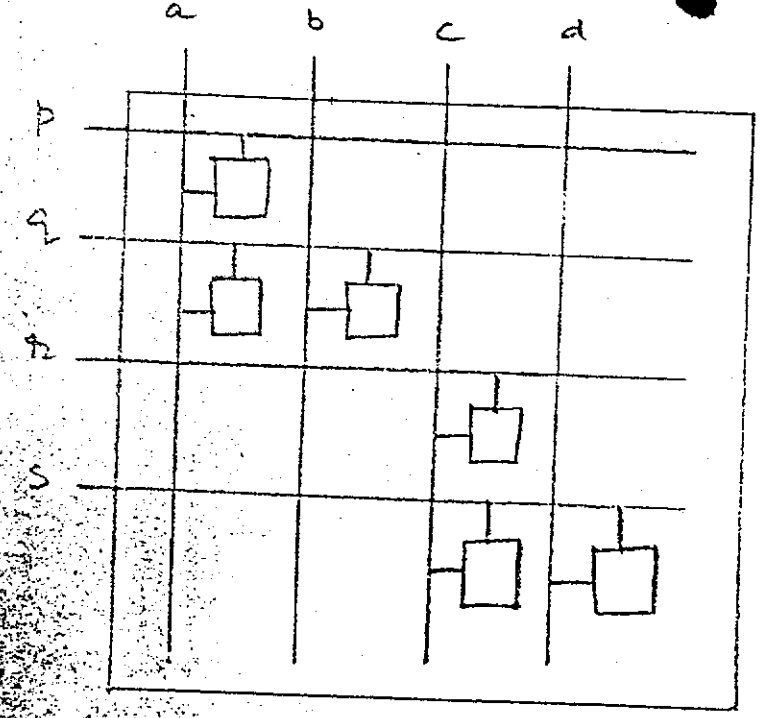


CARD No.	ANT. (a)	ANT. (b)	ANT. (c)	ANT. (d)	ANT. (P)	ANT (Q)	ANT (R)	ANT (S)
22	1	2	3	4	3	4	29	30
23	5	6	7	8	7	8	29	30
24	9	10	11	12	11	12	29	30
25	13	14	15	16	15	16	29	30
26	17	18	19	20	19	20	29	30
27	21	22	23	24	23	24	29	30
28	25	26	27	28	27	28	29	30

TOTAL OF 7 CARDS

WITH 15X2 ASIC'S EACH

FIG 3.2 (b)



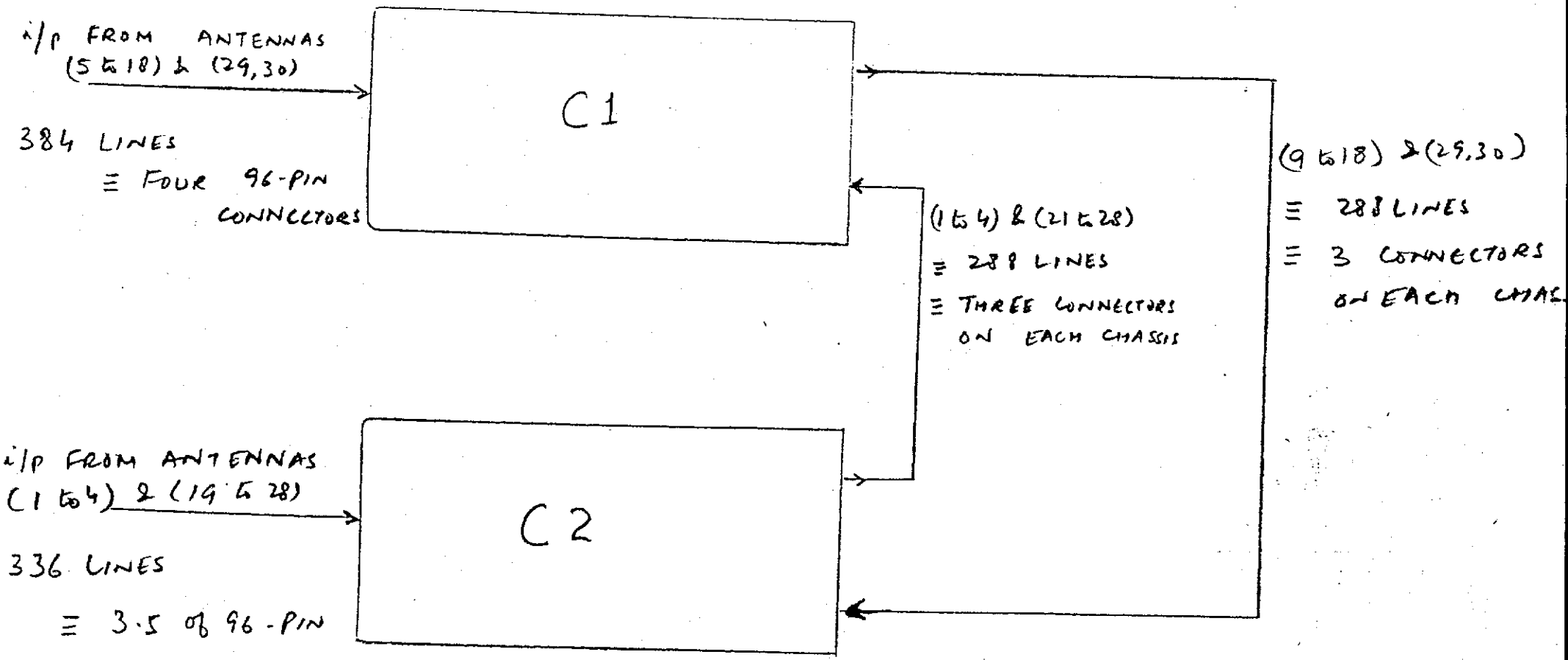
CARD No.	ANT. (a)	ANT. (b)	ANT. (c)	ANT. (d)	ANT. (p)	ANT (q)	ANT. (r)	ANT (s)
29	1	2	5	6	1	2	5	6
30	9	10	13	14	9	10	13	14
31	17	18	21	22	17	18	21	22
32	25	26	29	30	25	26	29	30

TOTAL OF 4 CARDS WITH 2 X 6 ASIC's EACH

FIG 3.2(c)

27, 29, 31

C1 " " " - 4, 5, 6, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 28, 30, 32



TOTAL OF TEN 96-PIN CONNECTORS PER CHASSIS

FIG. 4.1

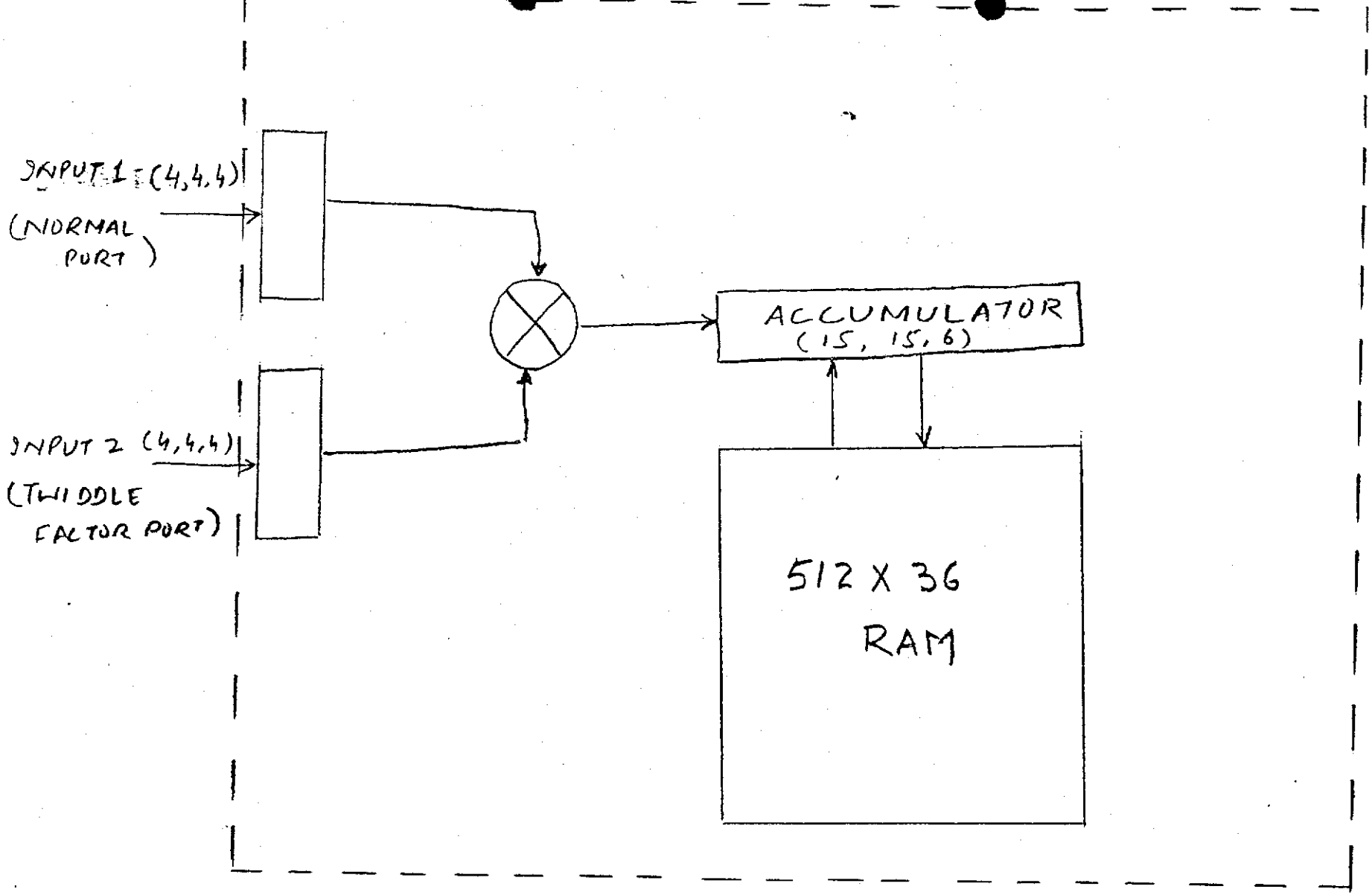

INPUT 1 (4,4,4)
(NORMAL PORT)
INPUT 2 (4,4,4)
(TWIDDLE FACTOR PORT)
ACCUMULATOR (15, 15, 6)
512 X 36 RAM

FIG. 5.1.

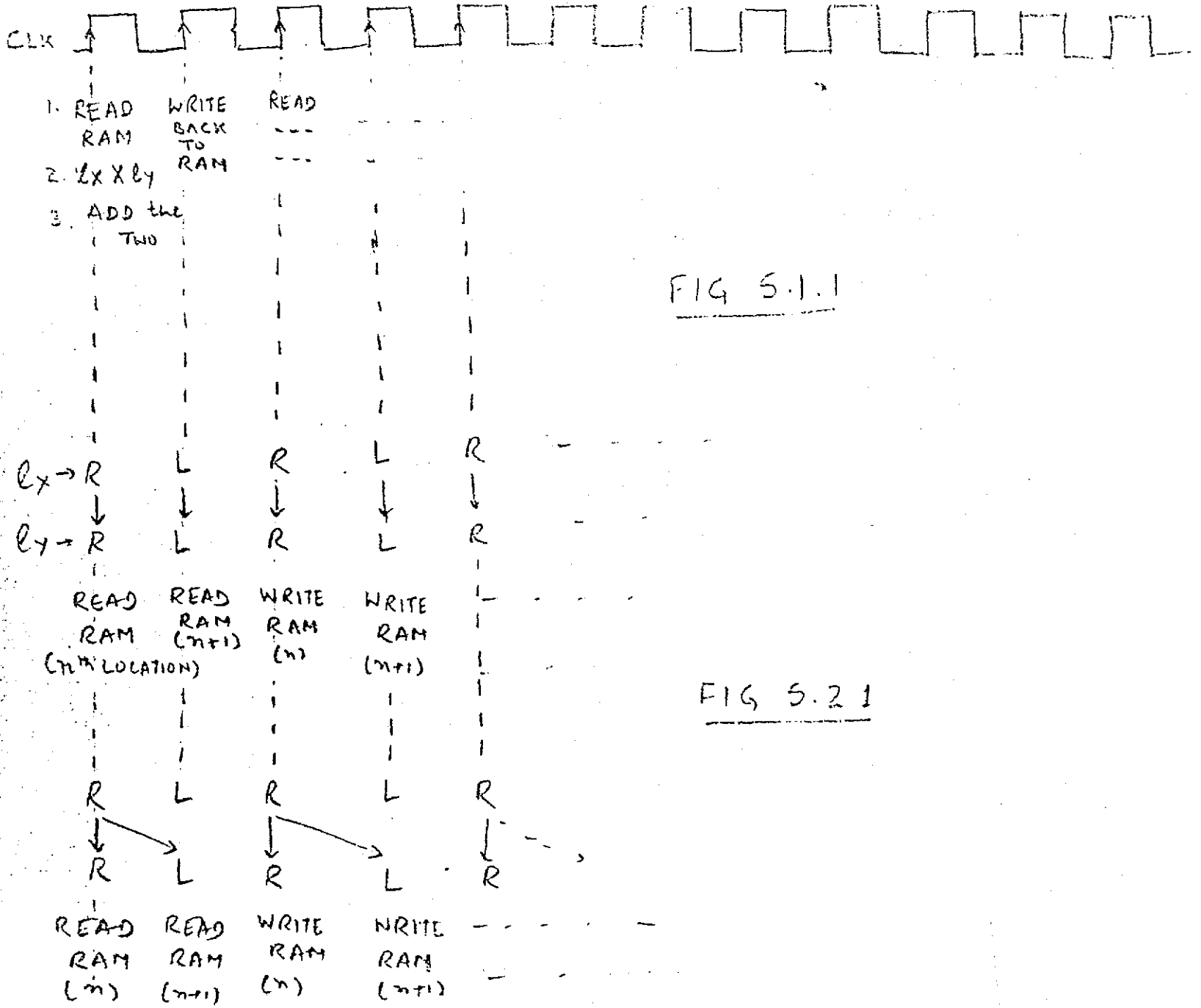


FIG 5.1.1

FIG 5.2.1

FIG 5.3.1

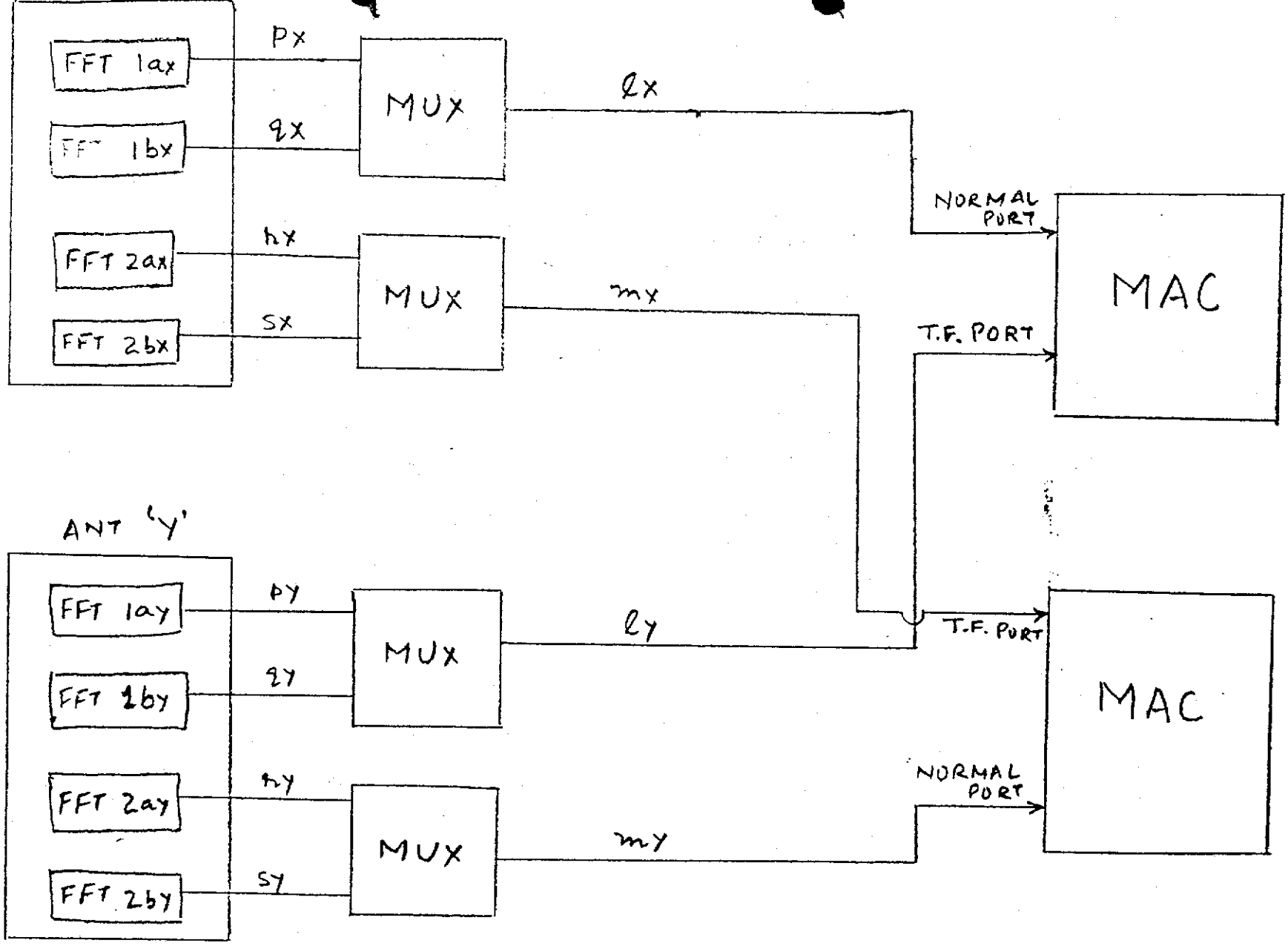

FFT 1ax
FFT 1bx
FFT 2ax
FFT 2bx
px
qx
hx
sx
MUX
MUX
Qx
mx
NORMAL PORT
T.F. PORT
MAC
ANT 'Y'
FFT 1ay
FFT 1by
FFT 2ay
FFT 2by
py
qy
my
sy
MUX
MUX
Qy
my
T.F. PORT
NORMAL PORT
MAC

FIG 5.2

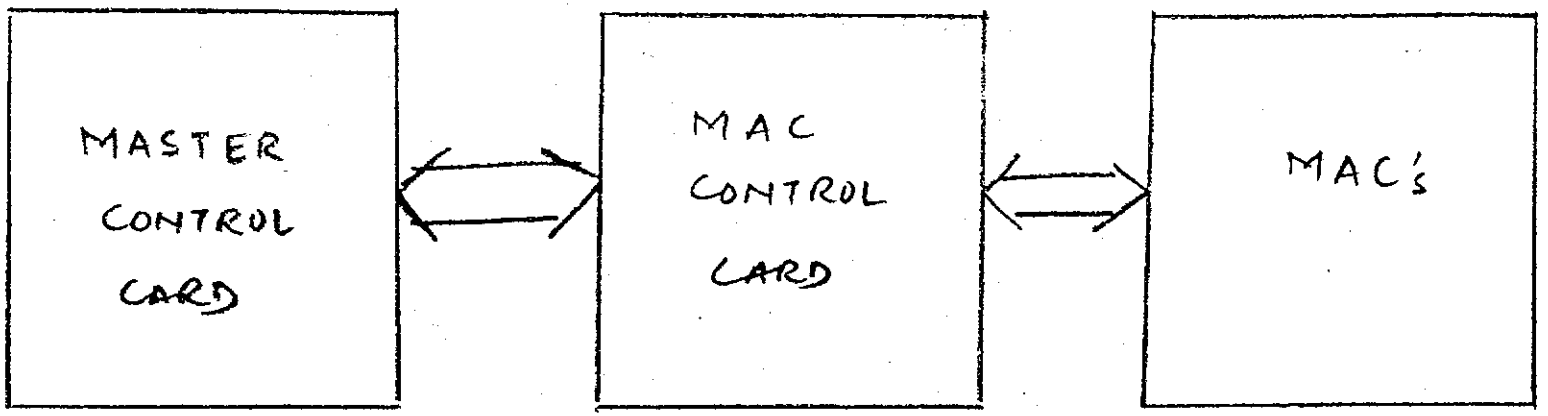


FIG. 6.1