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(Ref: rkm2/SPEC1/june)
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DYNAMIC SPECTROGRAPH : DESIGN DETAILS

Design details of a 256 Channel Digital Spectrograph are given in this report. The circuit described here processes a baseband of 16 MHz only giving a frequency resolution of 62.5 kHz and a time resolution of 4ms. Minor modifications which will be necessary to have one more FFT Pipeline, in order to have an option of obtaining a Cross Spectrum also for Solar Observations, are also mentioned herein. For test purposes, the Spectrograph will be interfaced with a Microprocessor Board which has been designed by Shukla. However the no. of signals required from the external Microprocessor Board has been kept to a minimum so that the survival of the Spectrograph is not dependent on any particular Microprocessor and later on when the Computer interface is changed to suit real time requirements of very high data rates, most of the Spectrograph Design will still be the same.

1. SPECIFICATIONS :

Max. No. of Frequency Channels	= 256
Max. Baseband Width	= 16 MHz
Max. Frequency Resolution	= 62.5 kHz
Max. Time Resolution	= 4 ms
No. of Sampling Bits	= 4

The circuit performs a maximum of 512 point FFT on real data and thus gives an output of 256 Channels. However provision has been made in the circuit for the user to select any of the following no. of channels :

256, 128, 64, 32, 16 or 8.

Further integration will be done in Software as per the requirements.

The user will also have an option of loading a known data in a RAM at the input to the FFT Pipeline

and performing FFT etc on the known data instead of Sampled Data in order to check whether everything is fine with the spectrograph or not.

Any desired Data Windowing Function can also be defined by the user.

2. FUNCTIONAL DESCRIPTION :

Block Diagram of the Spectrograph is shown in *Fig 1.* FFT Block consists of 5 ASIC Chips. Each ASIC is capable of performing either RADIX-4 FFT or RADIX 2 FFT. Whether a particular ASIC is going to perform a RADIX-2 or a RADIX-4 FFT is defined in the begining by loading appropriate ASIC Control Word. Through the ASIC Control Word, one can also define a "BYPASS" mode for one of the ASICs in which that ASIC just lets the data go through without performing any operation on the data. Exercising these options allows one to select the desired no. of channels at the output mentioned in the previous section. For 256 Channels and hence 512 -Point FFT, the First four ASICs perform RADIX-4 operations and the last stage is configured for RADIX-2.

As shown in the Schematic Diagram (Sheet 1 of 2), each ASIC is accompanied by a RAM bank. First RAM Bank stores the WINDOW Function ; the last one is for performing Fractional Sample Time Corrections while the remaining three RAM banks store the Twiddle Factors (Sin/Cos Factors).

Each ASIC has two 512 X 18 internal RAM Banks. While one of the RAMs is being loaded with data, FFT is performed on the data in the other RAM.

With each Rising Edge of the 32 MHz Clock, one Data-point and one Twiddle Factor point enter the ASIC through "Normal" and "Twiddle " Port respectively. The whole FFT block is pipelined so that every 32MHz clock cycle, there is one input and one output. Output of the FFT goes to MAC (Multiplier and Accumulator) where it is squared and integrated and thus Power Spectrum obtained.

The "NORMAL" Port of the ASIC is 18 Bit wide (7 bits Real, 7 bits Imaginary and 4 bits for Exponent).Width of the "TWIDDLE" Port, however, is only 10-bits. Even though the output of the FFT is in (7,7,4) Format, only 12 bits in the (4,4,4) Format are fed to the MAC because of the restrictions imposed by the availability of the input pins on the ASIC as "TWIDDLE" Port is used as one of the Input Ports in the MAC Mode.

That is as far as the functioning of the Spectrograph goes for a user not interested in hardware details.

Remaining of the report describes in detail the operation of the Spectrograph Card.

3. OPERATION DETAILS:

For using the Dynamic Spectrograph successfully, the following set of operations have to be necessarily performed :

(i) Loading of the RAMs (U1C, U[5,7,9,11,13]A and B; ref. Sheet 1 of 2) and FIFO (U35A; ref. Sheet 2 of 2)

(ii) ASIC Control Word Loading

(iii) Generation of Control Signals during FFT and MAC operation.

(iv) Data Read Out to Some Storage Device

3.1. RAM and FIFO Loading:

The Spectrograph stays in "IDLE" state after "POWER - ON" until it receives a **STRTRMLD** pulse from the Microprocessor Board. Hereafter the first task that is performed is the loading of the RAMs and the FIFO. RAM (U1C) contains the Known Data, RAM Bank2 (U5A and U5B) together contain the Window Function, RAM Banks3 to 5 (U7A and U7B; U9A and U9B; U11A and U11B) are loaded with the Twiddle Factors and finally the RAM Bank6 (U13A and U13B) stores a phase ramp for fractional sample time corrections. The FIFO (U35A) is loaded with ASIC Control Words for 6 ASICs (5 for FFT and 1 for MAC) - a total of 24 Bytes plus one Byte for defining the mode of operation.

Each Byte of the data to be loaded comes from the external microprocessor board with a "WRITE" pulse – **WEP** $\diagdown$. The incoming data goes to the RAMs through Buffers (74ALS541's). With the rising edge of WEP , the Buffers are released from "Tristate" by **BUFx** $\diagdown$ signals which are followed by "WRITE ENABLES" to the RAMs **RWEx** $\diagdown$. **BUF** and **RWE** signals go to all the RAM Banks but the "Chip Enable" signals – **CE** x to different RAMs are generated selectively so that at a time, data is written to one RAM only .

Generation of these **CE** signals is directly related to the appearance of **CYx** signals (ref U3A). **CYx's** are generated by (U4C) by counting the no. of Carry pulses - **LCY** generated by (U4A). With the appearance of every **CY**, address counter is reset for the next RAM Bank. Generation of reset pulse – **RMADDRST** in this manner is necessary because same address counter is being used for so many RAM's of unequal sizes.

After all the six RAMs have been loaded, FIFO is loaded after resetting it. All the operations described in this section are asynchronous. Detailed TIMINGs can be seen in *Fig.2 and Fig.3.*

3.2. Control Word Loading :

Control Word is loaded into the ASICs serially with **SFTCLK** of 16MHz. This data is read from the FIFO. The last Byte is latched in (U39B). First bit of this latched byte is for selecting the MUX (U1E) at the input and the next 3 bits are for selecting the no. of channels from among the options mentioned in section 1. Control Sequences required for this operation are read from a PROM (U38B) by continuously incrementing the Address (U38A). Details are available in *Fig. 4.* Generation of **CY6** indicates the end of the Asynchronous operation.

3.3. Control Signals for FFT and MAC Operation:

After the Asynchronous Operation of RAM Loading, ASIC Control Word loading etc. is over, the Spectrograph waits for a **START** pulse to start the Synchronous operation of FFT and Integration. With the **START** pulse, all the "Chip Enable" – **CE** s – go LOW thus selecting all the RAMs. RAM o/p Enable and INIT signals are generated thru a FFT Sequencer. FFT Sequencer repeats the pattern every 516 Clock Cycles as shown in *Fig. 5.*

Signals required for the MAC operation – *Fig. 6* – are generated by another Sequencer shown in the "Dynamic Spectrograph Control" sheet. Since Addressing in the MAC mode, unlike the FFT mode, is external, two Address Counters – (U32A and U32B) are used — one for Addressing that half of the internal RAM in which Accumulation is taking place and the second one for Reading Out that half of the RAM which is not being currently used for the purpose of integration. (Details of MAC Mode operations are mentioned in *rkm1/MAC/march.*)

3.4. Data Readout for Storage:

18 bits of data readout from the MAC is temporarily stored in (U42A, B, C). Once these RAMs get filled up, signal **CY7** is generated telling the Microprocessor Board to start reading out the data. Data Reading out is again an Asynchronous Operation. **RDP** $\searrow$ from the processor is used for incrementing the address. Data is sent out One Byte at a time by using **GENBL** [1,2,3] signals to enable the Buffers sequentially. **LEP** $\searrow$ is used to tell the Microprocessor Board that valid data has appeared on the i/p

Data Port of the Processor. Timing details are given in *Fig. 7.* This setup is tentative and is to be used in the debugging stage only. For real time operation, VME/ SCSI Interface options are being explored.

4. MODIFICATIONS for X-SPECTRUM OPTION:

Modifications required for this options are literally minor. As shown in *Fig. 8*, this will involve just another FFT Pipeline but no change in the Peripheral Components or the Logic. Fifth bit of the latch (U39B) will be used to select the MUX's for obtaining the X-Spectrum. With this configuration, it would be possible to either obtain a Dynamic Spectrum over 32 MHz Band or X-Spectrum along with Power Spectrum across 16 MHz Baseband.

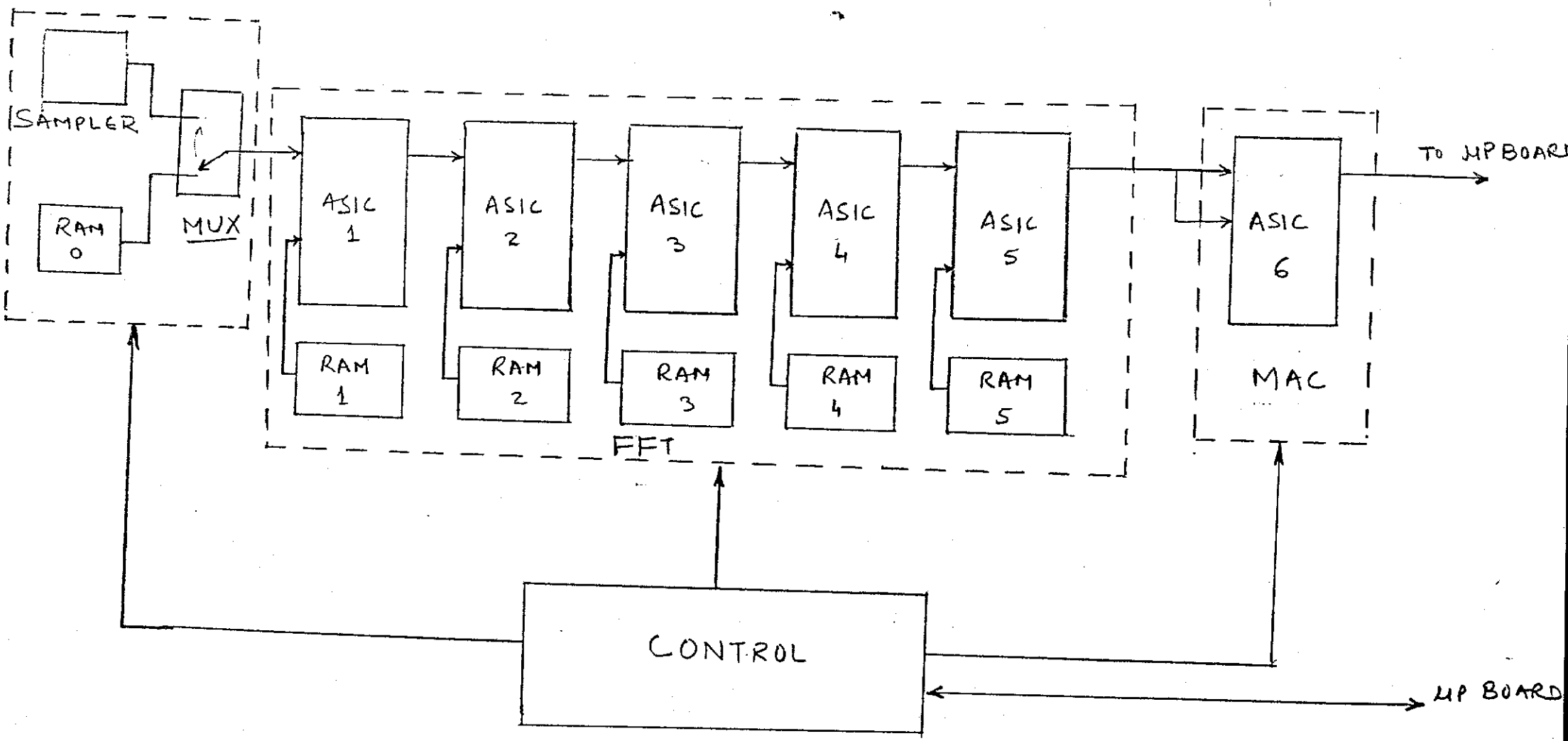

SAMPLER
RAM 0
MUX
ASIC 1
ASIC 2
ASIC 3
ASIC 4
ASIC 5
ASIC 6
RAM 1
RAM 2
RAM 3
RAM 4
RAM 5
FFT
MAC
TO HP BOARD
CONTROL
HP BOARD

FIG. 1

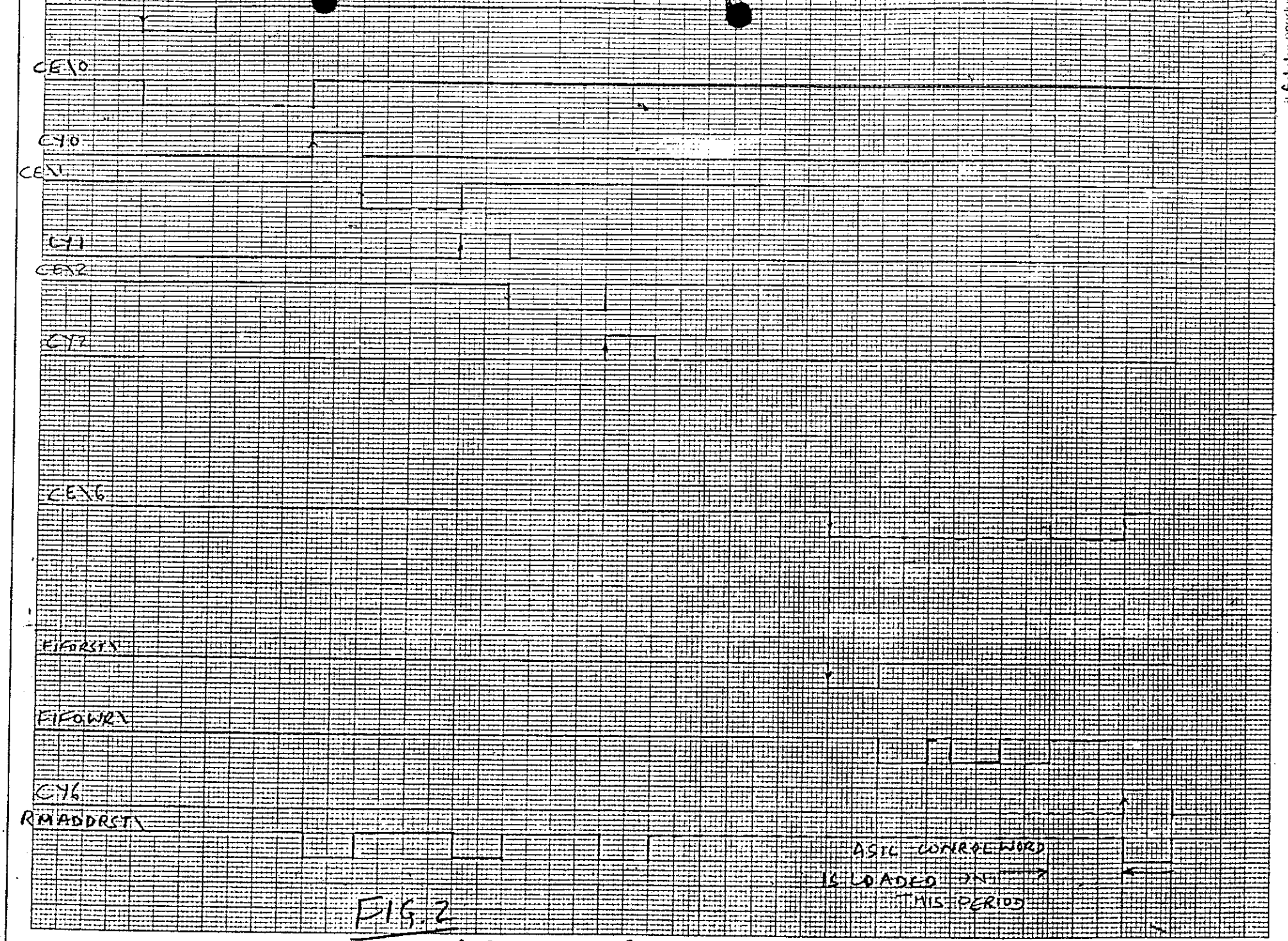


FIG. 2

CHIP SELECT SIGNALS FOR RAM.

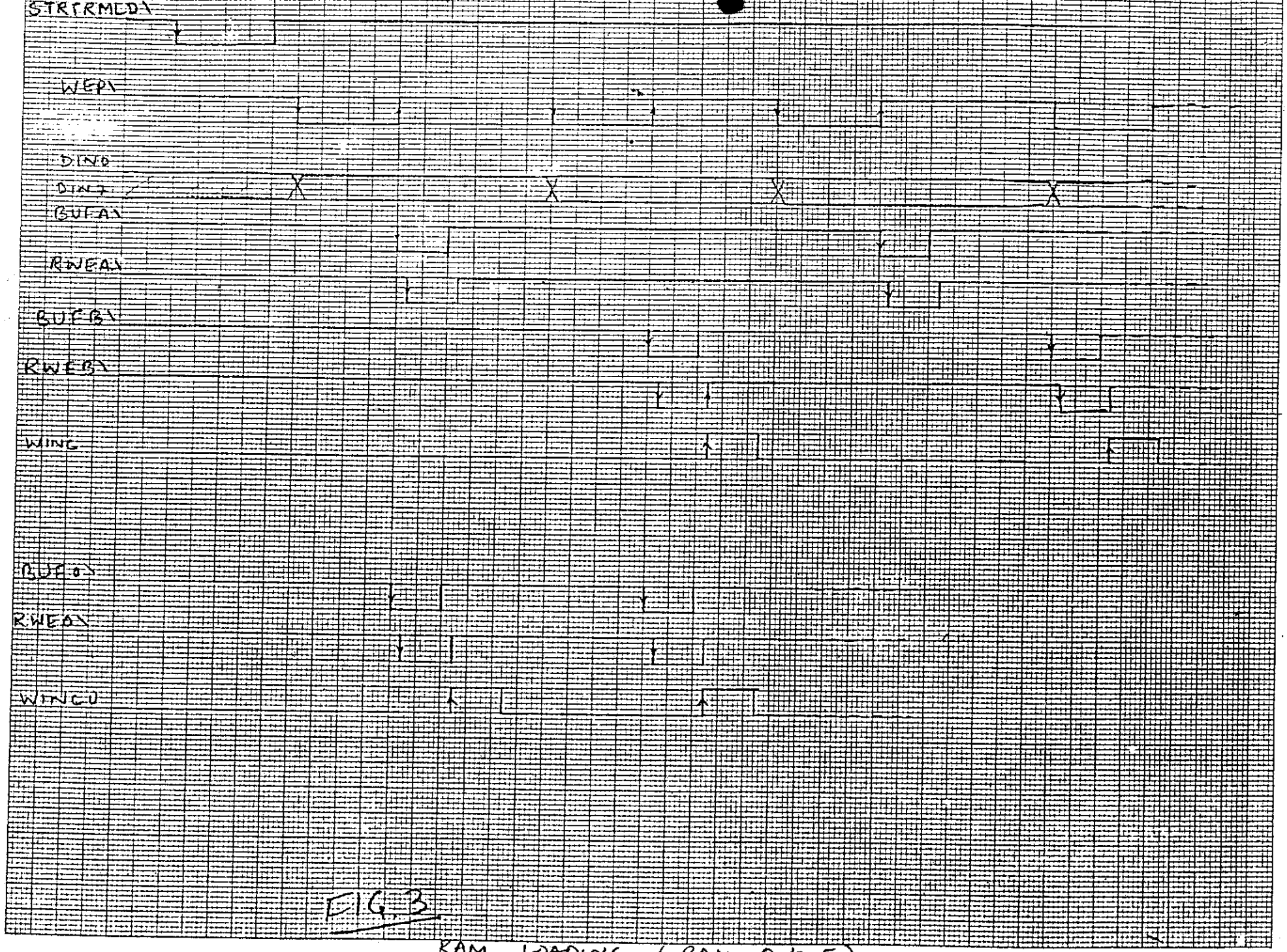


FIG 3

RAM LOADING (RAMs 0 to 5)

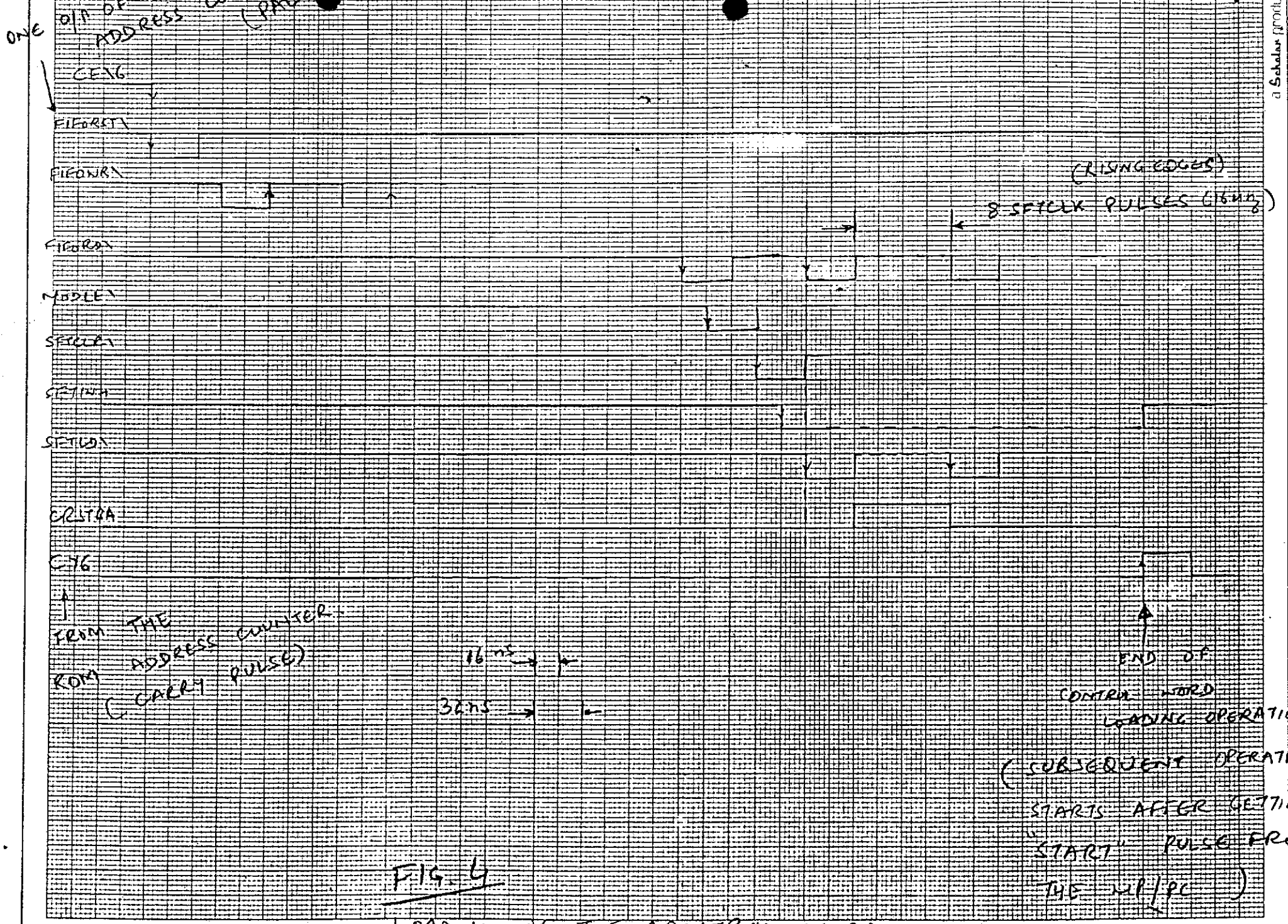
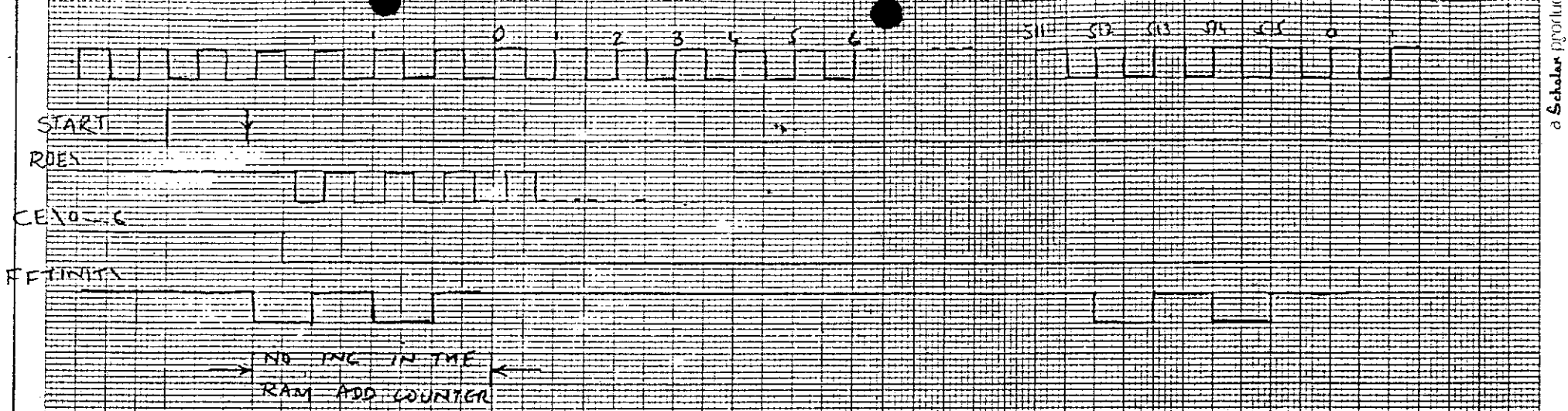


FIG. 4

LOADING OF THE CONTROL WORDS



ALL OTHER "INITs" ARE

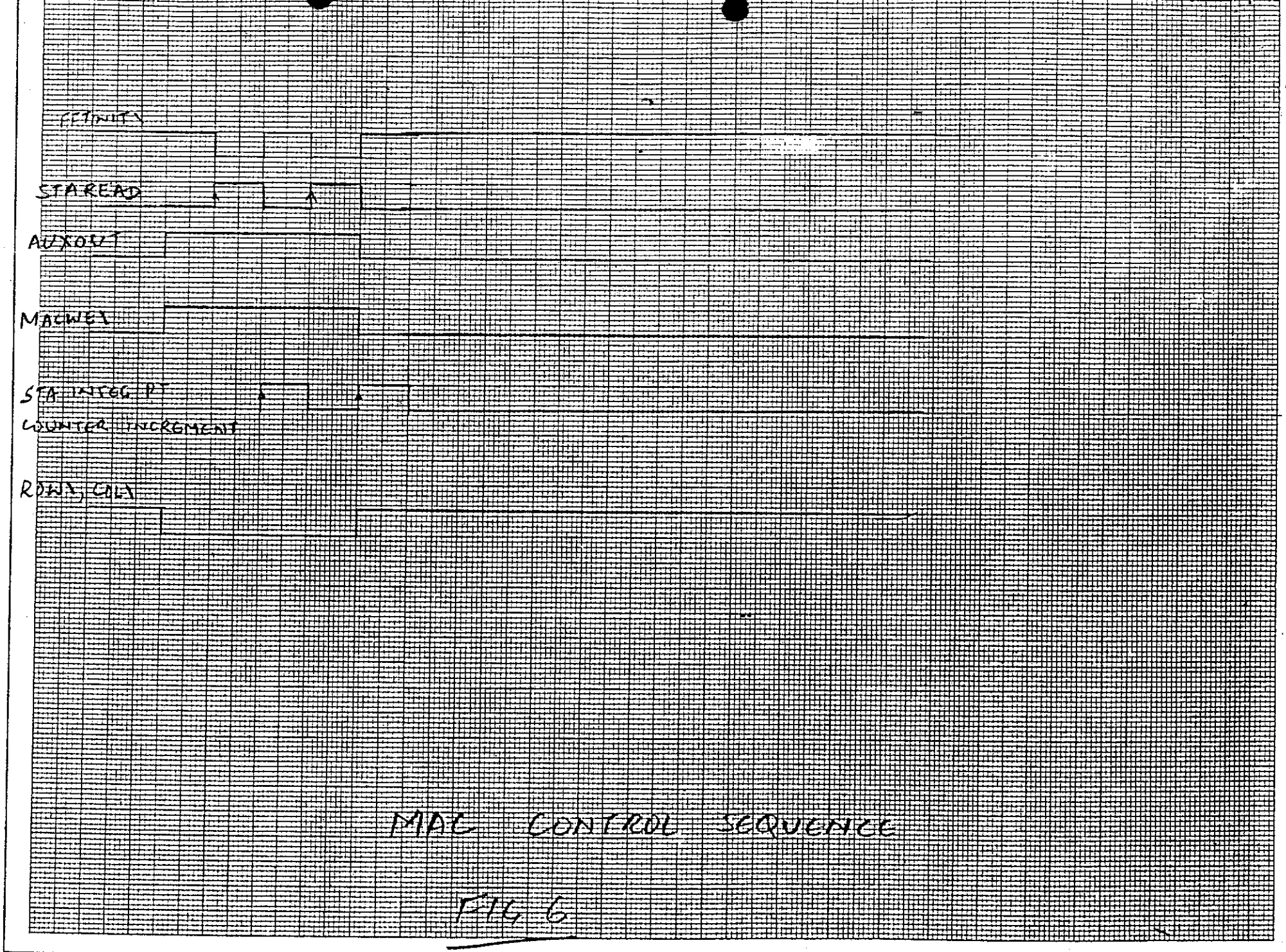
DERIVED FROM "FFTINITs"

WITH 11 Clock DELAY BETWEEN

ANY TWO SUCCESSIVE INITs

FIG 5

FFT SEQUENCER



MAC CONTROL SEQUENCE

FIG 6

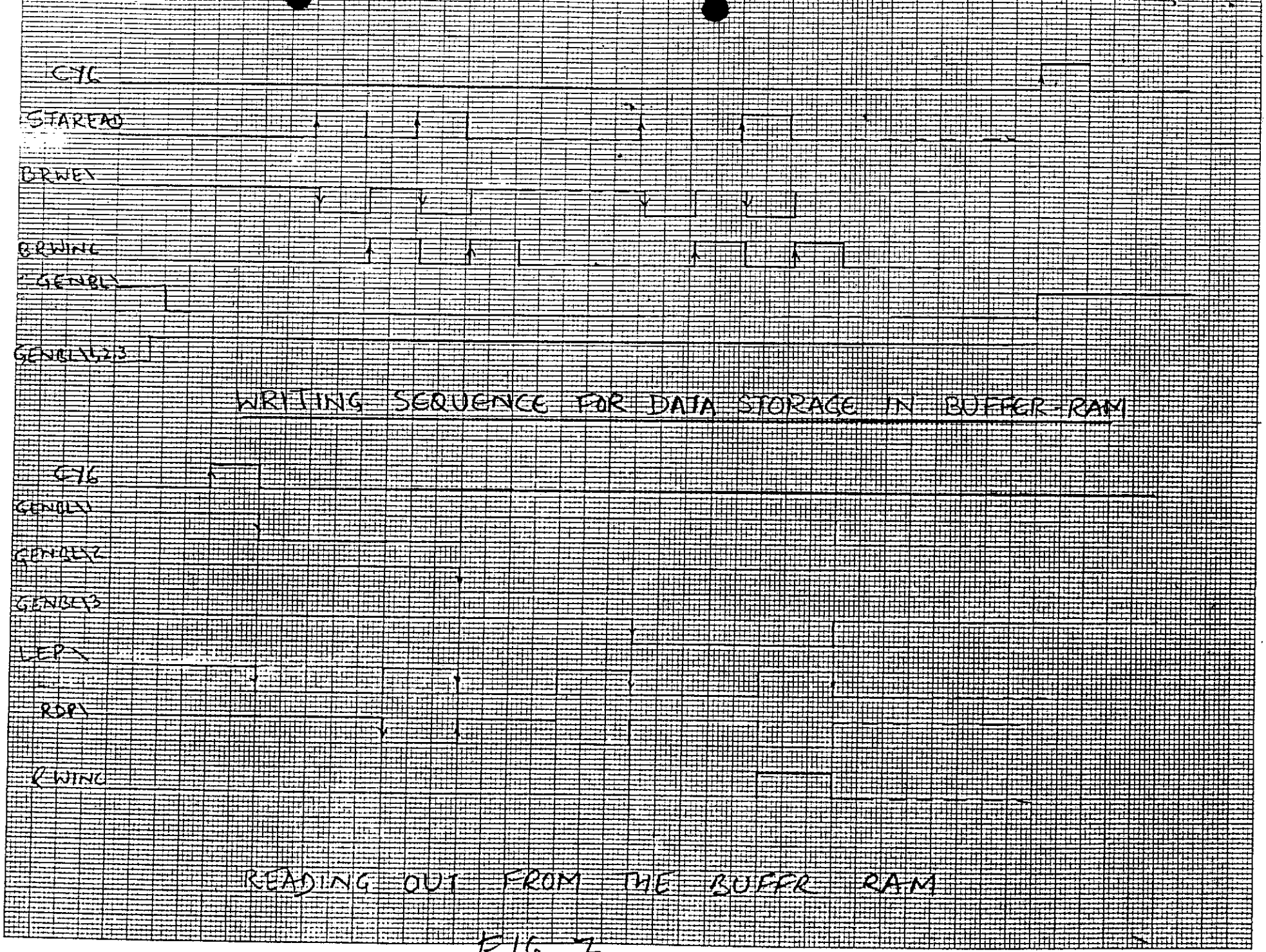

CYC
STAREAD
BRWEN
BRWINC
GENBLK
GENBLK2,3
WRITING SEQUENCE FOR DATA STORAGE IN BUFFER-RAM
CYC
GENBLK1
GENBLK2
GENBLK3
LEP
RDEN
R WINC
READING OUT FROM THE BUFFR RAM

FIG. 7

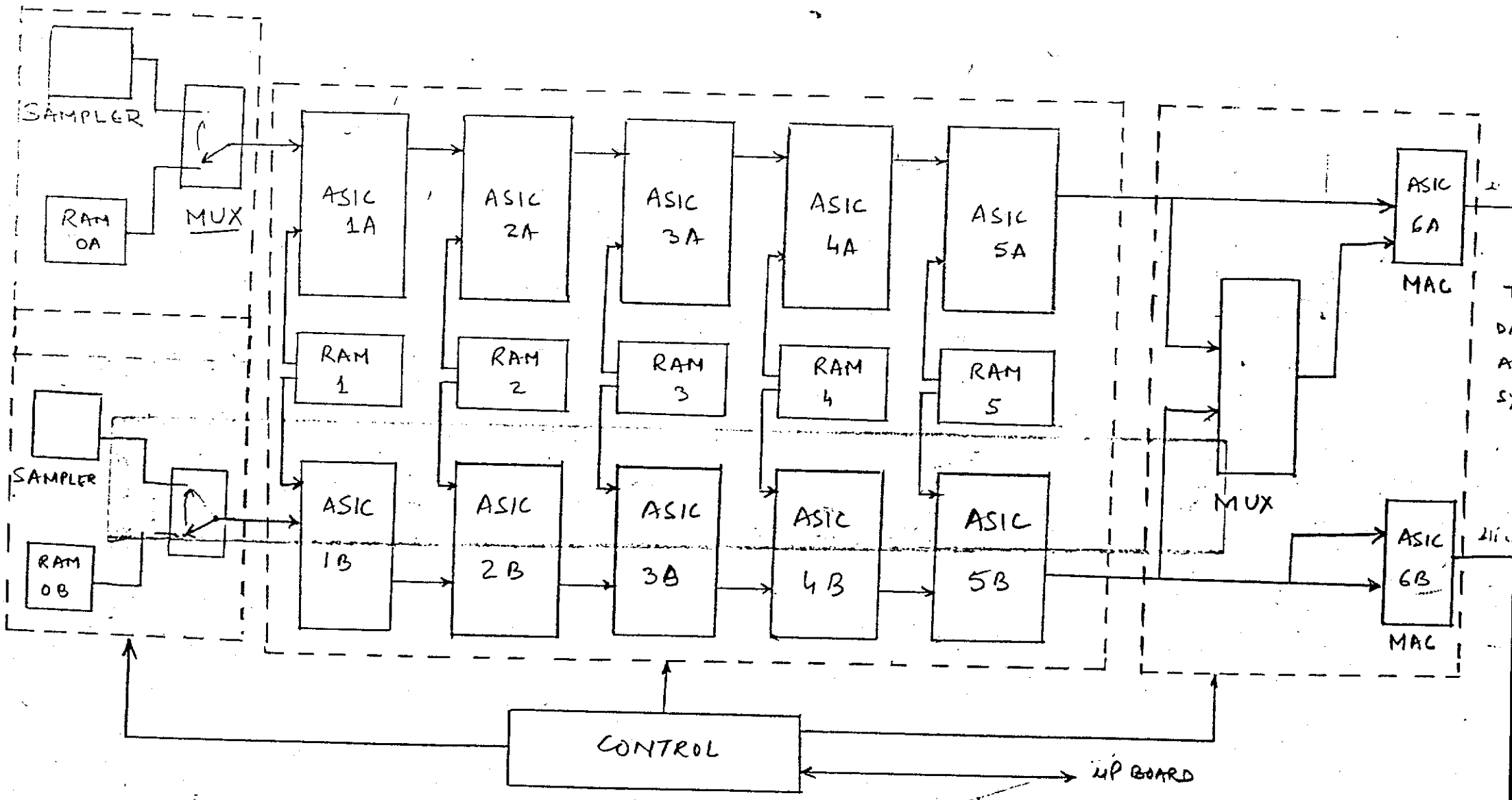
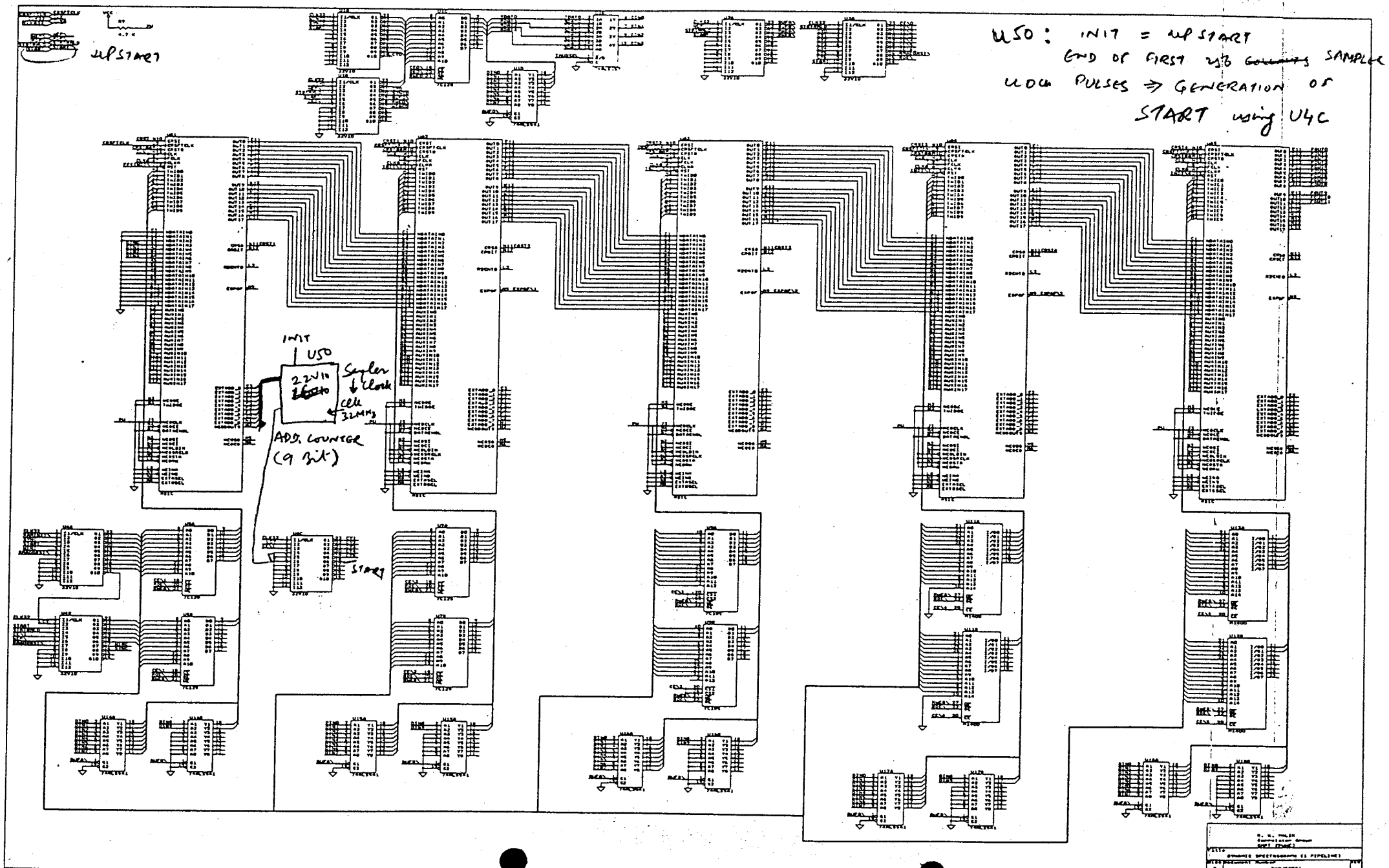

SAMPLER
RAM 0A
MUX
ASIC 1A
ASIC 2A
ASIC 3A
ASIC 4A
ASIC 5A
ASIC 6A
MAC
RAM 1
RAM 2
RAM 3
RAM 4
RAM 5
SAMPLER
RAM 0B
ASIC 1B
ASIC 2B
ASIC 3B
ASIC 4B
ASIC 5B
MUX
ASIC 6B
MAC
CONTROL
µP BOARD

FIG. 8


U50 : INIT = UPSTART
END OF FIRST 256 SAMPLE
CLOCK PULSES ⇒ GENERATION OF
START using U4C
UPSTART
INIT
U50
22V10
Sampler Clock
CLK 32MHz
ADD. COUNTER
(9 bit)
START