GMRT CORRELATOR CARDS

(Note: This is very sketchy, and partially reflects the status till June 1991. Refer to documents of related cards for a more accurate information.)

The various signal processing operations in the GMRT Correlator System is performed in the following types of cards, with the arrows indicating the direction of signal flow.

Sampler ==> DPC ==> FFT ==> MAC ==> LTA ==> Data Acquisition/archival

(DPC: Data Preparation Card LTA: Long-Term-Accumulator
MAC: Multiply-Accumulator card)

These signal processing cards are controlled by 3 types of control cards:

Master Control for the overall timing etc,
FFT Control Card
MAC Control Card

All these control cards are based on 8751 microcontroller with which the Array Control Computer can interact.

A brief outline of the functions of these cards is presented below.

1. Sampler Card: Accepts 4 analog input signals, digitises them at 32 Ms/s in 4-bit sign-magnitude form, and outputs the signals to Data Preparation Card.

   Total Number of Cards: 60 for 120 samplers
   Card type: 4-layer, 6U (4U?) cards, individually shielded 7T enclosures for RFI
   Chassis: 5 chasses in a single rack
   User-selectable options: none

   (Note: Sampler clock and the corresponding clock for DPC input is at a slightly slower rate by a factor 512/516 compared to DPC output, FFT and MAC clocks.)

2. Data Preparation Card(DPC): Accepts 4 x 4-bit words at 32 Ms/s rate; validates every v'th sample; reallocates the input streams into 4 channels in one of 3 modes for bandwidth selection (16 MHz or 32 MHz total per polarization); flips the sign-bit as per the Walsh function sequency introduced at the antenna; validates and selects data at the Nyquist rate (say 32/v Ms/s); buffers the valid data; reads from the buffer at 32 Mw/s; re-allocates the data streams into one of two possible schemes of channel-allocation (polarization selection; full or RR/LL); outputs the data in ECL differential form to the appropriate FFT card.

   Total no. of cards: 30 for 120 channels
   Card type: 4-layer, 6U (9U?) cards
   Chassis: 3 chasses
   User-selectable options:
   overlap factor = 32 MHz/(effective sampling rate) = v
   Input channel select = AB, AA, BB
   Output channel select = full pol, RR/LL only
   Delay update

(Except delay update by FFT control card every STA cycle, all other parameters are set once every session only. Overlap factor is constant for both polarizations of a given frequency band, while fixed delay is constant for a given polarization of both frequency bands.)

3. FFT card: Accepts 4 x 4-bit words at 32 Mw/s rate; performs fringe rotation by multiplying by exp(i.phase); performs FFT of size 32, 256 or 512; compensates for fractional delay errors (Fractional Sample Time Correction: FSTC); outputs the data in ECL differential form to the MAC cards and the pulsar machine.

Total number of cards: 30
Card type: 10-layer, 9U cards with 3 x 96-pin + 1 x 60 pin connectors
Chassis: 3 chasses with 10 cards each
User-selectable options:
FFT size = 32, 256, 512 [= (no. of spectral chan)/2]
Fringe phase: initial value and rate of change
FSTC: delay ramp

(Fringe phase and FSTC are updated by the FFT control card)

4. MAC card: Accepts a pair of complex numbers (4,4,4 format) every clock cycle from two FFT engines, multiplies them and adds the result to one of the 256 short-term-accumulators (STA) present inside the ASIC. There are 3 distinct modes of operation: (a) RR mode, in which a pair of numbers is accepted every alternate clock cycle, i.e., every 64 ns, and accumulates the product into the STA -- this mode gives twice as many spectral channels as in the other modes; (b) RR,RL mode, in which FFT outputs are received every clock cycle, but one of the numbers is assumed to be common to two consecutive products -- thus only one new number is read in every second clock cycle; (c) RR,LL mode -- a pair of numbers is read every clock cycle and the product accumulated in the STA memory. In the last two modes, consecutive products of the same type are accumulated into the same STA location, and thus there will only be 128 maximum spectral channels. The STA results are read out during the pauses in FFT cycle, one result being read out in every FFT cycle per ASIC. It is assumed that the FFT outputs corresponding to R and L channels are multiplexed and appear in the same input pins.

Total number of cards: 64
Type and size: 8(?)-layer, 9U x 280 mm;
with 3 x 96-pin + 1 x 50 pin connectors
Chasses: 7 chasses total with 9/10 cards + one controller in each.
User-selectable options:
Polarization mode = [RR,LL], [RR]/[LL], [RR,RL]/[LL,LR]
Maximum number of channels = k
STA integration cycle = 128 ms default;
provision for smaller integration times from 8 ms.

(All options are defined at the start of a session, and are implemented indirectly by the Multiplier control card)

5. LTA Card: Gets the STA results from all the multiplier cards; converts them from ASIC internal floating point to IEEE floating point format (2 x 32 bits complex); provides a dual buffer for storing the complex correlations;adds results across frequency and/or time; applies bandpass calibration.

Number, type of cards: not finalised, probably accommodated within the MAC control cards by including a fast processor and

adequate memory buffer.

User-selectable option(all options defined once every session)
Bandpass calibration = 256 complex numbers
Channel select: ALL or any subset of spectral channels
Spectral smoothing: adds adjacent spectral channels
Integration factor: adds consecutive samples of each channel

(Total input data rate - from all LTA cards - is 23080 complex words to be read every 128 ms, about 2 Mword/s where a word is assumed to to hold a complex number. With a 24-bit floating point representation (3 most significant bytes of IEEE floating point word), this amounts to 12 MB/s. The output rate depends on the user option, but current plan is to restrict it to a maximum of 0.5 MB/s.

6. Master Control Card: Provides clock distribution to all the FFT, MAC LTA, DPC cards by providing the necessary sequencing pulses to the appropriate control cards;

Number of cards: One
Type of Card: 9U x 280 mm; design under development
Location: not finalised
User option: None

7. FFT Control Card: Provides the FFT cycle sequences to the FFT cards (10 FFT cards are controlled by one FFT control card); Loads the FFT card RAMs with the trigonometric functions required at each stage; Loads all the ASIC control words determining the window, FFT size, FSTC implementation; Periodically communicates (a) fringe phase and rate of change to FFT cards, (b) fractional part of delay (clock cycle units) to FFT cards; Communicates with the Array Control Computer to obtain the model parameters and the FFT control words.

Number of cards: 3 (Each controls 10 FFT cards)
Type of card: 9U x 280 mm; probably 4-layer PCB
Chassis: Located along with the FFT cards being controlled by it
User options:
FFT size (common to all 4 FFT engines in a card)
Window (size 512 words)
Fringe phase and its rate of change
Delay and rate of change
(Pulsar Gate generator is not finalised yet)

MAC Control Card:
Generates all ASIC control words and external addresses required for the MAC operation including STA readout; distributes the various MAC sequencer pulses received from Master control card to the MAC cards (upto 10 MAC cards are controlled by one control card.) provides buffer for STA results which can be accessed by the LTA or other data acquisition system.

Number of cards: 4 (Each controls 8 MAC cards)
Type: 9U x 280 mm; probably 4 layer PCB
Chassis: Located along with the MAC cards controlled by it
User options:
All MAC control options are actually implemented here
STA read-out is also controlled here, hence time-resolution (8,16,32,64 or 128 ms) is actually chosen here.

9. Correlator Control Card: Provides a communication interface between the Array control computer and the various microcontrollers within

the correlator system. Not finalised yet. Essentially a single-board computer with multi-drop serial links (RS 485) to various microcontrollers within the correlator system (all are 8051 family) and Probably linked to the Array control computer through a high speed serial link. Only the Fringe and delay parameters (and perhaps pulsar model parameters if pulsar gate generator is implemented) need to be updated periodically. All other parameters are defined only once at the beginning of each session. The fringe and delay parameters are expected to be communicated to the FFT control card once every few seconds (both values and their rate of change need to be specified, assuming variation to be linear with time)

. Data Acquisition Card: Reads the correlator outputs from the LTA cards, provides some elementary real-time functions including data-compression, archives data on Exabyte tapes and simultaneously writes the data on the File-Server disk using the NFS protocol on the ethernet.

Number of Cards: Two (One will suffice for 128 kB/s archival rate)
Type of Card: Sun 1E single-board-computer based on SPARC processor, with on-board memory (4 MB), ethernet, SCSI, 2 x RS 422 ports; Real time operating system (VxWorks) is used
Size: 6U, VME card

(Connected to the LTA cards through the VME bus, and to Online computer system - File Server - through a dedicated ethernet link.)