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DIGITAL SPECTROGRAPH USING FX CHIPS - data acquisition

crs/26.3.91

As the first hardware exercise using the FX chips, it is planned to build a digital spectrograph, which can record power spectra for 256 channels for a signal of bandwidth upto 4 MHz. It consists of an 512-point FFT engine (5 FX chips) and a 256-channel MAC card (1 FX chip). The FFT and MAC will operate at 8 MHz clock, which is slower than the GMRT correlator. The slow speed helps in triggering a quick activity, since all components should be locally available. All efforts will be made to have a working system during May 1991. The details of the spectrograph are being worked out by Rakesh Malik and will be described in a separate note. This note mainly concerns with the data acquisition using 80C452 microcontroller-based card.

The basic scheme will be kept as close to the default operating mode of the GMRT correlator as possible, except for the reduction in operating speed. Thus, each FFT cycle will consist of 516 clock cycles, out of which 4-tick duration will be a "dead time" used for internal operations rather than processing input data. The short-term-accumulator (STA) readout will also occur during this dead time. During the 4 ticks of the dead time, two 18-bit words will be read from the MAC, which together constitute one 36-bit complex word. The word will be latched into five output registers, accessible to the external microcontroller card for reading.

From the point of view of the power spectra, it is only necessary to record the real part (6 bit exponent, 14-bit mantissa, sign-bit always zero). However, in order to facilitate some initial experiments to help understanding the operation of the FX chips as well as for signal-processing experiments, the hardware will have provision to read the full 36-bit complex word. The selection of reading only the real part is done at software level in the microcontroller.

The following is the sequences of operations leading to transfer of STA results from the multiplier chip to the microcontroller.

A. microcontroller loads address (8 bit) of the STA
B. microcontroller sends a request for read (by outputting 1 bit)
C. MAC reads the corresponding 36-bit word during the next available dead time and latch the data on to 5 registers (2 for real part one for exponent and 2 registers for imaginary part).
D. At the end of read-out in the previous operation, MAC will raise an interrupt to the microcontroller; also, if the previous address was 255 (1111 1111b), will perform a bank-switch operation.
E. On receiving the interrupt signaling availability of STA results in in the 5 registers, microcontroller will read these 5 registers, convert the 36-bit complex word into two 32-bit integer words, and provide Long Term Accumulation (LTA) for a user specified number of STA cycles. (Each STA cycle is 0.512 sec.) Typically, the LTA cycle lasts for 10 sec, consisting of 20 STA cycles. At the end of LTA cycle the accumulated results will be communicated to an online computer connected via RS232 port at 9600 baud.

Note: The 36-bit complex notation for the STA values has the (15,15,6) format as follows:

bit 1 (msb)	: sign of real part
bits 2-15	: magnitude of real part
bits 16-21	: common exponent (base 2) for real and imaginary parts, with an IMPLIED negative sign. (All numbers will be numerically less than or equal to 1)
bit 22	: sign of imaginary part
bits 23-36	: magnitude of imaginary part.