Correlator System Document - Introduction

INTRODUCTION

The purpose of this document is to bring a comprehensive overview of the GMRT Correlator System and to spell out the plans and invite suggestions from astronomers as well as engineers for helping us to build a friendly and versatile correlator system for the GMRT. Much of the implementation of the architecture described in these pages is expected to be finalised by mid-1991. On the basis of this document, we intend to review the system design within the next couple of months. Although component procurement process has already begun, we are sure there is room for considerable improvement without hurting the procurement plans.

Before giving details of the GMRT Correlator System, a summary of various signal processing operations performed by the GMRT correlator system will be provided in Chapter II. Chapter III will give a brief outline of the functions of the major types of cards present in the system. A functional overview of the system is presented in Chapter IV, which will include the specification of individual modules with some comments of interest to the users. Subsequent chapters will present schematic description of each card along with supporting block diagrams.

The features presented in the following chapters are all intended to be made available in the system targeted for operation in 1993. Due to logistic problems, we expect very few prototypes to be available this year. However, this is unlikely to affect the availability of a usable system when two antennas are ready with prototype analog electronics in operation. This is mainly due to the resemblance of the FFT-multiplier portion of our system to that of the system being built by the National Radio Astronomy Observatory, USA for their VLBA project. Thus it is in order to discuss what we propose to deliver during this year so that the users and engineers building the rest of the GMRT are generally aware of what to expect. This will be done towards the end of this chapter.

THE VLBA FX CHIP

Since our correlator system will be based on the 1.5 micron ASIC designed by the NRAO engineers, a brief description of this chip will be given first. The ASIC is designed to perform the FFT and multiply-accumulate (MAC) operations (the "FX" operation) in a fully pipelined system capable of handling 32 Ms/s. The chip has two primary operational modes -- the FFT and MAC mode -- depending on the control word specified to it. In the FFT mode, it can perform a radix-4 or radix-2 butterfly operations (or straight through). Within one clock cycle of 32 nanosec, it can accept two complex inputs (one data sample and one "twiddle factor"), perform one complex multiplication followed by addition to an accumulator, exchanging a complex word between the accumulator and the internal RAM, output one complex word from an alternate RAM buffer. This implies two inputs, one output, one internal RAM access, 4 multiplications and 4 additions -- all within one clock tick of 32 ns! Another way of expressing the processing power is to recall that the equivalent operations imply 256 Mflops and simultaneous i/o of 1472 Mbits/s . To give the reader a scale of the number of operations performed in an FX correlator, the GMRT system uses 1650 of these ASICS in a fully pipelined system operating at 32 MHz - a horendous sustained processing power of over 400 gigaflops.

In addition to the operations mentioned above, each FX chip has two more features: internal RAM and a number-controlled oscillator. The internal RAM consists of two memory banks - organised as 512 x 18bit words in the FFT mode and 256 x 36-bit words in the MAC mode for each bank. Each chip has also a 10-bit slice of a number-controlled-

oscillator (NCO) which can be cascaded with adjacent ASICs for better accuracy.

The ASICs are designed for pipelined operation and can be cascaded to obtain larger size FFTs. In the GMRT system, we have cascaded 5 ASICs to be able to perform 512-point FFT.

In the MAC operation, the FX chip has 3 distinct modes - two capable of different data streams coming in every 32MHz cycle ("polarization mode") and one assuming a single data stream entering in alternate cycles ("non-polarization mode"). In the non-polarization mode, it is assumed that the ASIC receives a pair of complex numbers every 64 ns. It will then multiply them and add to consecutive locations of internal RAM consisting of 256 accumulators. The polarization mode was designed specially to suit an application where the outputs of FFT engines handling right and left-circular polarizations (R and L) are multiplexed as is the case with both VLBA and GMRT correlators. In this case, the chip receives a pair of complex words in every 32 ns clock cycle. Let us call these R1,R2 in one cycle and L1,L2 in the next cycle. Then in the normal polarization mode the chip can be instructed to generate R1 * R2 (called RR for brevity) in one cycle and R1 * L2 (RL for brevity) in the next cycle. One can thus obtain RR,RL or LR,LL using this mode. To obtain both pairs, it is essential to have two independent ASICs for the correlation.

In addition to the above MAC operations, the NRAO engineers have also introduced a third mode at our request which we intend to exploit for the GMRT application. In this mode, one can use the same chip to obtain both RR and LL. This mode enables us to double the bandwidth of correlators without increasing the multiplier chips, but adding more FFT engines and sacrificing cross-polarization products of the type RL,LR. This is particularly significant since we are anyway providing 32 MHz support for the FFT engines for pulsar observations.

Currently, we have procured all our requirement of the FX chips from LSI Logic Corporation, the manufacturers.

THE VLBA FFT AND MULTIPLIER BOARDS

Our decision to base the GMRT correlator system on the FX chips designed by NRAO has naturally resulted in a close interaction between us and the VLBA Correlator Group. We have been seriously studying the design of FFT and multiplier boards by the NRAO engineers for the VLBA correlator. In the true spirit of co-operation prevailing among the international astronomical community, the VLBA correlator group has been providing us with all the necessary information in this regard.

While we now find it appropriate to re-design all the boards for our correlator system to optimise our requirement, a large part of the NRAO design is still relevant for our FFT and multiplier cards. In the first phase, we have ordered a few PCBs identical to those being used in VLBA for their FFT and MAC boards. These will be used for initial experience as well as to provide the first correlator when the antennas begin to be operational. The modifications required for our purpose will be summarised below.

In the FFT cards, we want to provide for 4-bit samples instead of the 2-bit samples provided in the VLBA system. Further, our maximum FFT size is 512-points instead of 2048 points. Since we can accomplish this bypassing an FFT-stage in each of the 4 FFT engines in a card, we are able to save 4 FX chips per card (total of 120 chips in our system) by suitably modifying the board.

The MAC cards of the VLBA have been designed to enable every pair

pectra to be sent to two distinct ASICs simultaneously, which is
ntial for getting full polarization information. However, this
irement clashes with our desire to utilise RR,LL mode of the ASIC
louble the correlator bandwidth, since this requires only one ASIC
receive a given pair of signals. Thus, we will need some intelligent
tching of data entering the FFT engines as well as a modification
the VLBA multiplier card for our requirement. The modification
MAC card essentially consists of eliminating one matrix containing
ASICs and retain only a maximum 16 ASICs per card instead of the 32
n the VLBA card. The total number of MAC cards required for GMRT
ill be 64 to support full 32 MHz bandwidth. If we allow two different
ard types rather than one, we can manage with 60 cards instead of 64.

PLAN OF ACTION

We have planned to execute the development of the correlator system in
4 phases: (a) Test Fixture, (b) Limited system for 2-6 antennas
(c) Prototype system for 2 antennas; and (d) Final system.
In the first two phases, VLBA boards will be used without modification
for FFT and MAC units, but the control cards will have more limited
capability compared to the VLBA system.

A brief summary of these phases is given below.

(a) Test Fixture: The Test fixture consists of 5 parts - input preparation,
FFT, MAC and a control card. The input preparation will be based on two
6-bit sampler evaluation board based on AD9000 whose output will be
given to two FFT engines for a period of 128 ms. The output of FFT engines
is simultaneously fed to the MAC board, all ASICs in the board receiving
essentially the same signals. At the end of 128 ms, the data from the
MAC are read out into a computer. All the 32 ASICs in the multiplier
cards are then expected to give identical answers. By inputing known
signals from a signal generator into the sampler, we can know beforehand
the results to be expected. These can be preloaded into a buffer in the
Test Fixture in order to compare them with those read out from the MAC
card and thus validate each ASIC in either FFT or MAC functionality.

After the initial completion, some improvisations will be made to the
test fixture and some experiments will be performed to assess the effects
of quantisation especially with regard to understanding the influence
of CW interference on the FX correlator. In addition, attempt will be
made to infer the cross-coupling by measuring the correlation coefficient
of two noise sources in order to work out a goot strategy for proper
isolation and shielding requirements.

The delay card, the updated control cards will all be first used in
the test fixture so that the final test fixture should not be much
different from a 2-station interferometer to be used in the field.

(b) Field trials with the first antennas: For this purpose, a system
for 2-aerial interferometry will first be released based mainly on the
test fixture. Improvisation of buffer-recirculation-card and control
and data acquisition will take place in parallel so that a workable
correlator system for 4-6 antennas is available by early 1992.

It should be recalled that the system available during this phase will
depend upon the VLBA cards for FFT and MAC without modifications, altho
the sampler and delay line will actually correspond to 4-bit
implementations. The upgradation from 2-stations to 6 stations will be
and the data acquisition scheme may be a shortgap arrangement.
data rates are moderate and a simple serial interface
with the test fixture may be acceptable.)
heavily with the earlier

phases. Since there are 10 different types of cards, we expect various prototypes to be ready gradually during the next two years with mass-production efforts beginning sometime during 1992. The component procurement process has already begun for the FFT, MAC and control cards. All critical components for the remaining systems will also be identified within the next month or two so that all the required components are available in our stores by the time we begin the mass-production. We aim at testing final prototype versions in the field at least for 2 antennas (and perhaps for 4 antennas) before mass production is initiated.

(d) The Final System: The major mass-production items are the Sampler, Delay, FFT and MAC cards. There will be 30 cards in each of the first three types and 64 (60?) MAC cards. The FFT card is expected to be a 8-10 layer PCB while the MAC card might be a 6-8 layer PCB. These may be fabricated abroad. The sampler cards will be 4-layer PCBs which will be fabricated indigenously.