90107

GMRT CORRELATOR SYSTEM OVERVIEW

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The GMRT Correlator System consists of 4 subsystems: Sampler+Delay Subsystem; F-subsystem, X-subsystem, Long-Term Accumulator. The F- and X- subsystems have a strong resemblance to the VLBA Correlator system. In the following, the specifications of these 4 subsystems are outlined along with the constraints in terms of providing connection to other digital systems or to provide synchronization necessitated by astronomical requirements. In particular, the entire system is fully pipelined and capable of handling a continuous stream of input data for at least several seconds without any break in the astronomical data. The continuity of data stream is required primarily by machines operating in non-interferometric mode, e.g., for pulsar observations or VLBI observations where the entire array is presented as though it were a single antenna. The following specifications are a result of discussions we have had in the past couple of years on the scope and limitations of GMRT. They are only presented as an outline rather than going into a detailed justification, nor is any attempt made to be accurate in the engineering details of implementation (which is beyond me anyway!)

1. Sampler and Delay Subsystem

Before the sampler, the signals are assumed to have undergone several operations: (a) optional Noise-signal injection at the station to help gain calibration, (b) optional phase-switching based on Walsh functions injected at remote stations which are expected to be synchronously demodulated AFTER SAMPLING (synchronisation to an accuracy of about half a millisecond or so is expected between the switching time and demodulation), (c) Fringe-tracking at the local oscillator (which needs to synchronize its phase jumps with delay step), (d) Doppler-tracking, etc., etc.

General specifications:

Number of stations	32
No. of IFs/station	4
maximum IF-bandwidth per FFT-engine	16 MHz

(Note: The 4 channels are primarily intended for providing 32 Ms/s bandwidth for pulsar search machine; however, a special mode has been incorporated into the ASIC by NRAO with which we may be able to handle a total IF bandwidth of 32 Ms/s without increasing number of multiplier chips but sacrificing polarization information.)

Sampler:

Sampling frequency	32 Ms/s
Number of bits	4 bits (16 levels)
Thresholds	uniform, symmetric about mean
Level-step	0.3352 x rms
Number of samplers	32 x 4 = 128
output format	4-bit, sign-magnitude format

(Note: Coding of output to sign-magnitude form may be in this stage or after the delays, as convenient to the engineers; however, engineers to specify the coding of digitized signals available to pulsar-timing machine)

Delay Line:

Delay step	4 ns (accuracy = 2 ns)
Maximum delay	256 microsec

Minimum integration time	4 ms
Maximum integration time	100 ms (normal and default)
Number of multipliers	528 (32 x 33 - two per baseline)
Number of channels	528 x 256 = 207336 = 264 kw (complex)
Number of spectral channels	256 (RR,LL only) per baseline 128 (RR,RL,LR,LL) per baseline
Output representation	IEEE floating point (2 x 32 bit normalised floating point converted from the original 15,15,6 complex)
Output interface standard	serial, SCSI (???)
Synchronization and Pauses	The output sampling (100 ms pulse) is used in several places for synchronization -- e.g., start of Walsh-function sequency phase-switching, delay-step and the associated phase jump in the Local Oscillator, and so on. The above synchronisation aspect should be kept in mind if pauses are introduced at the end of each 100 ms-cycle. As a matter of fact, it is not some absolute 100 ms-periodicity that is relevant, but the end of a fixed number of FFT cycles (approximating 100 ms) which is important for synchronisation. An interrupt should be generated at the beginning of each FFT-cycle FOLLOWING the accumulator cycle, and it is this interrupt which is used for synchronization

(Note: The X-subsystem will generate a constant data rate irrespective of the details of number of channels or sub-arrays or polarization mode etc. In the case of sub-array implementation, irrelevant channels may be masked by the long-term accumulator at the software level.)

There is a special mode in the ASIC (also in the VLBA board?) which enables us to implement RR,LL for 128 spectral channels using only one chip per baseline. With this, it should be possible to realise RR,LL for 256 spectral channels for a total of 32 MHz bandwidth (2 x 32 Ms/s) since provision has been made for the FFT engines to handle this bandwidth - there are 4 FFT engines per station. Another option worth implementing is 1024-point FFT (512 spectral channels) by reducing the number of antennas -- this requires feedback from the engineers.

4. LONG TERM ACCUMULATOR

The details of long term accumulator are still not finalised. At present, two models exist - a dedicated hardware circuitry using fast adders working on IEEE floating point representation - which will integrate to the specified duration. The second model is based on a multi-microprocessor system (e.g. 16 transputer-based processing elements) on a VME bus, and the various options of adding provided in the software residing on the processing elements). Presumably, each of these processing elements has a SCSI port from which to accept the short-term integrated values in IEEE floating point representation (or perhaps 15,15,6 itself??), and they all send their results to the data acquisition system which is on the same VME bus. The current thinking is in terms of a dedicated hardware using fast adders. It is planned to re-assess the scope and need for flexibility of long term accumulator at a later date and, depending on the availability of manpower, we may also pursue the model using a multi-microprocessor system.

Input data rate	264 x 1024 complex words every 100 ms (18.88 MB/s if 15,15,6 is accepted; or 21.12 MB/s if IEEE format is accepted)
Integration Time	2.5, 5, 10 sec
Output data rate	0.8, 0.4, 0.2 MB/s depending on integration-time
Output interface	VME bus

The reason for investigating a general purpose multi-microprocessor system for long-term integration is to provide versatility, e.g., providing options of averaging over spectral band in addition to time, sub-array recognition, evaluate statistics to help on-line flagging of data.

The on-line computer will have the following specifications:

cpu	SPARC
memory	16 MB
bus	VME
peripherals	Exabyte (8mm video cartridge) - - 1 controller with 2 drives Disk - nominal (about 300 MB or diskless)
network	Ethernet - tcp/ip, nfs
O/S	Vx-Works -- multitasking real-time o/s
Development	on Sun 3 or SPARC sytem

Software -- VxWorks from Wind River Systems and Debugger from SUN -- is expected to be available by the end of 1990, and the hardware (SPARC cpu card from Sun or Myzar is expected to be available in 1991. A development system based on Tadpole 68030+68882 board (manufactured by Godrej) will be available during late 1990 - a VxWorks target in a VME card cage and with built in ethernet, SCSI and serial controllers.