Noise Source

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A 15 MHz white Gaussian noise source was designed and fabricated. Thermal noise in the resistors is the fundamental source. The noise source is useful for testing communication links. With a fast Analogue to Digital Converter (ADC) it can be used as an hardware random number generator. This is useful in digital simulation work where it is time consuming to generate Gaussian distributed random numbers using software methods.

Operating Principle

All references to components are with respect to the circuit diagram in Appendix-1.

Thermal noise is white Gaussian. Noise voltage in the resistors R_1 & R_2 is amplified to the desired level by amplifier chain comprising IC_1, IC_2, IC_3 & IC_4. IC_1 to IC_3 are differential video amplifiers (LM 733). They have a bandwidth of 120 MHz. Differential configuration is used throughout to reduce external 'noise' and interference. Differential configuration also reduces coupling problems. Total required gain is distributed throughout the stages for optimum bandwidth and stability. The final stage (IC_4) is primarily used to convert the balanced input to single ended low impedance output.

Automatic Level Control (ALC) is incorporated for stability. The Field Effect Transistor (FET) acts as a voltage controlled resistor. The FET is a BEL BFW 10. The effective reistance between pins 12 & 7 of IC_2 determines the gain of that stage and thus the overall gain. The ALC control voltage can also be given from outside the board permiting the extension of the ALC loop to include the final element (for example ADC).

All precautions required for high frequency circuits are taken. PCB layout is compact, ordered and symmetrical. Ground and power supply lines are properly laid. Power supplies to the IC's are decoupled. Voltage regulators are on the outside of the enclosure. Feedthrough capacitors are used at the powersupply entry points.

Enhanments

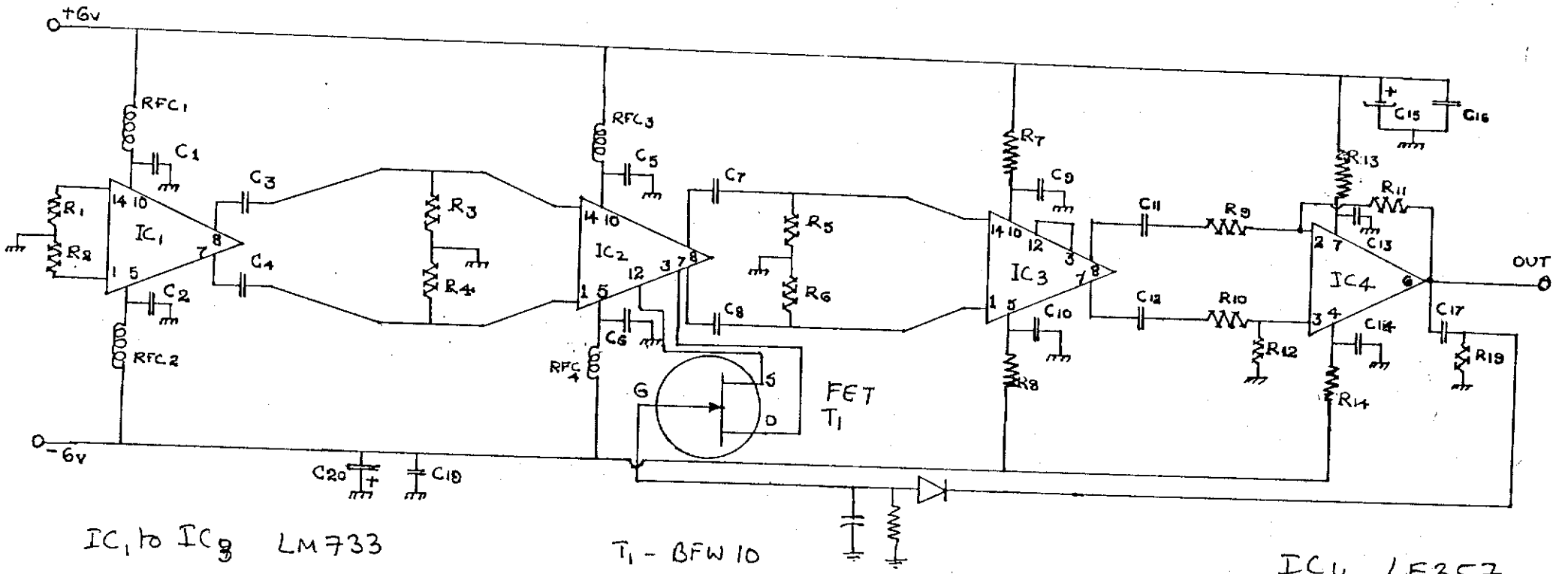
1. The final output voltage can be compared with a precision voltage reference and the error voltage can be used to control the FET . This would provide greater amplitude stability.
2. A wideband Operational Amplifier can be used in the final stage to provide grater bandwidth.

Conclusion

The noise source has been used with the flash ADC card and the PC Interface. The Probability Distribution Function (PDF) has been determined and when averaged is found to closely approach the Gaussian function.

Appendices

1. Circuit Diagram
2. PCB Layout
3. Brief Data on LM 733.
4. Brief Data on LF 357.



IC_1 to IC_3 LM733

T_1 - BFW 10

IC_4 LF357

C_1 to C_{14} 0.1μF CER.

C_{17} 0.2μF Poly.

R_1 to ALL RESISTORS 10KΩ **EXCEPT**:

R_7, R_8, R_{13}, R_{14} 150 Ω

R_{19} - 120KΩ

R_1, R_2 - 47Ω

C_{15}, C_{20} - 6μ8 12V tant

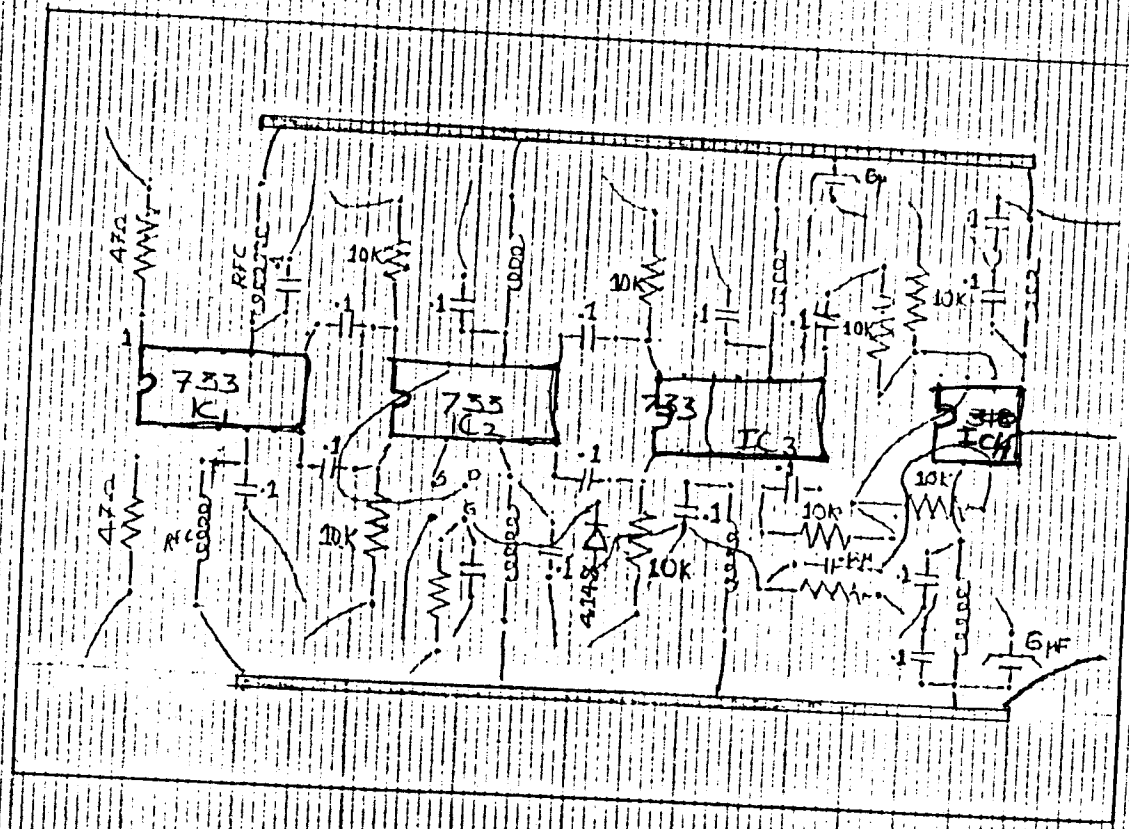
C_{19}, C_{16} - 0.1 cer disk

APPENDIX - 1

CIRCUIT DIAGRAM NOISE SOURCE

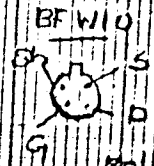
NOISE GEN.

24081987



AYP035

FET = BF W10



PC Layout Noise Source.

APPENDIX 2 Layou

μA733

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

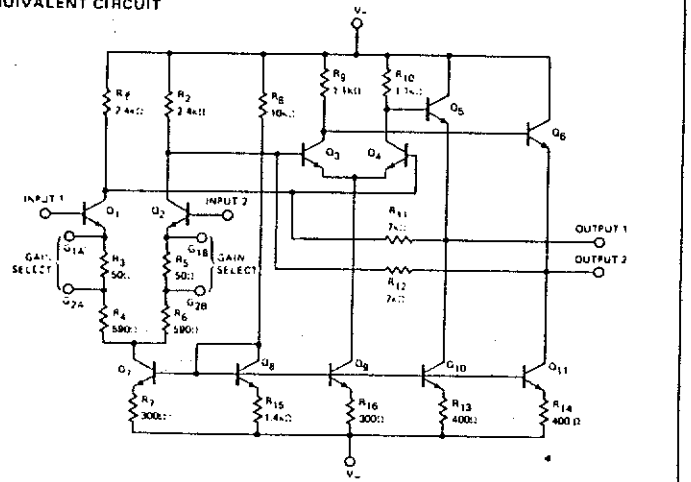
GENERAL DESCRIPTION – The μA733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar™ epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- 120 MHz BANDWIDTH
- 250 kΩ INPUT RESISTANCE
- SELECTABLE GAINS OF 10, 100, AND 400
- NO FREQUENCY COMPENSATION REQUIRED

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range	
Military (μA733)	−55°C to +125°C
Commercial (μA733C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

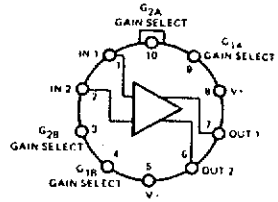
CONNECTION DIAGRAMS

10-LEAD METAL CAN

(TOP VIEW)

PACKAGE OUTLINE 5N

PACKAGE CODE H



Note: Pin 5 connected to case

ORDER INFORMATION

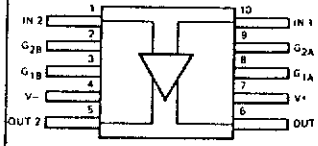
TYPE	PART NO.
μA733	μA733HM
μA733C	μA733HC

10-LEAD FLATPAK

(TOP VIEW)

PACKAGE OUTLINE 3F

PACKAGE CODE F



ORDER INFORMATION

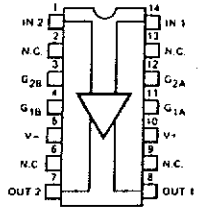
TYPE	PART NO.
μA733	μA733FM

14-LEAD DIP

(TOP VIEW)

PACKAGE OUTLINE 6A

PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA733	μA733DM
μA733C	μA733DC

μA733

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔVS = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

Siemens

JFET Input Operational Amplifiers

These operational amplifiers have JFET input transistors and feature very low input and offset currents. The output is designed for high capacitive load without any stability problems.

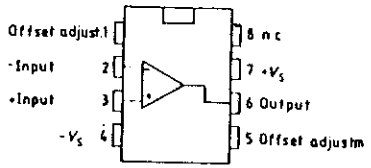
Additional features:

- Extremely high input resistance
- Slight drifting at temperature changes
- Wide bandwidth
- High input voltage up to $+V_S$ permitted
- Internal frequency compensation

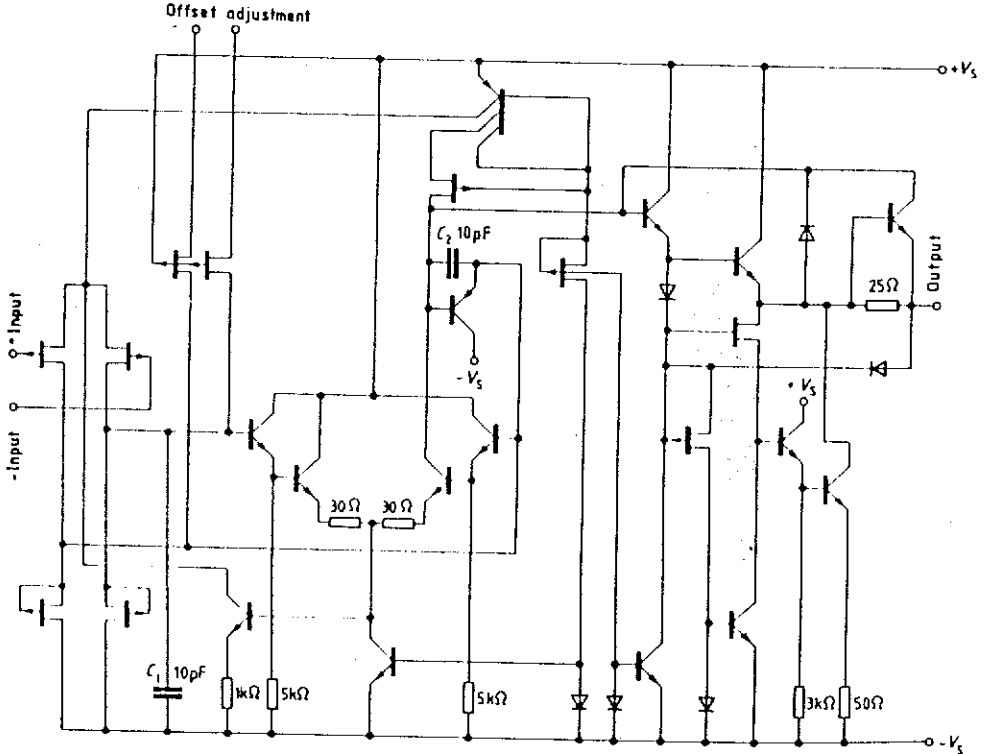
Maximum ratings

Supply voltage	V_S	± 18	V
Differential input voltage	V_{ID}	± 30	V
Output short-circuit duration	t_{OSC}	∞	
Storage temperature range	T_s	−55 to 125	°C
Junction temperature	T_j	100	°C
Thermal resistance system — ambient air	R_{thsamb}	175	K/W

Pin configuration



Circuit diagram



Siemens

Characteristics

V_S = ±15 V, T_{amb} = 25 °C

			min	typ	max	
Open loop supply current	LF 355 N	I_S		2	4	mA
	LF 356 N, LF 357 N	I_S		5	10	mA
Input offset voltage	(R_G = 50 Ω)	V_{IO}		3	10	mV
Input offset current		I_{IO}		3	50	pA
Input current		I_I		30	200	pA
Input resistance		R_I		10^{12}		Ω
Open loop voltage gain		A_{VO}		80	106	dB
Rate of rise	LF 355 N: A_V = 1	$\frac{dvq}{dtr}$		5		V/µs
	LF 356 N: A_V = 1			12		V/µs
	LF 357 N: A_V = 5			50		V/µs
Performance bandwidth	LF 355 N	f_p		2.5		MHz
	LF 356 N	f_p		5		MHz
	LF 357 N	f_p		20		MHz
Transient time (for 0.01%)	LF 355 N	t_r		4		µs
	LF 356 N, LF 357 N	t_r		1.5		µs
Input noise voltage R_S=100Ω;f=100 Hz:	LF 355 N	V_{IN}		25		nV/√Hz
	LF 356 N, LF 357 N	V_{IN}		15		nV/√Hz
R_S=100Ω,f=1000 Hz:	LF 355 N	V_{IN}		20		nV/√Hz
	LF 356 N, LF 357 N	V_{IN}		12		nV/√Hz
Input noise current f = 100 Hz, or 1000 Hz		I_{IN}		0.01		pA/√Hz
Input capacitance		C_I		3		pF

Characteristics

V_S = ±15 V; T_{amb} = 0 to 70 °C, unless otherwise specified

		min	typ	max	
Input offset voltage R_G = 50 Ω	V_{IO}			14	mV
Temperature coefficient of V_{IO}: R_S = 50 Ω	α_{VIO}		5		µV/K
Change of α_{VIO} after a change of V_{IO} adjustment[1]	$\Delta\alpha_{VIO}$		0.5		per mV
Input offset current T_j = 70 °C	I_{IO}			2	nA
Input current[2] T_j = 70 °C	I_I			8	nA
Open loop voltage gain R_L = 2 kΩ, V_{Opp} = ±10 V	A_{VO}	63			dB
Output voltage R_L = 10 kΩ	V_{Opp}	12	±13	−12	V
R_L = 2 kΩ	V_{Opp}	10	±12	−10	V
Input common mode range	V_{IC}	+11	+12	−11	V
Common mode rejection	k_{CMR}	80	100		dB
Supply voltage rejection	k_{SVR}	80	100		dB

Remarks:

1) Compared to the originally non adjusted value, the temperature coefficient of the adjusted input offset voltage changes only slightly (typ. 0.5 µV/K) for every mV of the setting range. Adjusting the offset voltage has no effect on the common-mode rejection and open-loop voltage gain.
2) The input currents

Appendix 4