HIGH VOLTAGE VARIABLE POWER SUPPLY

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Introduction

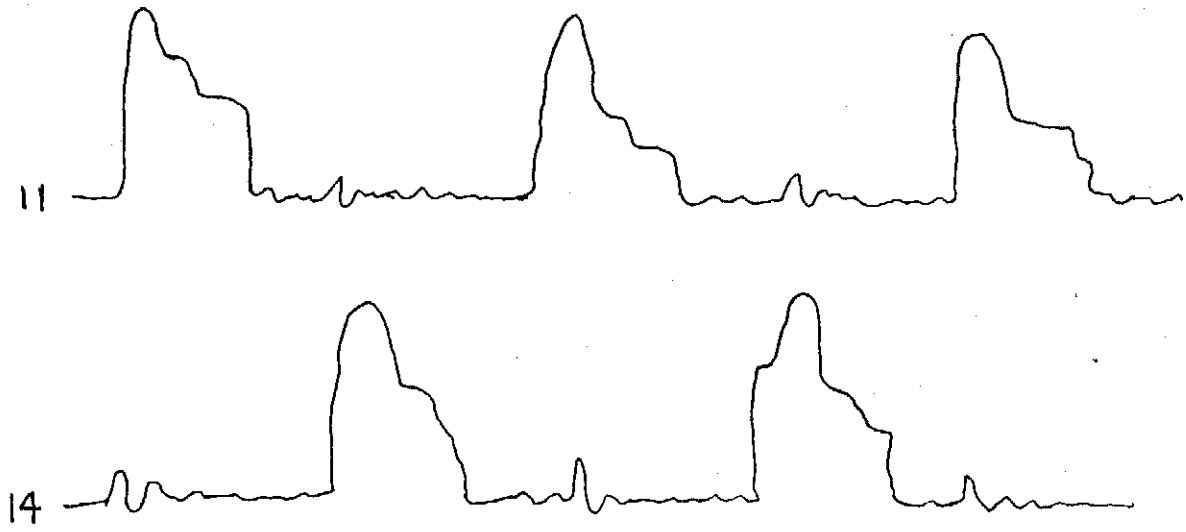
A high voltage variable power supply was developed for fibre optic receivers using APD (Avalanche Photo Diode) detectors. The voltage range is variable from 90 V to 350V to take care of both Silicon and Germanium APD's. A primary source of 12 V DC is used. The power supply will also be useful for genarating narrow pulses using the second breakdown effect in bipolar transistors. To reduce power dissipation over the wide output voltage range required SMPS techniques are used. A locally avaliable controller SG 3524 is used.

Operating Principle

All references to the components are with respect to the circuit diagram in Appendix-1.

R_3 & C_1 determine the frequency of the 3524 controller.(100Khz for the values shown).The final switching elements operate at half this frequency. C_3 & D_1 provide soft start.Complementary PWM outputs are avaliable at pins 11 & 14 , for driving the MOSFETS directly.There is a dead time when both the transistors are off.This provides protection against accidently turning both the transistors on. R_5 & R_6 turn off the MOSFETS in

the absence of drive. D_2, D_3, & D_4 provide flyback protection for the MOSFETS. On the secondary side a bridge configuration is chosen to simplify the transformer winding. Rectifier losses are small as the output voltage is large compared to the diode drops. L_1 C_6 form a resonant filter at the switching frequency. R_7, R_8 & R_9 form a voltage divider for feedback to the error amplifier. R_4 & C_2 provide loop compensation . The transformer is wound on a CEL ferrite toroid (T-27) HP3C material (H=3900A/m). Teflon tape is used for insulation. Turn ratio is 6 + 6 : 375 . The diodes are fast recovery type. Typical waveforms at the gates of the MOSFETS are shown below.



Performance

Input voltage	:	12 V DC
Output voltage	:	70 to 500 V DC Adjustable.
Ripple @ 300V	:	200 mV peak to peak (0.06 %.)
Efficiency @ 300V	:	50 %

Ripple can be reduced by using filter capacitor with low ESR (Efective Series Resistance) or by paralleling capacitors. ESR of the capacitor used now is high. Efficiency is poor due to

(i) High step up ratio and the resulting large winding capacitances.

(ii) Slow recovery of the diodes (T = 300 ns max) compared to the MOSFETS (T = 100ns).

Enhancements

(1) Fast rectifiers (T $\lesssim$ 80 ns) should be used for good efficiency. The operating frequency can be increased to 100Khz.

(2) At low powers BJT's can be used to reduce ~~the~~ cost.

(3) Improved SMPS controllers can be used.

(4) An Opto-Coupler can be incorporated in the feedback path to provide greater Isolation between the primary and secondary sides.

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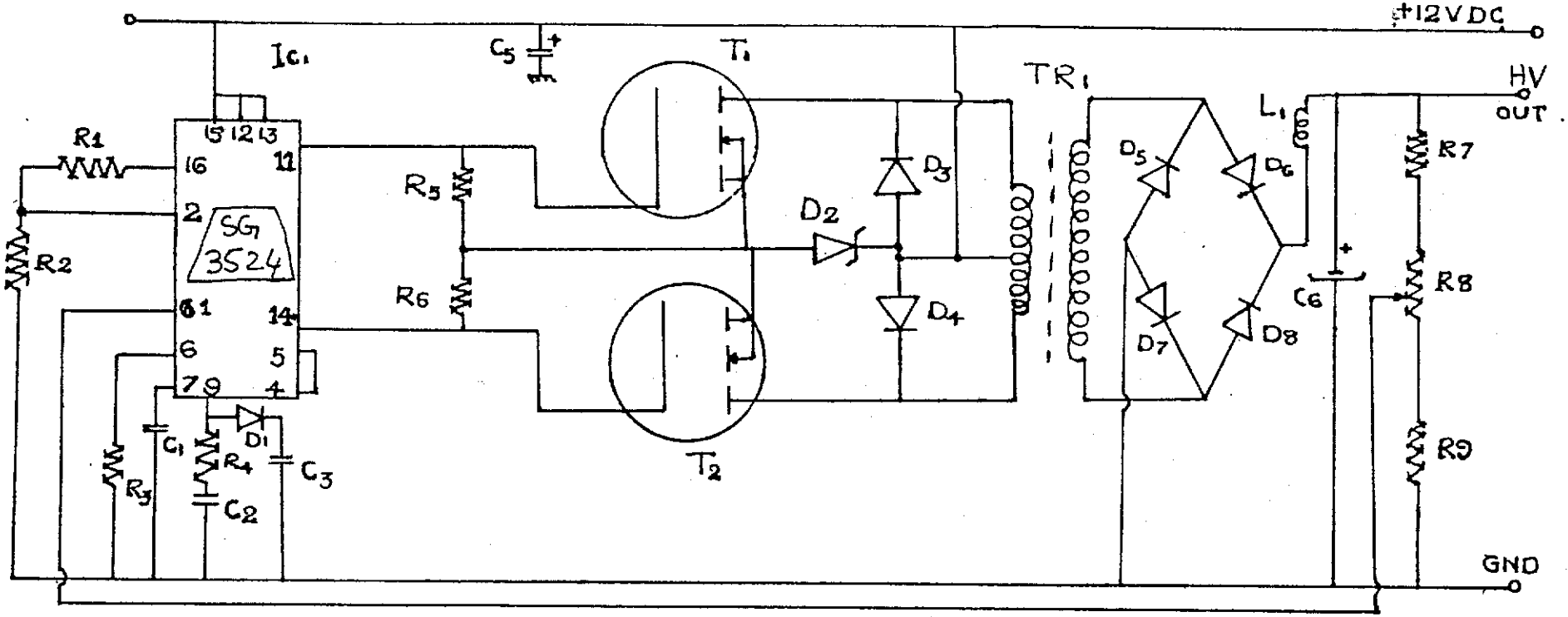
Appendix 1 : Circuit Diagram.

Appendix 2 : Brief Data on SG 3524

Appendix 3 : Brief Data on MOSFETS (BUZ 53)

Appendix 4 : PCB layout of the power supply



R_1, R_2, R_3 10KΩ

C_1 - 20Kpf
C_2 - 1nS
C_3 - 5mfd.

R_5, R_6 220Ω

C5 470uF 16V

T_1, T_2 BUZ 53
D_2 33V ZENER
D_3, D_4 PFR 811

D_5, D_6 } PFR 817
D_7 D_8 }

TR1: 6+6 : 375 T-27

C_6 100μF 500V

R_7 2 MΩ
R_8 50K preset
R_9 10KΩ

DESCRIPTION

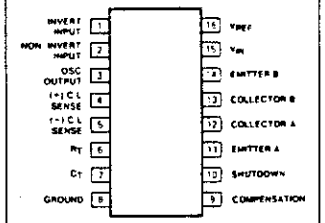
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D,F,N PACKAGE

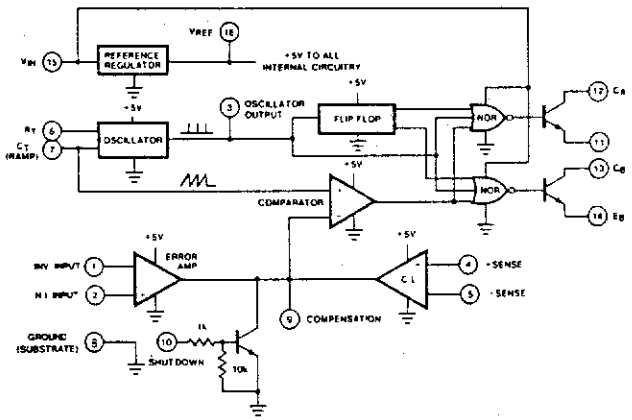


ORDER PART NUMBERS
SG3524F, SG3524D,
SG3524N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{ON} = 20V, and f = 20kHz unless otherwise specifi

PARAMETER	TEST CONDITIONS	SG3524		
		Min	Typ	Max
Reference Section				
Output voltage		4.6	5.0	5.4
Line regulation	V_{IN} = 8 to 40V		10	30
Load regulation	I_L = 0 to 20mA		20	50
Ripple rejection	f = 120Hz, T_A = 25°C		66	
Short circuit current limit	V_{REF} = 0, T_A = 25°C		100	
Temperature stability	Over operating temperature range		0.3	1
Long term stability	T_A = 25°C		20	
Oscillator Section				
Maximum frequency	C_T = .001 mfd, R_T = 2kΩ		300	
Initial accuracy	R_T and C_T constant		5	
Voltage stability	V_{IN} = 8 to 40V, T_A = 25°C			1
Temperature stability	Over operating temperature range			2
Output amplitude	Pin 3, T_A = 25°C		3.5	
Output pulse width	C_T = .01 mfd, T_A = 25°C		0.5	
Error Amplifier Section				
Input offset voltage	V_{CM} = 2.5V		2	10
Input bias current	V_{CM} = 2.5V		2	10
Open loop voltage gain		66	80	
Common mode voltage	T_A = 25°C	1.8		3.4
Common mode rejection ratio	T_A = 25°C		70	
Small signal bandwidth	A_V = 0dB, T_A = 25°C		3	
Output voltage	T_A = 25°C	0.5		3.8
Comparator Section				
Duty cycle	% each output "ON"	0		45
Input threshold	Zero duty cycle		1	
Input threshold	Maximum duty cycle		3.5	
Input bias current			1	
Current Limiting Section				
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, T_A = 25°C	180	200	220
Sense voltage T.C.			0.2	
Common mode voltage		−1		+1
Output Section (each output)				
Collector-emitter voltage (breakdown)		40		
Collector-leakage current	V_{CE} = 40V		0.1	50
Saturation voltage	I_C = 50mA		1	2
Emitter output voltage	V_{IN} = 20V	17	18	
Rise time	R_C = 2kΩ, T_A = 25°C		0.2	
Fall time	R_C = 2kΩ, T_A = 25°C		0.1	
Total standby current (excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10

APPENDIX 2

APPENDIX 2
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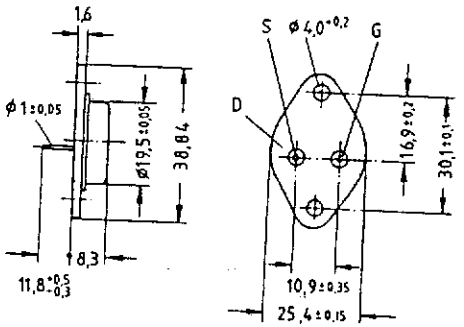
Drain-source voltage	V_{DS}	= 1000 V
Continuous drain current	I_D	= 2,6 A
Drain-source on-resistance	$R_{DS(on)}$	= 5,0 Ω

Description SIPMOS power FET, N-channel enhancement mode

Case Metal case 3A2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 53 A	C67078-A1009-A3



Dimensions in mm

Absolute maximum ratings

Drain-source voltage	V_{DS}	1000V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	1000V
Continuous drain current, T_{case} = 25 °C	I_D	2,6A
Pulsed drain current, T_{case} = 25 °C	I_{Dpuls}	10A
Gate-source voltage	V_{GS}	±20V
Max. power dissipation	P_D	78W
Operating and storage temperature range	T_j T_{stg}	−55 °C ... + 150 °C
Isolation test voltage (t = 1 min)	V_{is}	–
DIN humidity category		C

Thermal resistance

$R_{th\ JA}$	≤35K/W
$R_{th\ JC}$	≤1,6K/W

MOSFET BUZ53

Electrical characteristics

at T_{case} = 25 °C (unless otherwise specified)

Static ratings

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 1mA
Gate threshold voltage	$V_{GS\ (th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 10mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\ (on)}$	–	4,5	5,0	Ω	V_{GS} = 10V I_D = 1,5A

Dynamic ratings

Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120		
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} (t_{on} = $t_{d\ (on)}$ + t_r)	$t_{d\ (on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} (t_{off} = $t_{d\ (off)}$ + t_f)	$t_{d\ (off)}$	–	110	140		
	t_f	–	60	80		

Reverse diode

Continuous reverse drain current	I_{DR}	–	–	2,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs
Reverse recovery charge	Q_{rr}	–	15	–	µC	

APPENDIX 2

APPENDIX 3

BUZ53

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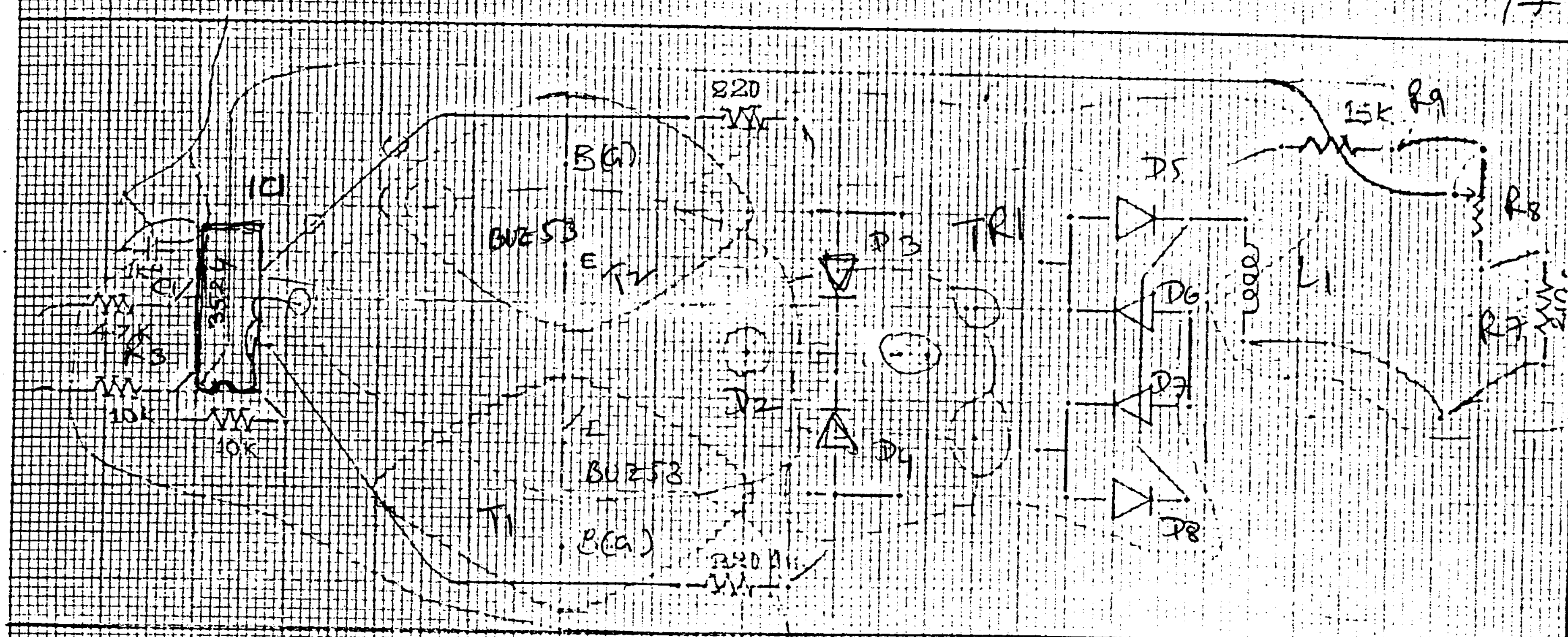
300v. SWITCHING REGULATOR



APPENDIX 6

APPENDIX 6

Layout