Project Report

On

UHF FRACTIONAL-N
FREQUENCY SYNTHESIZER

By
Ms. Ashwini Beke
(Exam. No. B013032)
Ms. Girija Deo
(Exam. No. B013039)

Year : 1998 - 99

Department of Electronics and Telecommunication
Engineering.
Government College of Engineering
Pune – 411005

This is to certify that **Ms. Ashwini Beke** and **Ms. Girija Deo**
have completed their project entitled

' UHF Fractional-N Frequency Synthesizer '

to our satisfaction and submitted the same during the academic year
1998 – 99
towards the partial fulfilment of the degree

BACHELOR OF ENGINEERING
In
ELECTRONICS AND TELECOMMUNICATION ENGINEERING
of the University of Pune.

Prof. (Mrs.) C. V. Joshi
Project Guide

Dr. (Mrs.) K. S. Jog
Head of the Department

**Department of Elecectronics and Telecommunication
Engineering
Government College of Engineering
Pune – 411005**

The project entitled ' **UHF Fractional-N Frequency Synthesizer** ' was carried out successfully by **Ms. Ashwini Beke** and **Ms. Girija Deo** during the academic year 1998-99, under the guidance of

Mr. A. Praveen Kumar
(Scientific Officer, S.E.)
National Centre for Radio Astrophysics (NCRA)
Tata Institute of Fundamental Research (TIFR)
Pune-411007

K.J.

Dr. (Mrs.) K. S. Jog
Head of the Department
Department of E & TC Engineering
Government College of Engineering
Pune – 411005

ACKNOWLEDGEMENTS

special thanks to Shri. J. K. Solanki for his help in sorting out various administrative formalities.

Finally, we wish to thank all the staff members of NCRA, Pune and GMRT project site, Khodad, for making our stay in this place a memorable one.

Ashwini Beke

Girija Deo

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1 OVERVIEW

Frequency synthesizer is a system that generates any one of equally spaced frequencies within a given band referenced to a stable frequency. The aim of the project is to develop a prototype frequency synthesizer for the frequency range of 200 to 400 MHz for possible use in the Receiver System of the Giant Meterwave Radio Telescope (GMRT).

GMRT is a very sensitive aperture synthesis radio telescope with 30 paraboloidal dish antennas of 45m diameter each, set up at about 80 km North of Pune City as a National facility for frontline research in Radio astronomy and Astrophysics. Twelve antennas form a random array in a central 1 km × 1 km area and the remaining 18 are equally distributed along the 3 arms of an approximate 'Y' configuration, resulting in a maximum baseline separation of about 25 km. GMRT has been designed to operate at 6 frequency bands at 50 MHz, 150 MHz, 233 MHz, 327 MHz, 610 MHz, 1000 MHz to 1500 MHz.

The signals from celestial sources are amplified in Low Noise Amplifiers and mixed with Local Oscillator (LO) to an IF of 70 MHz. These 70 MHz IF signals from different antennas are brought to central location (Central Electronics Building – CEB) and after Base Band conversion are sampled and correlated. Since the RF frequency range is from 38 MHz to 1420 MHz and the IF frequency is at 70 MHz, Local Oscillator frequency required at each of the antennas is in the range of 100 MHz to 1500 MHz.

One of the major blocks in the GMRT Local Oscillator system is the 'Frequency Synthesizer'. Synthesizers are required at each of the antenna shells for the generation of Local Oscillators. The frequency synthesizers to cover the above range of 100 MHz to 1500 MHz are realized using a set of Voltage Controlled Oscillators (VCO), a YIG (Yttrium Iron Garnet) Tuned Oscillator (YTO), each of them working within a Phase-Locked Loop (PLL), as per the following scheme.

LO RANGE	TUNNABLE OSCILLATOR	STEP-SIZE
100-200 MHz	VCO1	1 MHz
201-354 MHz	VCO2	1 MHz
355-600 MHz	VCO3	5 MHz
500-1500 MHz	YTO	5 MHz

A 5 MHz oven controlled crystal oscillator is used as the basic reference for GMRT time and frequency standard. All the other frequencies generated in the entire system are phase locked to this basic reference.

1.2 SCOPE OF THE THESIS

The scope of this project is to design and optimally realize a Frequency Synthesizer covering a frequency range of 200 MHz to 400 MHz (VCO2 and associated PLL) using new generation PLL ICs and VCOs, which are now available. The power dissipation of these new ICs is low compared to older versions. This project was assigned to us so that, if successfully completed, it could be used in the future system upgrades. Though the synthesizer was designed for 200-400 MHz, it can be modified to cover any of the frequency ranges upto 1600 MHz using appropriate VCOs and YTOs. The synthesizer uses a frequency reference of 105 MHz, which is generated at each of the antenna shells in a separate reference generation system. The reference for this frequency is derived from the basic GMRT time and frequency standard.

1.3 ORGANIZATION OF THESIS

Chapter 2 introduces the reader to the basic working principle of PLL system, VCOs, different Frequency Synthesis Techniques, Phase noise concepts. Chapter 3 covers system specifications, schematic of proposed system and design of PLL synthesizer subsystem. Chapter 4 includes Loop Filter and VCO subsystem design. Interface control drawing and material list are covered in chapter 5. The thesis ends with conclusion, list of references used and appendixes covering manuals of various ICs used in the system.
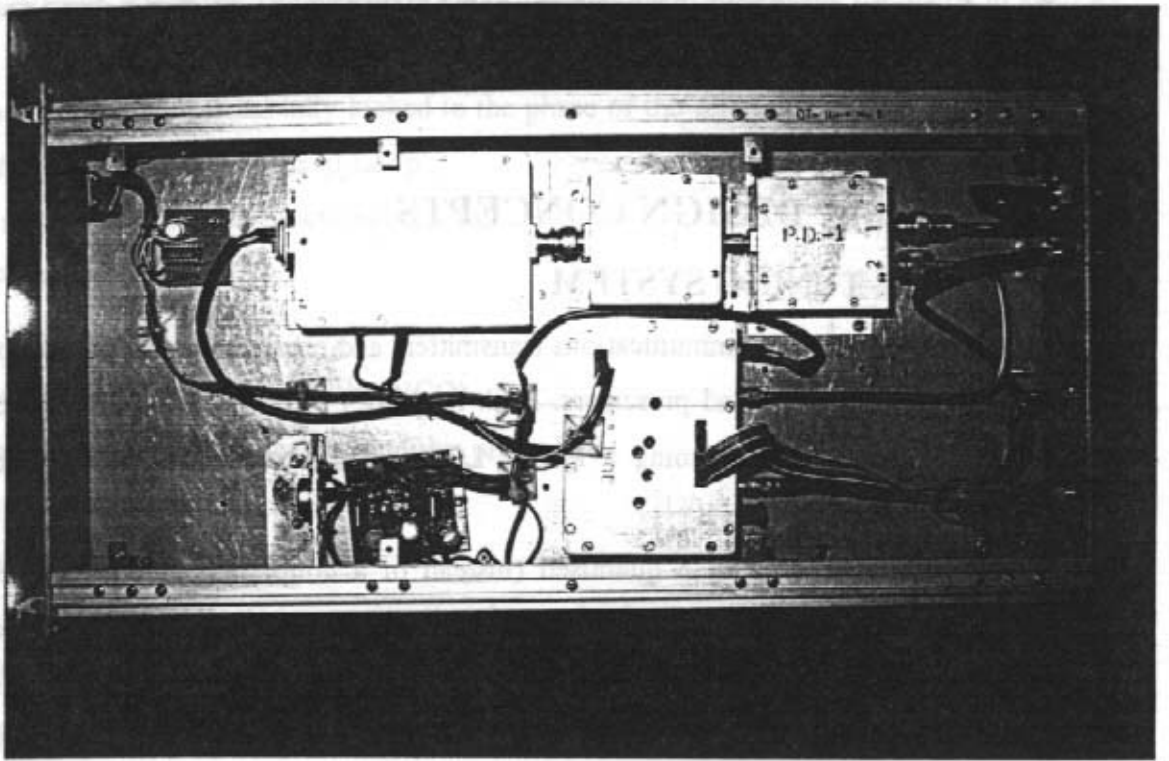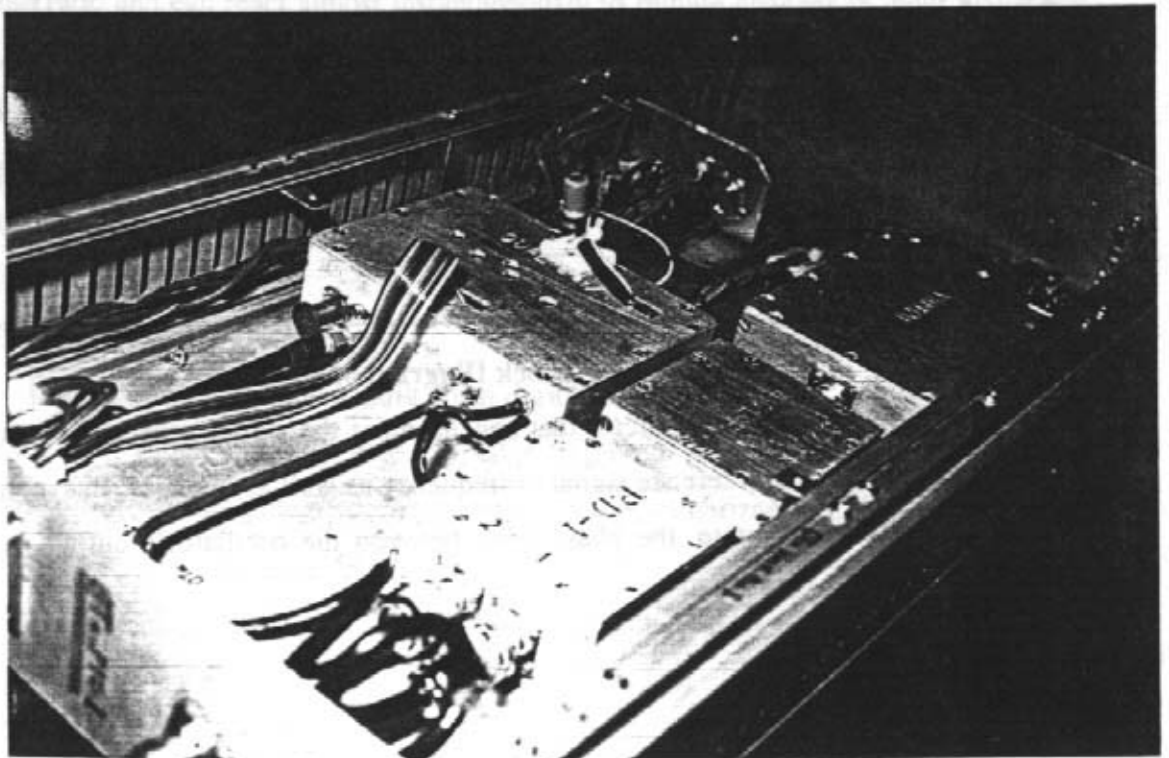
2. SYNTHESIZER SYSTEM CONCEPTS

2.1 BASIC DESIGN CONCEPTS

2.1.1 PLL TUNING SYSTEM

Tuning of telecommunications transmitters and receivers is the largest application area for today's PLLs and prescalers. High frequency PLLs have largely replaced older methods such as direct tuning a RC or LC oscillator to the desired local oscillator frequency.

At the expense of a quantised (instead of a continuous frequency) resolution, PLLs provide a cheaper, faster, more compact and reliable solution to tuning circuitry. The fact that PLLs allow selection of frequencies in discrete steps, rather than over a continuous range, is not a big limitation for use in present day communication system.

PLL :

The schematic for Phase Locked Loop is as illustrated in Fig. 2.1
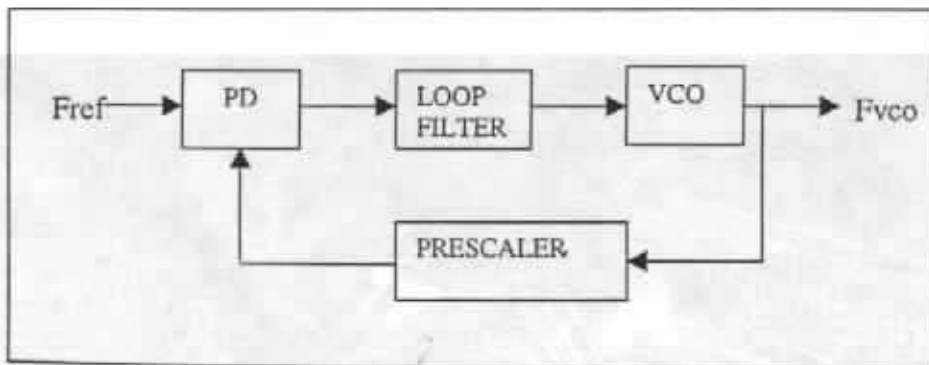
Fig. 2.1 Block Diagram of PLL

A PLL is a feedback circuit that synchronizes the signal generated by a tunable oscillator with a stable reference signal in frequency as well as in phase. In synchronized, often called 'Locked' state, the phase error between the oscillator's output signal and reference signal is very small.

• If the phase error builds up, a control mechanism acts on the oscillator in such a way that phase error is again reduced to a minimum. In such a control system, the phase of the output signal is actually locked to the phase of the reference signal. That is why it is referred to as 'Phase-Locked Loop'.

It consists of three basic functional blocks:

• Phase Detector (PD)

• Loop Filter

• Voltage Controlled Oscillator (VCO)

and as necessary, single or dual modulus prescalers.

Phase Detector :

The phase detector compares the phase of reference signal with that of the phase of VCO output signal. The output of Phase Detector is a measure of phase difference between its two inputs. There are two types of phase detectors:
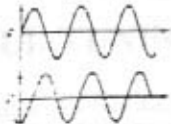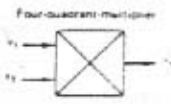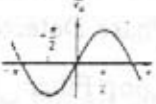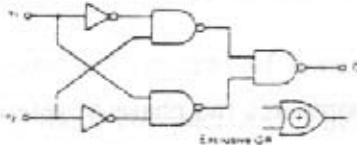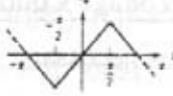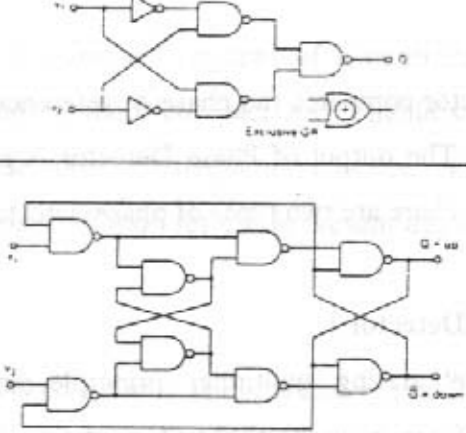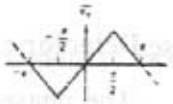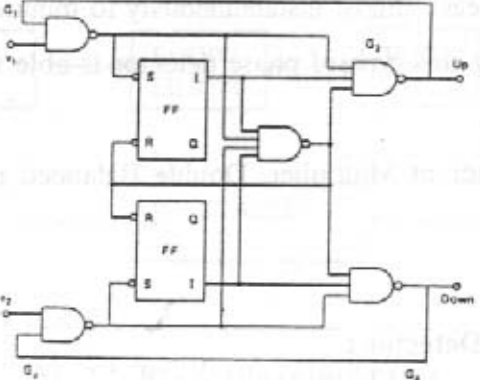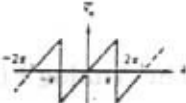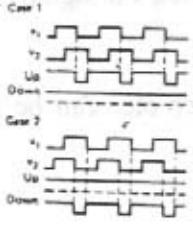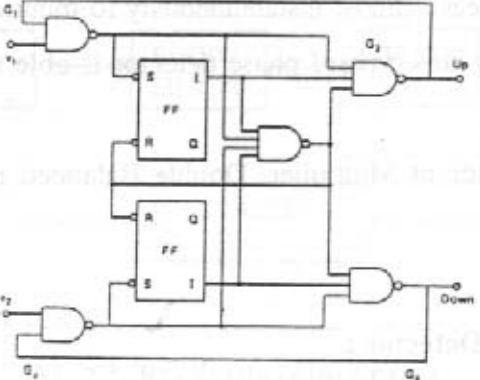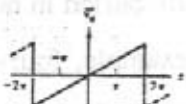
• The Analog Phase Detector :

It works on integrating multiplier principle and reflects not only timing differences, but also differences in the shape of input signals. It can offer superior signal-to-noise ratio and can react almost instantaneously to minute changes in input waveform. A PLL system utilizing this type of phase detector is able to lock on signals, which are heavily buried in noise.

For example, four-Quadrant Multiplier, Double Balanced mixer etc. can be used as an analog phase detector.

• The Digital Phase Detector :

Digital phase detector is built from digital components such as logic gates, flip-flops to form either EX-OR gate, an edge-triggered JK master/slave flip-flop etc. Comparison of various phase/frequency detectors is summarized in Table 2.1 and Table 2.2.

Input signals	Circuit	$V_{out} = f(\theta)$
	Four-quadrant-multiplier	
Square wave		
	Exclusive OR	
	JK master/slave FF	
Case 1 / Case 2		

*Courtesy of Fachschriftenverlag, Aargauer Tagblatt AG, Aarau, Switzerland.

Table 2.1 Circuit Diagrams and Input-Output waveforms of various
Phase/Frequency Comparators

TYPE	OPERATING RANGE	SENSITIVITY
4 Quadrant Multiplier	$-\pi$ to π	Phase only
EX-OR gate	$-\pi$ to π	Phase only
Edge Triggered JK f/f	-2π to 2π	Phase frequency; insensitive for small errors
Tri-state Phase/ Frequency Comparator	-2π to 2π	Phase frequency

Table 2.2 Comparison of various phase/frequency detectors.

EX-OR based phase detector is generally used in the applications where the waveforms are symmetrical. For asymmetrical waveforms the phase detector gain is reduced resulting in lower hold and lock ranges. Phase detectors using edge triggered JK flip-flops show frequency sensitive performance for large frequency offsets only, whereas tri-state phase/ frequency comparator is frequency sensitive for any value of frequency offset. In this type of comparator, (shown in Fig. 2.2), the UP and DOWN output signals are active LOW. Performance of tri-state phase/frequency comparator is illustrated in Fig. 2.2. In case of zero phase error (not shown in Fig. 2.2) both UP and DOWN output signals are permanently HIGH. If the VCO output signal U2(t) lags the reference signal U1(t), the UP output generates pulses with the duty cycle ratio proportional to phase error. The DOWN signal is then inactive and vice-versa.

This type of comparator has several advantages:

- It has the best possible locking performance and best frequency and phase difference detection.
- Regardless of the amount of frequency error, the average output voltage is always above or below half the operating voltage. This results in good locking performance.

Loop Filter :

The output of phase/frequency comparator is passed through loop filter, which pulls the VCO in lock. Loop filter is generally a low pass filter, which determines the noise characteristics of VCO. The loop filter integrates the output signal from phase/ frequency detector into a DC voltage to drive the VCO to a specific frequency.
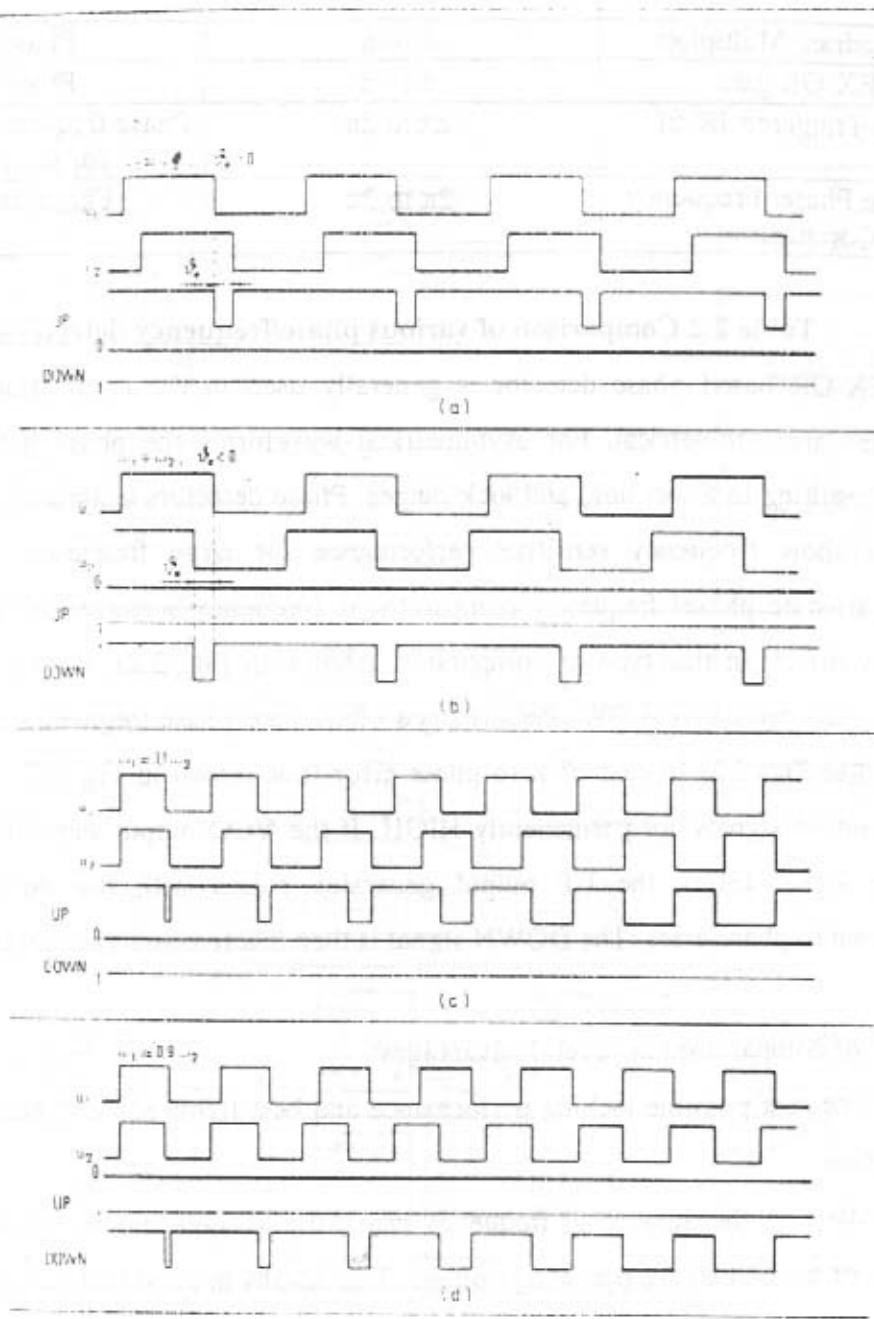
(Courtesy of Dr. Ronald E. Best, Phase-Locked Loops. Theory, Design and Applications)

Fig. 2.2 Waveforms of Phase/Frequency comparator

Loop Filter functions :

- It smoothes the Phase Detector output.
- It determines the dynamic performance of the loop.

The dynamic performance includes capture and lock ranges, the noise suppression bandwidth and the transient response.

Effect of LPF on:

Capture range: If beat frequency (the difference between the VCO output frequency and reference frequency) is too high to pass through the LPF, the PLL will not respond. Then the signal is said to be out of capture range. As the filter bandwidth is increased, capture range increases. Thus, capture range is controlled by LPF.

Noise suppression: The charge on the filter capacitor gives a short time memory to PLL. Thus even if the signal becomes less than the noise for few cycles, DC voltage on capacitor continues to shift VCO till it picks up the signal again. This produces high noise immunity and locking stability.

Faster lock-up times require wider Low Pass filters, while better noise characteristics are achieved with narrow filters.

Lag/lead filter is generally preferred as it has two independent time constants. Hence natural frequency and damping can be chosen independently. Also DC gain can be made as large as may be necessary for good tracking.

VCO :

In Voltage Controlled Oscillator, output frequency can be changed by applying a voltage to its control port or tuning port. The tuning voltage to frequency conversion of VCO, implements integration with respect to phase.

∴ Order of PLL = Order of Loop Filter + 1

Types of VCOs :

- Crystal oscillator (VCXO)
- Resonator (LC, coaxial or cavity) oscillator
- RC multivibrator
- YIG-tuned oscillator

8

Varactor tuned oscillator (VTO) :

Varactor tuned oscillator, has varactor diode as the basic component. The resonator of a VCO is LC circuit with a 'varactor' as a voltage controlled variable capacitance. Varactor is a diode operated in reverse biased condition providing a junction capacitance, that is a function of applied reverse bias voltage. The applied reverse bias produces a wide depletion region. Since the depletion region acts as a dielectric between two conducting plates, the device has the characteristics of a capacitor. The depletion region capacitance is proportional to the area and inversely proportional to the width of the depletion region. Thus the depletion region width is inversely proportional to the reverse bias voltage.

$$C(v) = \frac{C(0)}{V^n}$$

Where n (constant) depends on doping intensity.

Types of varactors :

In linearly graded junction, for a given voltage change, the change in the capacitance is smaller as compared to that of an abrupt junction. Since, in most cases, maximum capacitance change is required; the linearly graded junction is not used as a tuning diode. Hence most preferred types of varactor diodes are:

- Abrupt junction varactor :

    It gives a non-linear tuning. It has high Q value and gives the best noise performance.

- Hyper abrupt junction varactor:

    The hyper abrupt junction varactor provides a greater capacitance change than the abrupt junction diode for a given voltage change. Hence for this diode, lower tuning voltage range is required for given frequency range. Therefore, for wide band VCOs these varactors are preferred. Fig. 2.3 shows the tuning sensitivity Vs frequency characteristics of abrupt and hyper abrupt junction varactors.

Fig 2.3 Tuning sensitivity Vs Frequency characteristic for varactors

For a varactor diode, capacitance is related to bias voltage by following equation:

$$C(V) = \frac{C(0)}{(V + \Phi)^n}$$

Where, C (0) is capacitance of the diode with zero bias.

Φ is built-in potential, which is 0.7 V for silicon diode and 1.2 V for GaAs diode. Higher Q can be obtained from GaAs devices due to its lower resitivity. But it is more expensive due to higher material and processing costs.

An abrupt junction varactor has a constant value of $n = 0.5$. Hence, it has a smooth curve of 'temperature coefficient of capacitance' (Tcc) Vs 'reverse voltage' as shown in Fig. 2.4.

Fig. 2.4 Tcc Vs Tuning Voltage characteristic of abrupt junction varactor.

10

However, in case of hyper abrupt junction varactor, 'n' is a function of voltage, and the shape of Tcc curve depends on the details of n (V) curve shown in Fig. 2.5

(Courtesy of Application note 80500, Tuning Diode)

Fig. 2.5. Tcc Vs Tuning Voltage characteristic of hyper abrupt junction varactor

Hyper abrupt junction varactor has linear frequency versus voltage characteristics. For this diode, lower Q value must be settled than an abrupt junction varactor with same breakdown voltage and same capacitance. Hence the noise will be higher as compared to abrupt junction varactor diode.

Fundamental Oscillator Circuits :

Fig. 2.6

11

Fig 2.3 Tuning sensitivity Vs Frequency characteristic for varactors

For a varactor diode, capacitance is related to bias voltage by following equation:

$$C(V) = \frac{C(0)}{(V + \Phi)^n}$$

Where, C (0) is capacitance of the diode with zero bias.

ϕ is built-in potential, which is 0.7 V for silicon diode and 1.2 V for GaAs diode. Higher Q can be obtained from GaAs devices due to its lower resitivity. But it is more expensive due to higher material and processing costs.

An abrupt junction varactor has a constant value of n = 0.5. Hence, it has a smooth curve of 'temperature coefficient of capacitance' (Tcc) Vs 'reverse voltage' as shown in Fig. 2.4.

Fig. 2.4 Tcc Vs Tuning Voltage characteristic of abrupt junction varactor.

10

However, in case of hyper abrupt junction varactor, 'n' is a function of voltage, and the shape of Tcc curve depends on the details of n (V) curve shown in Fig. 2.5

(Courtesy of Application note 80500, Tuning Diode)

Fig. 2.5. Tcc Vs Tuning Voltage characteristic of hyper abrupt junction varactor

Hyper abrupt junction varactor has linear frequency versus voltage characteristics. For this diode, lower Q value must be settled than an abrupt junction varactor with same breakdown voltage and same capacitance. Hence the noise will be higher as compared to abrupt junction varactor diode.

Fundamental Oscillator Circuits :

Fig. 2.6

11

• The schematic illustrated in Fig. 2.6 is a simple design with minimum number of components. When a Si bipolar transistor is used, the phase noise will be very low and the maximum frequency will be typically 9 GHz. The oscillator will have a wide tuning range and a high tuning speed.
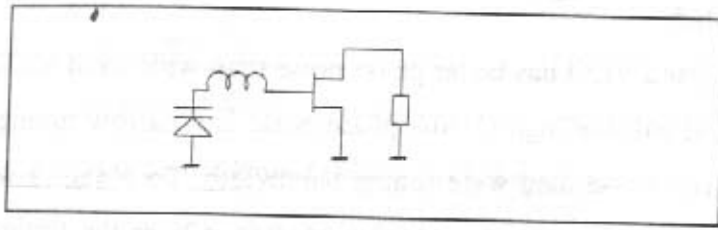
Fig. 2.7

GaAs FET transistor configuration shown in Fig. 2.7 has the maximum frequency more than 26 GHz. The phase noise will be 10 to 20 dB higher than for oscillators with Si transistors.
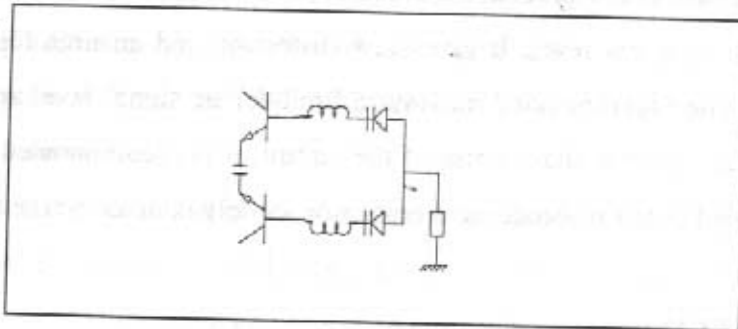
Fig. 2.8

The advantage of above configuration shown in fig 2.8 is that the excellent phase noise characteristics of the Si transistor oscillator can be achieved at frequencies up to 18GHz. A number of harmonics will be generated and will have to be considered when using the oscillator in a system.

High frequency VCO designs demand high 'ft' transistors, high Q varactors. The varactor Q falls rapidly at lower tuning voltages, therefore it is seen that for improperly chosen varactor, the oscillations stop at low tuning voltages when varactor Q is too low.

VCO phase noise depends on the resonant Q of the oscillator. Higher the Q, better is the phase noise performance. But resonators with high Q tune over narrow frequency ranges.

Advantages of wide band VCOs are:

- They provide fast tuning.
- When frequency pulling is significant enough to shift the VCO outside of its frequency range, wide band VCO can more easily accommodate the correction to the frequency shift.

Narrow band VCO has better phase noise than wide band VCO. Hence the design of the VCO must balance high Q, low phase noise and narrow tuning bandwidth against low Q, high phase noise, and wide tuning bandwidth. To obtain a wide bandwidth, the varactor diode must offer a wide capacitance change over the tuning voltage range. In many applications, the tuning voltage range is severely restricted, and therefore the varactor is required to offer a high capacitance ratio over a small voltage change. On the other hand, the varactor Q is usually compromised by a high capacitance ratio.

The most important precaution in the oscillator design is to maintain the ac signal across the diode to a low level. It gives low distortion and ensures reproducible tuning characteristics. The recommended maximum limit for ac signal level across the diode is 300 mV. To minimize the phase noise of the circuit, it is recommended that the varactor be loosely coupled to the resonator and resonator loosely coupled to the transistor.

Limitations of VCO :

- VCOs show significant degradation of noise due to non-linear reactance controlled unit, varactor.
- Commercially available VCOs are generally one octave or less in the frequency range.

To overcome these limitations, YIG-tuned oscillators are used.

YIG- Tuned Oscillator (YTO) :

YIG tuned oscillator is a current controlled device. YIG i.e. Yttrium Iron Garnet ($Y_3Fe_5O_{12}$) oscillators have wide tuning range and Linear tuning characteristics. The high Q of YIG resonator offers 20 dB better phase noise performance than the general VCOs. But YIGs are not available at low frequencies (frequencies below 500 MHz).
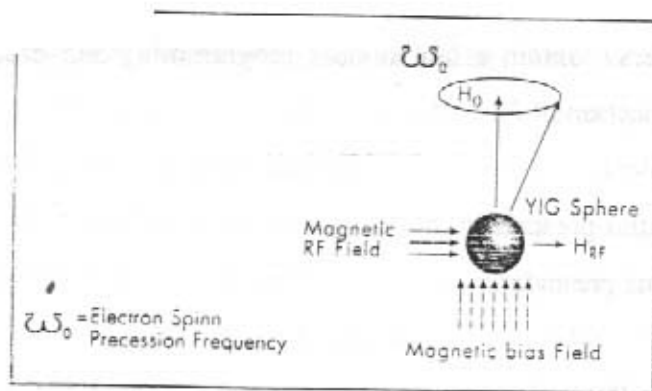
Fig. 2.9 Yttrium Iron Garnet.

The resonant element of YIG oscillator, as illustrated in Fig. 2.9, is formed by suspending small sphere of Yttrium Iron Garnet within resonant cavity and then applying magnetic field to it. Oscillator frequency can be changed by varying magnetic field.

YIG technology offers upto three octaves of tuning. The frequency range may be limited, in the high end, by saturation of the magnetic structure and in the low end by a physical frequency limit of the YIG crystal (500 MHz) and generally by the semiconductor properties.

YIG-tuned microwave oscillators exhibit an almost constant phase noise spectrum over an octave frequency band. Lowest noise is achieved below 20 GHz and may be further improved at lower frequencies and in narrow band designs.

Prescaler :

A prescaler is an integrated circuit that divides the frequency of an incoming signal by an integer P. The divisor 'P' is called the modulus.

A prescaler is a specialized ripple counter, which counts incoming pulses and performs one output cycle for every 'P' received input cycles. If 'P' is an even number the output is toggled following every 'P/2' input pulses. For 'P' odd, one of the toggles is delayed an extra input cycle (e.g., for P = 11, output high for 6 input pulses and low for 5 input pulses.)

There are distinct differences between prescalers and general-purpose divide by N counters. Prescalers are comparatively simple devices. They contain a minimal amount of logic (less than approximately 100 gates) and offer a few modulus numbers.

Program counters, contain a fair amount programming and decoding logic in order to allow a wide selection of N.

Types of prescalers :

- Single modulus prescalers.
- Dual modulus prescalers.

Single Modulus Prescaler :

Single modulus prescalers are fixed or semi-fixed dividers that only divide by a fixed number 'P'. A semi-fixed single modulus prescaler allows a choice of more than one modulus (e.g. 32,64,128), but is not necessarily optimized for switching between moduluses and the modulus choices are not spaced one apart.

Dual Modulus Prescaler :

Dual modulus prescaler allows a very rapid transition from a divide by 'P' mode to a divide by 'P+1' mode (e.g. from 10 to 11). Hence, they are often also called P/P+1 prescalers (10/11). In conjunction with PLLs and the pulse swallow method, dual modulus prescalers allow finer frequency resolution than single modulus prescalers.

Advantages of Prescaler :

- It will totally remove variations in the amplitude noise (amplitude envelope of the incoming signal) since its output amplitude is independent of input.
- It will reduce the phase noise (jitter of zero crossings) of the incoming signal by approximately a factor of 'P' since its output only switches synchronously with one out of every 'P/2' input pulses.

2.1.2 Frequency Synthesis

Frequency synthesis is a combination of system elements that results in the generation of one or many frequencies from one or few reference sources. There are three most common types of frequency synthesizers :

- Digital Synthesizer
- Direct synthesizer
- Phase locked or Indirect synthesizer

In Digital synthesizer, the waveform is synthesized piece by piece. This type of synthesizer can change frequencies very rapidly and fine resolution is relatively easy to attain. But the upper frequency is rather limited.

The Direct synthesizer employs multiplication, mixing, and division to generate desired frequency from a single reference. Like Digital synthesizer they can have very fine resolution. But, the output frequency is a fixed multiple of the reference. This type of synthesizer is very bulky.

Indirect synthesizer, (phase-locked synthesizer) multiplies the reference frequency by a variable number. It does so by dividing its output frequency by that variable and adjusting the output frequency so that, after division, it is equal to the reference frequency. The phase-locked synthesizer can often be made fairly simple and is suitable for miniaturization and for low power operation. It employs 'Pulse Swallow Technique' described in the next section.

Frequency Synthesis using 'Pulse-swallow technique' (Fractional-N Synthesis):
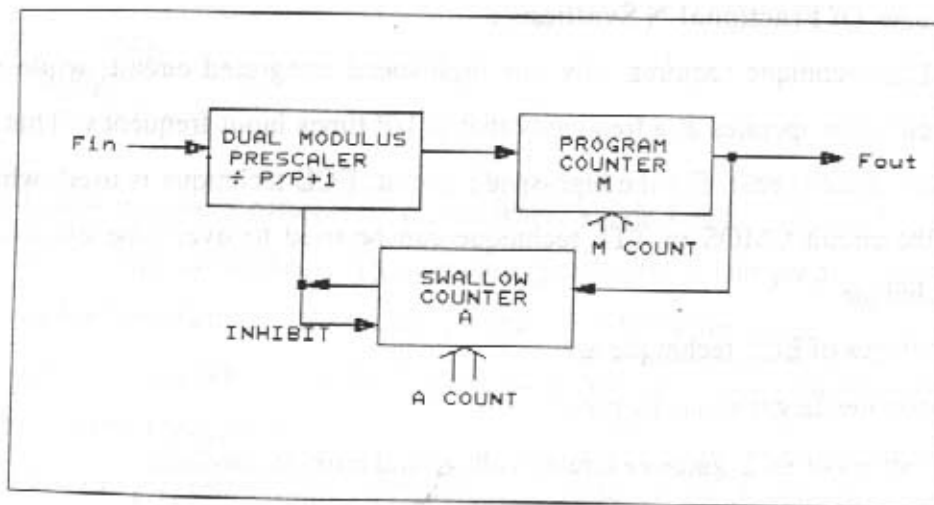
Fig. 2.10 Pulse Swallow Technique

The pulse-swallow technique i.e. 'multi-modulus division' employs two programmable counters (M and A) and a dual modulus prescaler inside the loop as shown in Fig. 2.10. M and A are the counts loaded in program counter and pulse swallow counter, respectively. The counters are preset by externally applied control logic to count from initial state to zero state (down counters). The condition is M must

16

be greater than A. Initially, the dual modulus prescaler is set to divide by 'P+1' (in our case, 11). After 'A' pulses, i.e. when the pulse swallow counter reaches to its zero state, it generates a HIGH modulo control signal. This changes the prescaler division to 'P' (10) and inhibits pulse swallow counter from counting. But, the program counter continues to count to its zero state. Thus after additional 'M-A' pulses, the control signal generated presets both program and pulse swallow counter. The division ratio 'N' is given by:

$$N = (P+1) \bullet A + P \bullet (M-A)$$

$$= A + M \bullet P$$

In other words, $F_{out} = (A + M \bullet P) \bullet F_{ref}$.

Since, P is multiplied by M but not A, the frequency will change by F_{ref} when A is changed by 1. This technique is also called as 'Fractional-N synthesis'. Thus, Fractional-N Synthesis effectively implements a programmable divide-by N counter at the VCO frequency.

Advantages Of Fractional-N Synthesis :

This technique requires only one high-speed integrated circuit, while remaining divider circuitry operates at a frequency that is 1/P times input frequency. This saves DC power and reduces cost. For the high-speed circuit, ECL technique is used, while for the rest of the circuit CMOS or TTL technique can be used to overcome disadvantages of ECL technique.

Disadvantages of ECL technique are:

- It dissipates larger stand-by power.
- High speed of ECL gates generates voltage and current transients.

Advantages of CMOS technique are:

- Almost zero power consumption in the steady state condition
- High noise immunity
- Large range of supply voltages

An important specification of fractional-N synthesizer is that it provides greater side band suppression than a conventional unit, for same filter bandwidth. This allows the use of wider loop filter, which results in a faster channel switching time.

2. 2 Phase Noise Performance of PLL

'Phase noise' is defined as the unwanted frequency or noise energy, which modulates the fundamental output frequency (carrier) thereby determining the overall noise floor characteristic of VCO's output. Phase noise performance is generally considered as 'Figure of merit' in qualifying VCO's spectral purity.

More specifically defined, phase noise is single sideband power level, relative to the level of carrier measured at specified offset frequencies from the carrier, in 1 Hz bandwidth. When the energy of a desired signal appears only at the desired frequency, phase noise is considered perfect and would consist of a single spectral line of infinitesimal width. In practice, the typical noise floor landscape of the VCO's output having a relatively high noise density very close to the carrier and tapering off symmetrically away from the carrier, is observed. Another way of defining the above-mentioned effects is to convert the single sideband power level to an equivalent frequency deviation that would produce the same noise density at the same frequency offset from the carrier. This relationship is determined by the following equation:

$$20\log\left[\frac{2F_{ssb}}{F_{div}}\right] = dBc \tag{2.1}$$

Where, Fssb = frequency offset from carrier where single sideband power level is given.

Fdiv = equivalent frequency deviation (peak) that would produce the same noise level in a1 Hz bandwidth at the same frequency offset from the carrier.

dBc = the level of the dBs below the carrier where the phase noise at given frequency offset is specified.

For example, if the single sideband phase noise is −94 dBc/Hz, then Fdiv is given as:

$$20\log\left[\frac{2.(10kHz)}{F_{div}}\right] = 94dB$$

Thus, Fdiv = 0.4 Hz peak

$$\frac{F_{div}}{\sqrt{2}} = 0.28 Hz(RMS)$$

Therefore a frequency deviation of 0.28 Hz RMS equates to a single sideband phase noise of −94 dBc/Hz at a 10 kHz-offset frequency.

The instantaneous output of an oscillator may be represented by:

$$e\,(t) = [Ec + A(t)]\,\sin[\omega c.t + \theta(t)]$$

(2.2)

Where, Ec and ωc represent the amplitude and the angular frequency of the signal, respectively. A(t) and $\theta(t)$ represent AM noise and FM noise, respectively.

The noise output of PLL is due to noise contribution of the reference source, the phase detector, the loop filter, the VCO and the feedback divider (shown in Fig. 2.11). Within the loop bandwidth, the reference noise is multiplied by the loop division ratio.

2.2.1 Phase-Locked Loop Noise Model
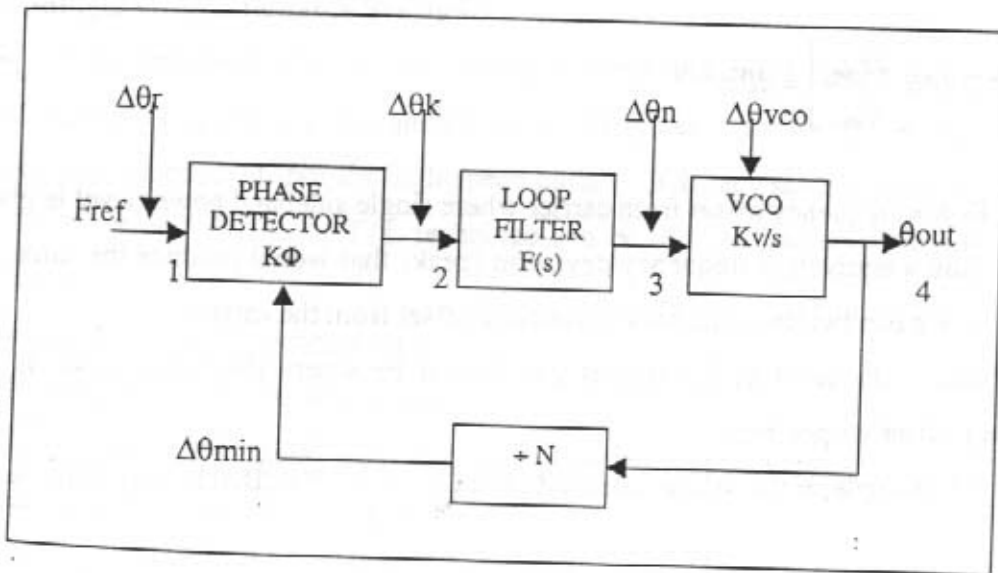
Fig. 2.11 PLL Noise Model.

(Courtesy of VCO manual, Mini-circuits)

The closed loop transfer function of the loop is given by:

$$T(s) = \frac{G(s)}{1 + G(s).H(s)}$$

(2.3)

19

Where, G(s) = forward loop gain

$$= \frac{K_\phi . K_V . F(s)}{s}$$

H(s) = feedback factor,

$$= \frac{1}{N}$$

Thus,

$$T(s) = \frac{N}{1 + \dfrac{s}{K.F(s)}} \tag{2.4}$$

Where,

$$K = \frac{K_V . K_\phi}{N}$$

The reference noise and the divider output noise could be calculated as follows.

The closed loop transfer function relating oscillator phase θout to reference θr is given as:

$$\frac{\theta_{out}(s)}{\theta_r(s)} = \frac{N.K.F(s)}{s + K.F(s)} \tag{2.5}$$

This equation shows that, PLL is effectively low pass filter with respect to noise of reference signal.

The phase noise contributions of reference and divider noise are therefore given by:

$$\Delta\theta_{oiut}^{2} = \left[\frac{N}{1 + \dfrac{s}{K.F(s)}} \right]^2 \left[\Delta\theta_{ref}^{2} + \Delta\theta_{div}^{2} \right] = x^2 \tag{2.6}$$

The loop division ratio must therefore be minimized so as to minimize the divider noise contributions.

The phase detector also contributes to the output noise. In general, any noise input following the phase detector contributes to the output noise.

The transfer function from point 2 to 4 is:

$$\frac{\Delta\theta_{out}(s)}{\Delta\theta_K(s)} = \frac{F(s).\dfrac{K_\Phi}{s}}{1+\dfrac{K_v.K_\Phi.F(s)}{s.N}}$$

(2.7)

$$= \frac{1}{K_\Phi}\frac{N}{1+\dfrac{s}{K.F(s)}}$$

Any noise input following the phase detector is therefore inversely proportional to $K\phi$. The noise contribution is then given by:

$$\Delta\theta_{out}^2 = \frac{1}{K_\phi^2}\left[\frac{N}{1+\dfrac{s}{K.F(s)}}\right]^2 \Delta\theta_K^2 = y^2$$

(2.8)

The phase detector gain constant must therefore be maximized so as to minimize the accompanying noise contributions. Outside the loop bandwidth, the noise will be mainly a function of the VCO.

The transfer function from point 3 to 4 is given by:

$$\frac{\Delta\theta_{out}^2}{\Delta\theta_{vco}} = \frac{1}{1+\dfrac{K.F(s)}{s}}$$

(2.9)

This equation shows that, PLL is effectively high pass filter with respect to noise of VCO. When evaluating the output noise spectrum, we must take into account the VCO noise and its sensitivity.

The following equation gives all the VCO noise contributions:

$$\Delta\theta_{out}^{2} = \left[\frac{s}{s+K.F(s)}\right]^{2}\left[\Delta\theta_{vco}^{2} + \frac{K_{v}^{2}}{s}\Delta\theta_{n}^{2}\right] = z^{2} \tag{2.10}$$

Here, Kv is the VCO gain constant and $\Delta\theta_{n}$ is any noise voltage appearing before the VCO. The overall phase noise of the synthesizer may be given as:

$$\Delta\theta_{out}^{2} = x^{2} + y^{2} + z^{2} \tag{2.11}$$

In conclusion, within the loop bandwidth the reference noise will be multiplied by the loop division ratio. Outside the loop bandwidth, the reference noise will be attenuated by the loop transfer function. Within the loop bandwidth, the VCO noise will be attenuated. Outside the loop bandwidth, the noise will be the same as that of the free running VCO. Near the loop bandwidth, phase noise is not dominated by either the reference or the VCO, but instead it is a function of reference, VCO and phase detector phase noise.

2.2.2 Sources of noise

In a synthesizer, the overall phase noise is determined by the contribution of each and every unit. It includes noise contribution from reference, VCO, phase detector, frequency divider and loop filter.

- The sources of phase noise in semiconductor devices are due to thermal noise, shot noise and flicker or 1/f noise.
- Component limitations such as the finite Q of the tank circuit, leakage effect, etc.
- Externally induced factors such as inadequate ground contacts, microphonic pick-up, or insufficient isolation of power supply and radiating signal sources.

Noise in oscillators :

- Phase noise in oscillators is due to instability. Phase instability results from the inherent phase variations produced by oscillator as a function of time.

- Phase noise from transistor oscillators (bipolar or FET) is due to the Q factor of resonating tank circuit. As Q increases stability increases.

  In general, phase noise generated by VCO is determined by:

- Q factor of resonator
- Q factor of varactor diode.
- The active device used for the oscillating transistor.

Noise in power supply :

Magnetic devices are common sources of interference. Power supplies utilize transformers, which exhibit complex spurious signals

- Primary leads can serve as transmission noise for high frequency energy.
- Magnetic fields associated with transformer iron core can couple to nearby circuits.
- Current associated with core saturation can also cause interference.
- Interruption of current within the magnetic device can result in voltage fluctuations.

    Power supply regulators can be source of low frequency phase noise due to offset and drift. Noise can couple both capacitively and inductively, entering via power leads, control leads or even shielded cables.

Loop filter phase noise :

    The resistor preceding the Op-amp, i.e. R1 determines the input impedance of Op-amp. It means that increase in R1 will increase the noise contribution by the loop filter, if Op-amp noise performance is not that bad.

As the divide fatio N changes from N(min) to N(max), the reference phase noise power is multiplied by 20 logN.

2.2.3 Ways to minimize noise

The following steps are recommended for obtaining the best overall performance.

VCO exhibits high modulation sensitivity, isolation from external circuitry must be added to avoid external coupling. Before isolation can be added, the potential paths of external coupling must be identified.

VCO's DC supply line :

DC noise can modulate the VCO and produce additive phase noise .If the VCO is powered from a regulated power supply, the regulator noise will increase depending upon the external load current drawn from the regulator. The phase noise performance of VCO may degrade depending upon the type of regulator used. To improve the phase noise performance of the VCO under the external load conditions, place a low ESR electrolytic capacitor of about 10µf on the Vcc line as shown in Fig. 2.12.
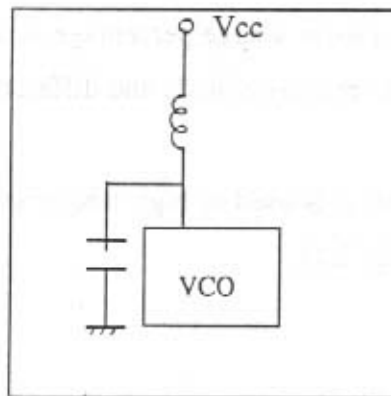
Fig. 2.12 Power Supply De-coupling of VCO.

VCO tuning voltage line :

By filtering this line, the effects of spurious signal coupling can be minimized.

VCO's output port :

By connecting an attenuator at this port, sufficient isolation can be provided to prevent the spurious signals of other circuits from mixing with the VCO's output signal. An attenuator with nominal of 6 to 10 dB should supply adequate isolation.

- Power supply (VCC) and tuning voltage (Vtune) returns must be connected to the printed circuit board ground plane. VCO ground plane must be the same as that of the printed circuit board and therefore all VCO ground pins must be soldered direct to the printed circuit board ground plane.

- Low noise power supplies must be used. Ideally, DC batteries for both supply (VCC) and tuning (V-tune) voltages will provide the best overall performance.

- Output must be correctly terminated with a good load impedance. It is also a good practice to use a resistive pad between the VCO and external load.

- Connections to the tuning port must be as short as possible and must be well screened, shielded and decoupled to prevent the VCO from being modulated by external noise sources.

- Adequate RF grounding is required. Several chip-decoupling capacitors must be provided between the VCC supply and ground. Proper use of grounding and shielding, in combination, can solve a large percentage of all noise problems. Ground loops, which are susceptible to magnetic fields and differences in ground potential are to be avoided.

A multi-point ground system is used at high frequencies to minimize the ground impedance as illustrated in the Fig. 2.13.
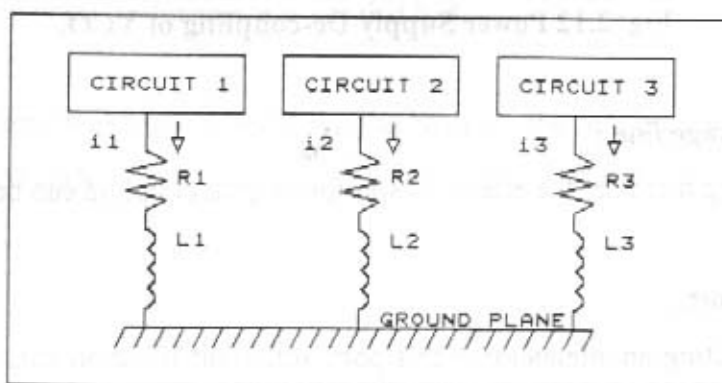
Fig. 2.13 Multi-point Ground.

3. SYSTEM DESCRIPTION

3.1 SYSTEM SPECIFICATIONS :

- Frequency range : 200 MHz to 400 MHz

- Frequency resolution : 1 MHz

- Reference frequency : 105 MHz

- Reference power level : +9 dBm ±0.5 dB

- Power supply : +18V DC (less than 150 mA), -18V DC (less than 100 mA),

  +10V DC (less than 1A)

- Minimum desired phase noise : -80 dBc/Hz @ 10 kHz offset from the carrier

- Synthesized RF output power : -3 dBm ±2 dBm

- Spectral purity :

  (a) Harmonic contents < −30 dBc

  (b) Other spurious products < −40 dBc

- Minimum suppression at an offset of 1MHz (Fpd) from carrier: -60 dBc

3.2 FUNCTIONAL OVERVIEW

The functional block diagram of the system is as illustrated in Fig. 3.1. The technical specifications and functional overview of IC Q3216 are given in appendix A. IC Q3216 is used in Direct Parallel Input mode.

According to the system specifications, the frequency resolution required is 1MHz. The internal reference frequency division chain, in IC Q3216 is not sufficient to divide available reference frequency, Fref (105 MHz), down to phase detector frequency, Fpd (1 MHz), using 6-bit R counter. Hence, external frequency divider is used.

The internal VCO frequency division chain of IC Q3216 is used to divide the VCO output frequency, Fvco (200 MHz - 400 MHz), down to phase detector frequency, Fpd (1MHz). In the prescaler mode, frequency division is accomplished with pulse-swallow technique, described in section 2.1.2. The pulse swallow counter is made up of 10/11 front-end Dual Modulus Prescaler, 4-bit A counter and 7-bit M counter.
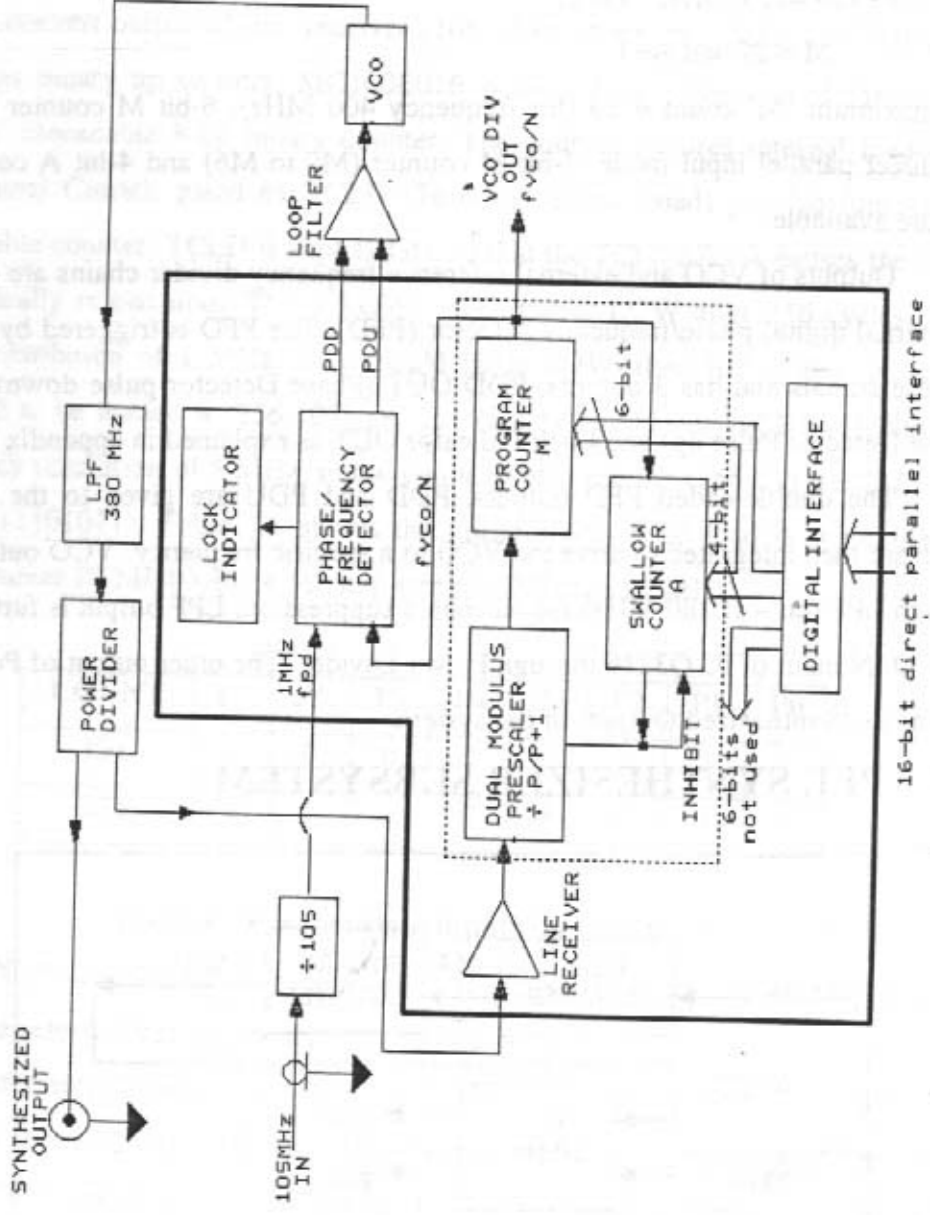
Fig. 3.1 Functional Block Diagram

According to internal circuitry of IC Q3216, the divide ratio is given as :

$N = A+(M+1) \cdot P$ where, P= 10.

In our case, VCO frequency (Fvco) ranges from 200 MHz to 400 MHz and Fpd is 1MHz. $\therefore N = Fvco/Fpd = 200$ to 400

As, $N = 10 \cdot (M+1)+A$

$M = $ integer $(N/10)-1$ and $A = N-10 \cdot (M+1)$

E.g. for Fvco =233 MHz, N = 233

$M = 22$ and A=3

As maximum 'M' count is 39 (for frequency 400 MHz), 6-bit M counter is sufficient. For direct parallel input mode, 7-bit M counter (M0 to M6) and 4-bit A counter (A0 to A6) are available.

Outputs of VCO and external reference frequency divider chains are connected to an internal digital phase/frequency detector (PFD). The PFD is triggered by rising edges of these signals and has 3 outputs, PDD OUT (Phase Detector pulse down), PDU OUT (Phase Detector Pulse up) and Lock Indicator OUT as explained in appendix A.

The double-ended PFD outputs, PDD and PDU are given to the Loop Filter, which are then integrated to drive the VCO to a specific frequency. VCO output is passed through LPF (cut-off 380 MHz) for harmonic suppression. LPF output is further fed back to VCO IN input of IC Q3216 through Power Divider. The other output of Power Divider is taken as 'Synthesized Output' of the system.

3.3   PLL SYNTHESIZER SUBSYSTEM
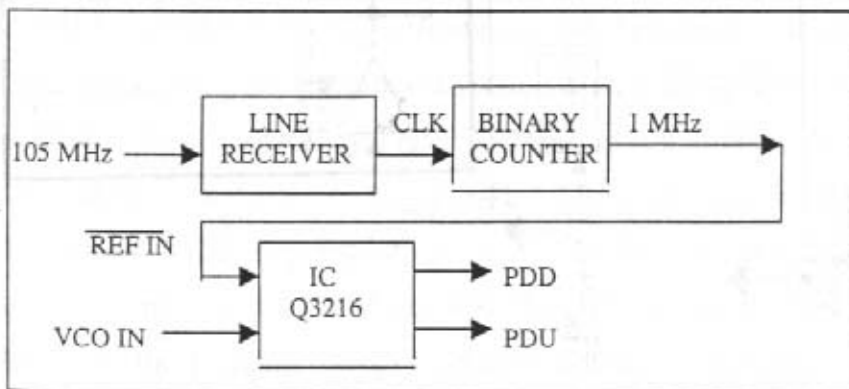
Fig. 3.2 PLL Synthesizer subsystem Block diagram

The block diagram and schematic for PLL Synthesizer Subsystem is as shown in Fig. 3.2 and Fig. 3.3, respectively.

+5 V supply derived from +10 V, is applied to the PLL synthesizer Subsystem. Reference frequency 105 MHz is fed to binary synchronous counter through line receiver IC MC100E116. It has emitter-follower outputs and an internally generated reference supply (Vbb) for single-ended reception. It is used to make input frequency, 105 MHz, ECL compatible with the counter IC MC100E016. It also acts as a buffer.

To convert output of line receiver (105 MHz) down to 1 MHz or 5 MHz, 8-bit synchronous binary up counter, MC100E016 is used. It is a high-speed synchronous, presettable, cascadable 8-bit binary counter. The counter features internal feedback of TC\ (Terminal Count), gated by TCLD (Terminal Count Load) pin. To function as a programmable counter, TCLD is kept HIGH, so that the TC\ feedback causes the counter to automatically reload upon TC\ = LOW. TC\ pulses LOW after 256 cycles. To get frequency resolution of 1 MHz, TC\ should pulse LOW after 105 cycles. Hence, the initial count to be loaded is (256-105) i.e. 151 (binary equivalent 10010111). Similarly, for frequency resolution of 5 MHz, initial count to be loaded is (256-21) i.e. 235 (binary equivalent 11101011). Table 3.1 shows the initial count to be loaded at parallel data inputs of counter IC MC100E016 for step size of 1 MHz and 5 MHz.

COUNT	P7	P6	P5	P4	P3	P2	P1	P0
151	1	0	0	1	0	1	1	1
235	1	1	1	0	1	0	1	1

Table 3.1 Parallel Data inputs for counter IC

The inputs P0, P1 and P7 can be permanently tied to VCC. Inputs P2, P4 and inputs P3, P5, P6 can be selected through switches S1 and S2 respectively.

Counter output frequency, 1 MHz or 5 MHz is given as reference frequency input to IC Q3216 at pin 42 (REF IN). IC Q3216 is configured in Direct Parallel Input Mode with BUSMODE\ input (pin 22) set HIGH and Q3036 MODE\ input(pin 44) set LOW. All the inputs except M7, M8, R4 and R5 are taken directly from external inputs, as listed in the Table 3.2.

30
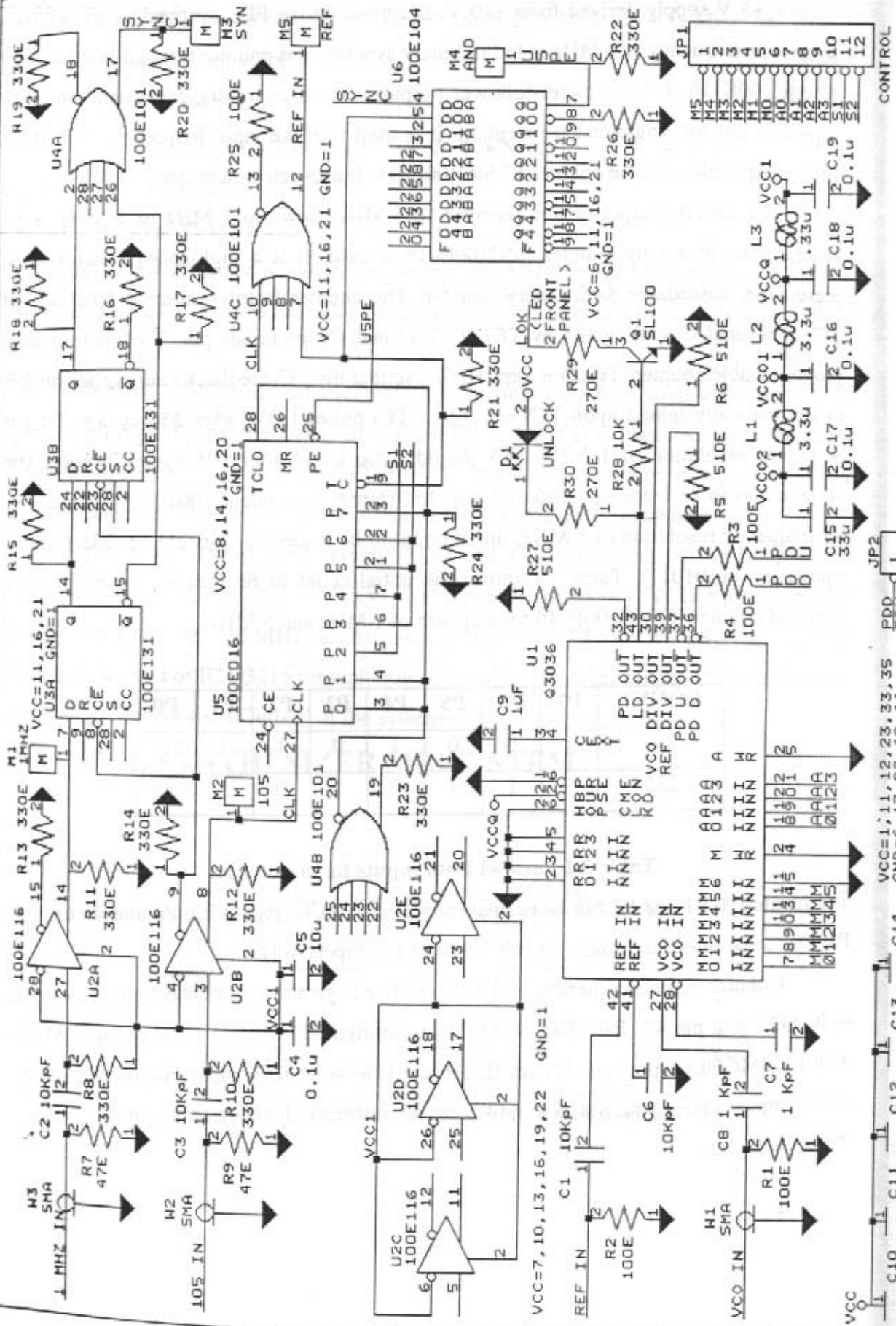
Fig. 3.3 PLL Synthesizer Subsystem

SYMBOL	PINS	I/O TYPE	FUNCTION
M(6-0)	15(MSB),14,13,10,9, 8,7(LSB)	CMOS/TTL INPUT	M-COUNTER BITS
A(3-0)	21(MSB),20,19, 18(LSB)	CMOS/TTL INPUT	A-COUNTER BITS
R(3-0)	5(MSB),4,3,2(LSB)	CMOS/TTL INPUT	R-COUNTER BITS
PRE EN/	16	CMOS/TTL INPUT	PRESCALER ENABLE

Table 3.2 Direct Parallel Mode input functions

Prescaler mode is enabled by setting PRE EN\ (pin 16) LOW. Internal reference frequency division chain is disabled by grounding inputs R0 to R3 (pins 2 to 5) of R counter. Internal VCO frequency division chain is used by programming M0 to M5 (pins 7 to 14) and A0 to A3 (pins 18 to 21) of M and A counters respectively. Input M6 (pin 15) is disabled. Inputs M WR, A WR, HOP WR (PINS 24,25,26 respectively), which are not used in Direct Parallel mode are disabled. Outputs PDD OUT, PDU OUT, REF DIV OUT, VCO DIV OUT, LD OUT (pins 36,37,39,30,43 respectively.) are taken out through JP2 connector.

4. SYSTEM DESIGN

4.1 Loop Filter and VCO Subsystem
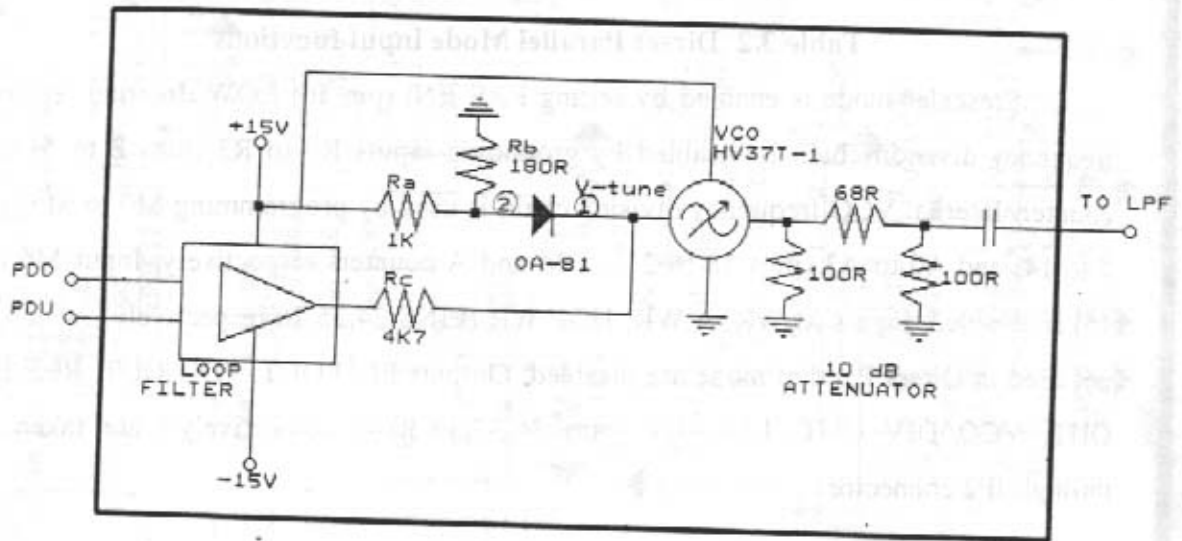
Fig. 4.1 Schematic for Loop Filter and VCO Subsystem

The schematic for Loop Filter and VCO subsystem is as illustrated in Fig. 4.1. As shown in the figure, supply of ±15V DC and +15V DC are applied to Loop Filter Op-amp and VCO respectively.

The double-ended outputs, PDD and PDU from PLL synthesizer subsystem are applied to Loop Filter. Output of Loop Filter is applied to V-tune pin of VCO. For frequency range of 200 MHz to 400 MHz, tuning voltage required at V-tune pin ranges from 2V to 18V. Therefore, any negative voltage should be prevented at V-tune pin. When the system is in unlocked condition, Loop Filter output voltage might go to negative saturation. Hence, it is required to design the circuit so that a certain positive voltage (1.5 V to 2 V) will be present at V-tune pin, irrespective of lock condition.

Diode and voltage divider circuit arrangement is as illustrated in Fig. 4.1. Voltage at point 2 is 2.2 V. Therefore, any negative voltage at the output of the Loop Filter will forward bias the diode.

The resulting circuit is as illustrated in Fig. 4.2.
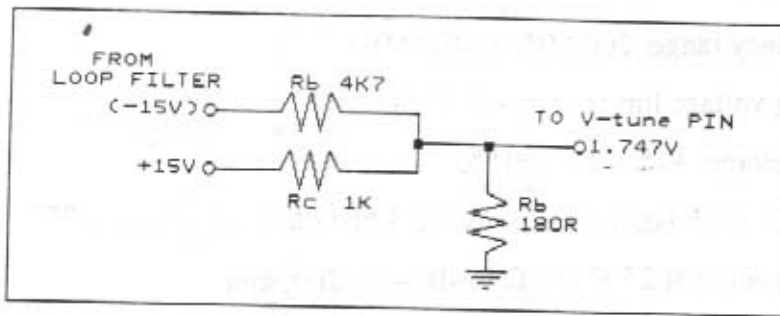
Fig. 4.2 Voltage divider

Thus, this arrangement protects the VCO from negative tuning voltage. Any positive output voltage of Loop Filter (2 V to 15 V), in locked condition will reverse bias the diode. Therefore, in locked condition voltage divider arrangement will not come into picture.

Output of VCO is applied at VCO IN pin of IC Q3216 through LPF and Power Divider. Output power level of VCO is in the range +10 dBm to +15 dBm. Input sensitivity range of IC Q3216 is −10 dBm to +5 dBm. To-make these two subsystems compatible with each other, a resistive attenuator of 10 dB (approximately) is used (taking into consideration 3-dB insertion loss of Power Divider) as illustrated in Fig. 4.1.

4.1.1 Selection Criteria of VCO:

The VCO should provide linear operation over its target frequency range, without sudden jumps in frequency or breaks in oscillation. The VCO's phase noise should meet following design criteria :

- Phase stability (spectral purity)
- Large gain factor (Kv)
- Linearity of frequency versus control voltage
- Large electrical tuning range
- Capability for accepting wide band modulation
- VCO must balance high Q, low phase noise and narrow tuning bandwidth against low Q, high phase noise and wide tuning bandwidth.

Required frequency range for the system is 200 MHz to 400 MHz

Magnum Microwave Voltage Controlled Oscillator HV37T-1 is selected with following specifications :

- Frequency range: 200 MHz to 400 MHz
- Tuning voltage limits: 0 to +20 V DC
- Bias voltage: +15 V DC (±1 %)
- Average modulation sensitivity: 12.5 MHz/V
- Power output at 25°C (50 Ω load): +10 dBm, min

The test procedure for the selected VCO is described in section 6.2.

4.1.2 Design of Loop Filter :

Selection Criteria of Op-amp:

- High input impedance
- Very high DC gain, so that the phase error between the reference and output signals is zero.
- Low bias current to minimize the reference oscillator sidebands.
- Low power consumption, small size
- Wide bandwidth to accommodate the given frequency range.
- High slew rate to handle high frequency signals of large amplitude

Op-amp used in differential configuration further rejects the reference sidebands because, the differential offset bias current is lower than the single ended offset bias current.

Op-amp OP-27 is selected with following specifications :

- It is a low noise precision operational amplifier.
- It allows accurate high gain (1.8 million) amplification of low-level signals.
- A gain-bandwidth product of 8 MHz and a2.8 V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.
- A low input bias current of ±10 nA is achieved by use of a bias current cancellation circuit. The output stage has good load driving capacity.

Magnum Microwave Voltage Controlled Oscillator HV37T-1 is selected with following specifications :

- Frequency range: 200 MHz to 400 MHz
- Tuning voltage limits: 0 to +20 V DC
- Bias voltage: +15 V DC (±1 %)
- Average modulation sensitivity: 12.5 MHz/V
- Power output at 25°C (50 Ω load): +10 dBm, min

The test procedure for the selected VCO is described in section 6.2.

4.1.2 Design of Loop Filter :

Selection Criteria of Op-amp:

- High input impedance
- Very high DC gain, so that the phase error between the reference and output signals is zero.
- Low bias current to minimize the reference oscillator sidebands.
- Low power consumption, small size
- Wide bandwidth to accommodate the given frequency range.
- High slew rate to handle high frequency signals of large amplitude

Op-amp used in differential configuration further rejects the reference sidebands because, the differential offset bias current is lower than the single ended offset bias current.

Op-amp OP-27 is selected with following specifications :

- It is a low noise precision operational amplifier.
- It allows accurate high gain (1.8 million) amplification of low-level signals.
- A gain-bandwidth product of 8 MHz and a2.8 V/µsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.
- A low input bias current of ±10 nA is achieved by use of a bias current cancellation circuit. The output stage has good load driving capacity.

Calculation of Loop Filter Component Values:
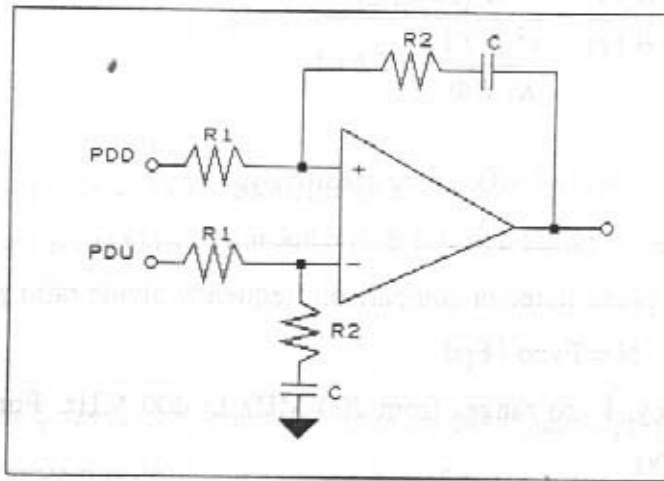
Fig. 4.3 First order Loop Filter

A second order type two PLL is implemented using the first order type one Loop Filter (shown in Fig. 4.3).

Transfer function of first order type one filter is given by:

$$F(s) = \frac{(1 + s.T2)}{s.T1} \qquad (4.1)$$

Where, $T1 = R1 \bullet C$ and $T2 = R2 \bullet C$
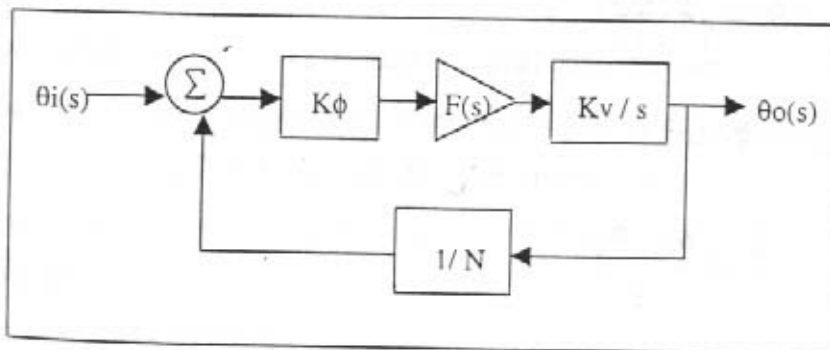
Fig. 4.4 Second order type 2 PLL

Fig. 4.4 shows second order type two PLL. The transfer function of output phase to input phase in terms of frequency is given by:

$$\frac{\theta_0(s)}{\theta_i(s)} = \frac{N.(1+s.T2)}{\dfrac{s^2.N.T1}{Kv.K\Phi} + s.T2 + 1}$$ (4.2)

Where, Kv (Rad/V Sec) is the VCO tuning sensitivity,

Kϕ (V/Rad) is the phase detector gain constant,

N is VCO to phase detector comparison frequency divide ratio given by:

$$N = Fvco / Fpd$$

VCO output frequency, Fvco ranges from 200 MHz to 400 MHz. For Fpd =1MHz, N ranges from 200 to 400.

Using standard control theory,

$$\frac{\theta_0(s)}{\theta_i(s)} = \frac{N.(1+s.T2)}{\dfrac{s^2}{\omega_n^2} + \dfrac{2.s.\zeta}{\omega_n} + 1}$$ (4.3)

Where, natural frequency is given as :

$$\omega_n = \sqrt{\frac{Kv.K\Phi}{N.T1}}$$ (4.4)

And the damping factor is given by:

$$\zeta = \frac{\omega_n \cdot T_2}{2}$$ (4.5)

From above equations,

$$R1 = \frac{Kv \cdot K\Phi}{\omega_n^2 \cdot N \cdot C}$$ (4.6)

$$R2 = \frac{2\zeta}{\omega_n.C} \qquad\qquad (4.7)$$

We have,

Kv = 2π•12.5 Rad/V Sec, VCO specification

Kϕ = 0.302 V/Rad, for Q3216

Design Criteria :

- Damping factor ζ has an important influence on the dynamic performance of the PLL. For $\zeta = 1$, the system is critically damped. For $\zeta > 1$, i.e. for overdamped system, the output will take more time to reach the steady state and the system becomes sluggish and slow. If the damping ratio, ζ is too small, the overshoot increases. Due these constraints, it is a design practice to select ζ in the range 0.7 to 1.
- From Eq. 4.4 and Eq. 4.5,

$$\zeta \propto \frac{1}{\sqrt{N}}$$

Hence, change in the Divide Ratio, N (200 to 400) changes the damping factor ζ. To restrict ζ in the range 0.7 to 1, system is designed with $\zeta = 0.85$ at N = 300.

- From Eq. 4.7 Reducing R2 decreases ζ and hence stability.
- Input impedance of Op-amp is determined by R1. Increase in R1 will increase the noise contribution by the Loop Filter if Op-amp noise performance is not that bad.

The natural frequency of oscillations, Fn is assumed to be 20 kHz.

We have, Fn = 20 kHz,

∴ ωn = 2π• 20 kRad/s

And $\zeta = 0.85$

Let C = 3.3 nF,

We get, R1 = 1.517 kΩ

And R2 = 4 kΩ

Components selected :

C = 3.3 nF

$R1 = 1.5\ k\Omega$

$R2 = 3.9\ k\Omega$

It is observed that, the above design does not provide adequate suppression at an offset of 1 MHz (i.e. Fpd) from the center frequency. Hence, proper optimization of the design is required.

Optimization of Phase Locked Loop:

The Q3216 digital phase detector supplies error information by generating pulses at the reference frequency with a duty cycle proportional to the phase error. Voltage offsets between the phase detector and VCO, caused by component mismatches, Op-amp input offsets, or other balances are transformed into a steady state phase-error. This results in error pulses of large amplitude and short duration that contain high power at many harmonics of Fpd. High frequency, large amplitude signals on the inputs of an Op-amp can cause non-linear saturation in the amplifier, greatly reducing its 'Gain-Bandwidth product'. This effect can be devastating to wide bandwidth PLLs.

One solution is to pre-filter the error pulses before they reach the active filter by inserting RC low pass section by splitting R1. The modified Loop Filter with the 'pre-integrator' filter is shown in Fig. 4.5.
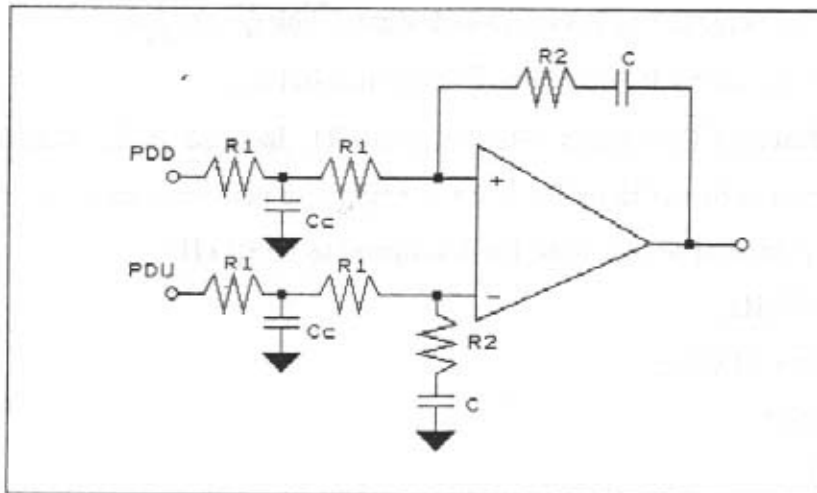
Fig. 4.5 Modified Loop Filter with pre-integrator

The addition of this circuit adds another pole, which can potentially degrade the phase margin. The time constant, Tc, and frequency, Fc, of the pole are given by:

$$Tc = \frac{R1.Cc}{4}$$

(4.8)

And,

$$Fc = \frac{1}{2\pi.Tc}$$

(4.9)

The pole should be placed far enough below the reference frequency to pre-filter the phase detector pulses enough to keep the Op-amp response linear and attenuate the reference spurs on the synthesizer output, while keeping it far enough above ωn so as not to degrade the phase margin.

From the first order lag filter design,

R1 = 1.517 kΩ

Inserting an RC low pass section by splitting R1,

R1/2 = 758 Ω

A rule of thumb is to place Fc greater than 10 times Fn (natural frequency of oscillations).

As Fn = 20 kHz,

Fc = 10 Fn = 200KHz

Using equations given above,

Cc = 2.84 nF

Components selected:

R1/2 = 750 Ω

Cc = 2.2 nF

- The schematic for Loop Filter and VCO is shown in Fig. 4.6.

  Performance of the system designed is evaluated in chapter 6, Section 6.3.
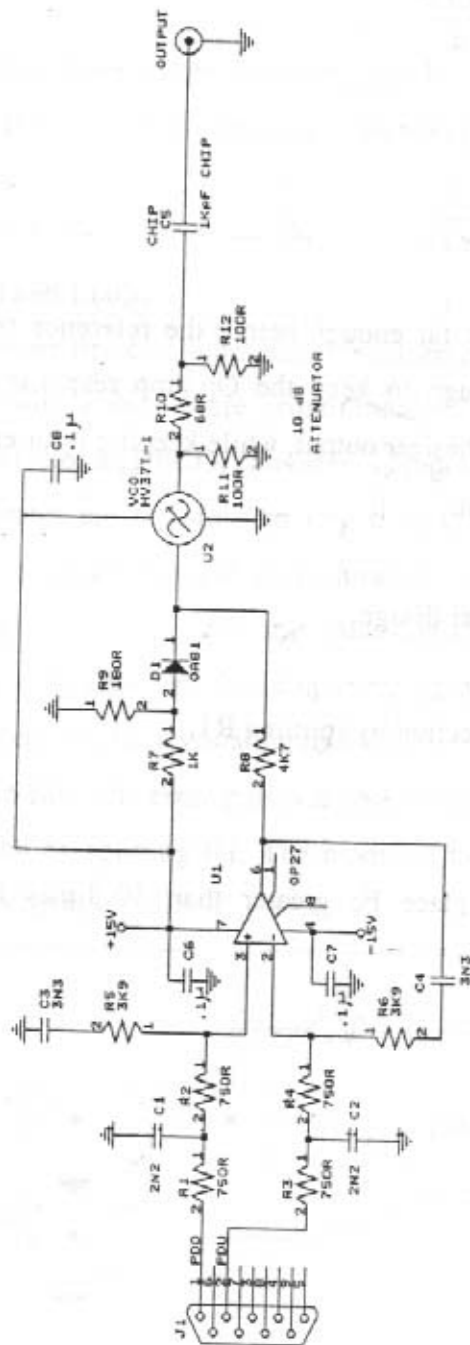
Fig 4.6 Loop Filter and VCO Subsystem

4.2 POWER DIVIDER AND LPF

Power divider :

Power Divider is a passive device, which accepts an input signal and delivers multiple output signals with specific phase and amplitude characteristics.

Selection criteria :

The output signals of power divider should possess following characteristics

- Equal amplitude
- Zero degree phase relationship between any two outputs
- High isolation between each output port.
- 3-dB (theoretical) insertion loss for two port power divider.

Mini-Circuits make power divider module, (PSC-2-1) is selected. The isolation between the output ports is of the order of 25 dB. Typical insertion loss is 3.4 dB. (Other details are given in Appendix F.) Performance characteristics viz. Insertion loss, Return loss and VSWR, of the power divider are given in Section 6.3.

Low Pass Filter :

A passive LC low pass filter with cut-off frequency 380 MHz is used for suppressing the harmonics present in the VCO output frequency. The typical harmonic suppression should be about 40 dBc. The Return loss and VSWR characteristics of the LPF are given in the Section 6.3.

5. PRACTICAL REALIZATION OF
· THE SYSTEM

5.1 Interface Control Drawing:

Fig. 5.1 and Fig. 5.2 give the top view and front – back panel view of the Plug in Unit (PIU), respectively.

5.2 Material List :

A. Connectors and Cables

Parts list :

B. PLL Synthesizer Subsystem

C. Loop filter and VCO
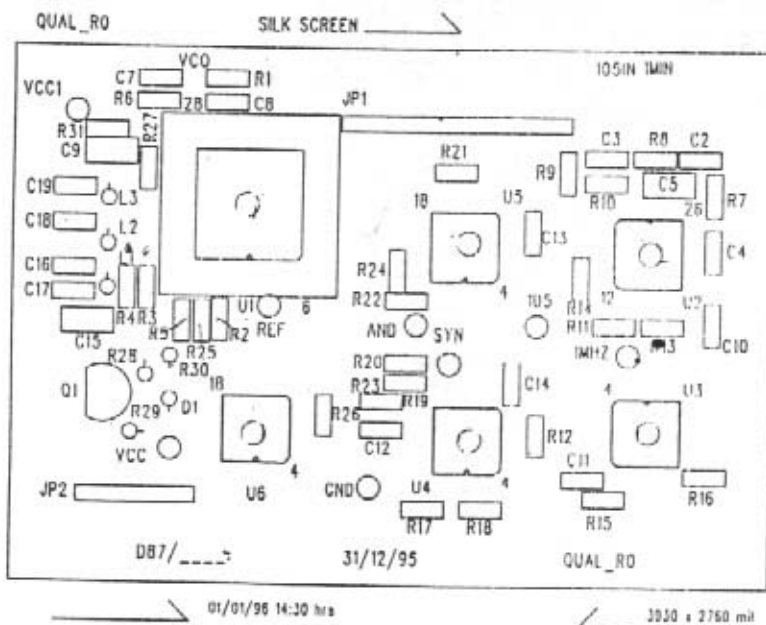
PLL Synthesizer Subsystem Component arrangement
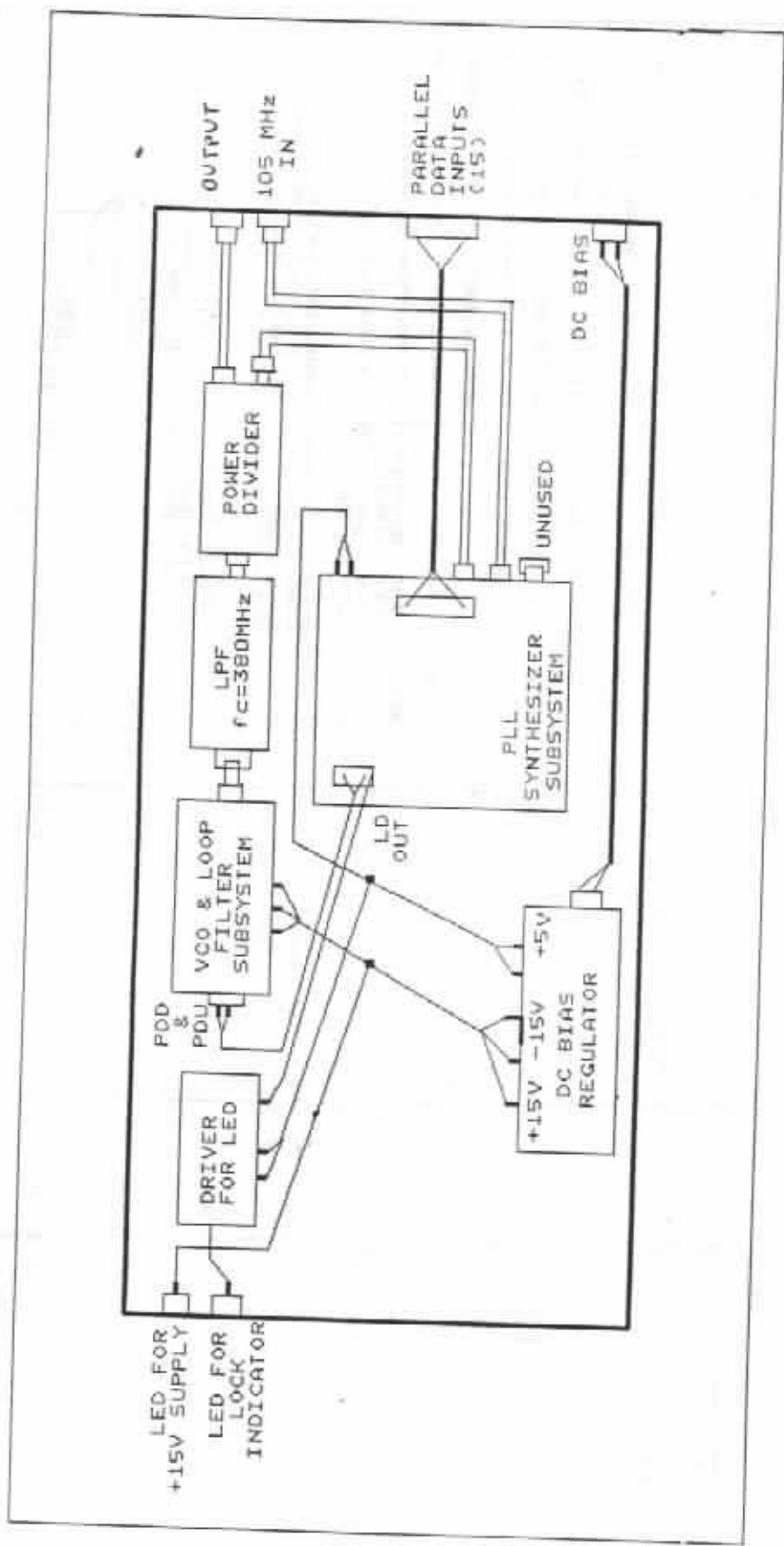
Fig. 5.1 Interface Control Drawing (Top view)

FRONT PANEL   BACK PANEL

PART NO.	DESCRIPTION	CONNECTION DETAILS
1	RED LED	'RED ON' = +15V SUPPLY OK
2	GREEN LED	'GREEN ON' = -15V SUPPLY OK
3	ORANGE LED	LOCK INDICATOR LED 'ORANGE ON' = LOOP PLOCKED
4	ORANGE LED	'ORANGE ON' = +5V SUPPLY OK
5 & 6	TNC, BULKHEAD FEED-THROUGH CABLE JACK FOR RG223 CABLE	5 = MONITORING PORT 6 = 105 MHz IN
7	D TYPE, 15 PIN FEMALE CONNECTOR (13 - NOT USED)	CONNECTED TO 15 PIN, D TYPE MALE CONNECTOR OF SWITCH MODULE (13 - NOT USED)
8	AMPHITRONIX, ROUND SHELL 5 PIN JACK AUDIO CONNECTOR	

+18V
GND
+18V
-18V

Fig. 5.2 Interface Control Drawing (Front panel–Back Panel)

MATERIAL LIST

A. CABLES AND CONNECTORS

SR. NO.	MATERIAL DESCRIPTION	PART NO.	QUANTITY	MANUFACTURER	USED IN
1.	0.141" Dia, 50 Ohm, Semi-rigid Coaxial Cable	UT141/A	1	Microcoax, USA	PIU
2.	RF Co-axial cable	RG223	1	TPI, India	PIU
3.	Flat Ribbon Cable (12 Core, 4 Core)	-	2	-	PIU
4.	TNC, Bulkhead, Feed-through, Cable Jack for RG223 cable	3104-7341-10	2	M/A COM, USA	PIU Back-panel(2)
5.	TNC, Straight Cable Plug for RG223 cable	3101-7341-10	1	M/A COM,USA	PIU
6.	TNC, Straight Cable Plug for 0.141" dia. Semi-rigid Cable, Direct Solder Attachment type	3101-7941-00	1	M/A COM, USA	PIU
7.	SMA, Straight Cable plug, Crimp Attachment for RG223 cable	2031-5011-02	1	M/A COM, USA	PIU

Fig. 5.2 Interface Control Drawing (Front panel-Back Panel)

PART NO.	DESCRIPTION	CONNECTION DETAILS
1	RED LED	'RED ON' = +15V SUPPLY OK
2	GREEN LED	'GREEN ON' = -15V SUPPLY OK
3	ORANGE LED	LOCK INDICATOR LED
4	ORANGE LED	'ORANGE ON' = LOOP PLOCKED
		'ORANGE ON' = +5V SUPPLY OK
5 & 6	TNC, BULKHEAD FEED-THROUGH CABLE JACK FOR RG223 CABLE	5 = MONITORING PORT 6 = 105 MHz IN
7	D TYPE, 15 PIN FEMALE CONNECTOR (13 - NOT USED)	CONNECTED TO 15 PIN, D TYPE MALE CONNECTOR OF SWITCH MODULE (13 - NOT USED)
8	AMPHITRONIX, ROUND SHELL 5 PIN JACK AUDIO CONNECTOR	

FRONT PANEL

BACK PANEL

MATERIAL LIST

A. CABLES AND CONNECTORS

SR. NO.	MATERIAL DESCRIPTION	PART NO.	QUANTITY	MANUFACTURER	USED IN
1.	0.141" Dia, 50 Ohm, Semi-rigid Coaxial Cable	UT141/A	1	Microcoax, USA	PIU
2.	RF Co-axial cable	RG223	1	TPI, India	PIU
3.	Flat Ribbon Cable (12 Core, 4 Core)	-	2		PIU
4.	TNC, Bulkhead, Feed-through, Cable Jack for RG223 cable	3104-7341-10	2	M/A COM, USA	PIU Back-panel(2)
5.	TNC, Straight Cable Plug for RG223 cable	3101-7341-10	1	M/A COM,USA	PIU
6.	TNC, Straight Cable Plug for 0.141" dia. Semi-rigid Cable, Direct Solder Attachment type	3101-7941-00	1	M/A COM, USA	PIU
7.	SMA, Straight Cable plug, Crimp Attachment for RG223 cable	2031-5011-02	1	M/A COM, USA	PIU

Sr. No	MATERIAL DESCRIPTION	PART NO.	QUANTITY	MANUFACTURER	USED IN
8.	SMA, Flange Mount Jack Receptacle,	2052-1201-02	4	M/A COM, USA	PLL Synthesizer subsystem(3), LPF(1)
9.	TNC , Flange Mount Plug Receptacle	3151-0000-10	1	M/A COM, USA	Power Divider(2) VCO & LPF subsystem(1)
10.	TNC, Flange Mount Jack Receptacle	3152-0000-10	1	M/A COM, USA	LPF subsystem
11.	SMA, Flange Mount Plug Receptacle	2051-1201-02	1	M/A COM,USA	Power Divider
12.	SMA, Straight Cable Plug for 0.141" Dia., Semi-rigid Cable, Direct Solder Attachment type	11SMA50-3-56C	1	Huber & Shuner, Switzerland	PIU
13.	D type, 9-pin, Female Connector	-	1	O/E/N	PIU
14.	D type, 9-pin, Right Angle, Male Connector	-	1	O/E/N	VCO & LPF Subsystem
15.	D type, 15-pin, Female Connector	-	1	O/E/N	PIU

Sr. No	MATERIAL DESCRIPTION	PART NO.	QUANTITY	MANUFACTURER	USED IN
16.	D type, 15-pin, Male Connector	-	1	O/E/N	Switch module
17.	Feed-through Capacitor (EMI filter),1500pF, 200V, 10A DC	51-712-014	1	Spectrum Control, USA	All Supply points
18.	5-pin, Audio Connector, Panel Mount, Female Socket	91-336006-H	1	Amphetronix, Pune	PIU
19.	FRC, 12-pin, Female Connector	-	1	-	PIU
20.	FRC, 6-pin, Female Connector		1	-	PLL Synthesizer subsystem

B. **PLL SYNTHESIZER SUBSYSTEM - PARTS LIST**

Sr. No	SYMBOL	QUANTITY	PACKAGE STYLE	VALUE	TOLER-ANCE	RATINGS	MATERIAL DESCRIPTION	MANUFA-CTURER
1	R1,R3,R4	3	Chip	100E	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.

Sr. No	MATERIAL DESCRIPTION	PART NO.	QUANTITY	MANUFACTURER	USED IN
16.	D type, 15-pin, Male Connector	-	1	O/E/N	Switch module
17.	Feed-through Capacitor (EMI filter),1500pF, 200V, 10A DC	51-712-014	1	Spectrum Control, USA	All Supply points
18.	5-pin, Audio Connector, Panel Mount, Female Socket	91-336006-H	1	Amphetronix, Pune	PIU
19.	FRC, 12-pin, Female Connector	-	1		PIU
20.	FRC, 6-pin, Female Connector		1	-	PLL Synthesizer subsystem

B. PLL SYNTHESIZER SUBSYSTEM - PARTS LIST

Sr. No	SYMBOL	QUAN TITY	PACKAGE STYLE	VALUE	TOLER- ANCE	RATINGS	MATERIAL DESCRIPTION	MANUFA- CTURER
1	R1,R3,R4	3	Chip	100E	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.

Sr. No	SYMBOL	QUAN TITY	PACKAGE STYLE	VALUE	TOLER- ANCE	RATINGS	MATERIAL DESCRIPTION	MANUFA- CTURER
1	R2,R8,R10,R11,R12, R13,R14,R15,R16, R17,R18,R19,R20, R21,R22,R23,R24, R25,R26	19	Chip	330E	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.
2	R5,R6,R27,	3	Chip	510E	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.
3	R7,R9	2	Chip	47E	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.
4	R28	1	Chip	10K	± 5 %	¼ W @ 70° C, 200 V rms	thick film chip resistor	RS components, U.K.
5	R29	1	Axial lead	270E	± 5 %	¼ W @ 70° C, 300 V DC max	Carbon film resistor	Thermax
6	R30	1	Axial lead	270E	± 5 %	¼ W @ 70° C, 300 V DC max	Carbon film resistor	Thermax
7	R31	1	Chip	39K	± 5 %	¼ W @ 70° C, 200 Vrms	thick film chip resistor	RS components

Sr. No	SYMBOL	QUAN-TITY	PACKAGE STYLE	VALUE	TOLER-ANCE	RATINGS	MATERIAL DESCRIPTION	MANUFA-CTURER
9	C2,C3	2	Chip	10kpF	±5 %	50 V DC	Multilayer ceramic chip capacitor	AVX, USA
10	C4,C10,C11,C12 C13,C14,C16,C17 C18,C19	10	Chip	0.1µF	±20 %	50 V DC	Multilayer ceramic chip capacitor	AVX, USA
11	C5	1	Radial Case T350	10µF	±20 %	35 V @ 85 °C	Solid tantalum capacitor	Kemet, USA
12	C7,C8	2	Chip	1 KpF	±5 %	50 V DC	Ceramic chip capacitor	AVX, USA
13	C9	1	Radial Case	1 µF	±20 %	50 V DC	Ceramic capacitor	Philips
14	C15	1	Radial Case	33 µF	±20 %	50 V DC	Electrolytic capacitor	Philips

Sr. No	CIRCUIT SYMBOL	PART NO.	PACKAGE STYLE	COMPONENT DESCRIPTION	MANUFACTURER
1	U1	Q3216	44-PIN PLCC	1.6 GHz PLL Synthesizer IC	Qualcomm, USA
2	U2	100E116	28-PIN PLCC	Differential line receiver	Motorola, USA
3	U3	100E131	28-PIN PLC	4-bit D flip-flop	Motorola, USA
4	U4	100E0101	28-PIN PLCC	Quad 4-input OR/NOR Gate	Motorola, USA
5	U5	100E016	28-PIN PLCC	8-bit binary up-counter	Motorola, USA
6	U6	100E104	28-PIN PLCC	2-input AND/NAND Gate	Motorola, USA

C. LOOP FILTER AND VCO SUBSYSTEM – PARTS LIST

Sr. No	SYMBOL	QUAN TITY	PACKAGE STYLE	VALUE	TOLER- ANCE	RATINGS	MATERIAL DESCRIPTION	MANUFA- CTURER
1	R1,R2,R3,R4	4	Axial lead	750R	±5 %	¼ W @ 70°C 300 V DC max	Carbon film resistor	Thermax
2	R5,R6	2	Axial lead	3.9K	±5 %	¼ W @ 70°C 300 V DC max	Carbon film resistor	Thermax
3	R7	1	Axial lead	1K	±5 %	¼ W @ 70°C 300 V DC max	Carbon film resistor	Thermax
4	R8	1	Axial lead	4.7K	±5 %	¼ W @ 70°C 300 V DC max	Carbon film resistor	Thermax
5	R9	1	Axial lead	180R	±5 %	¼ W @70 °c 300 V DC max	Carbon film resistor	Thermax
6	R10	1	Axial lead	68R	±5 %	¼ W @70 °c 300 V DC max	Carbon film resistor	Thermax
7	R11,R12	2	Axial lead	100R	±5 %	¼ W @70 °c 300 V DC max	Carbon film resistor	Thermax
8	C1,C2	2	Radial Case	2.2 nF	±20 %	50 V DC	Ceramic disc capacitor	Philips
9	C3,C4	2	Radial Case	3.3 nF	±20 %	50 V DC	Ceramic disc capacitor	Philips
10	C5	1	Chip	1 KpF	±5 %	50 V DC	Multi layer ceramic disc capacitor	AVX, USA
11	C6,C7,C8	3	Radial Case	0.1 µF	±20 %	50 V DC	Ceramic disc capacitor	Philips

Sr. No	CIRCUIT SYMBOL	PART NO.	PACKAGE STYLE	COMPONENT DESCRIPTION	MANUFACTURER
1	U1	OP-27	8-PIN DIP	Low noise precision Op-amp	Precision Monolithic Inc., USA
2	U2	HV37T-1	TO-8	200 to 400 MHz	Magnum Microwave, USA
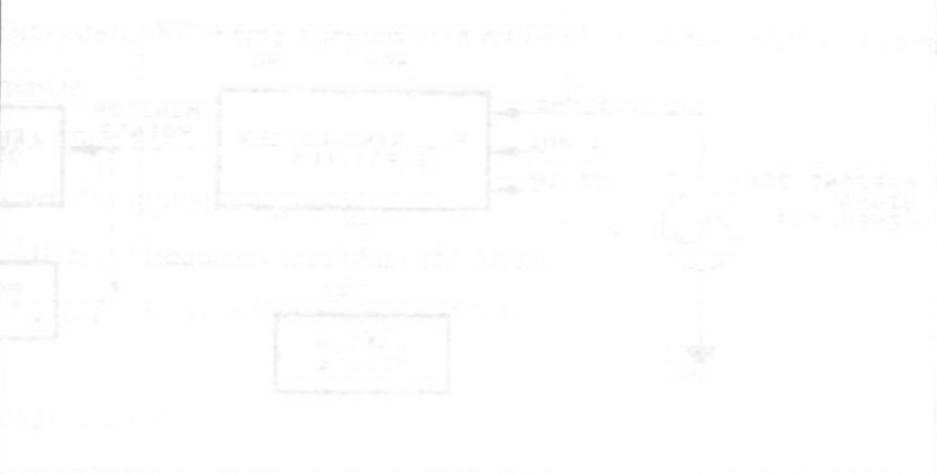
6. TESTS AND PERFORMANCE EVALUATION OF THE SYSTEM

6.1 Test Procedure Of PLL Synthesizer Subsystem

The Test setup for PLL Synthesizer Subsystem is as shown in Fig. 6.1
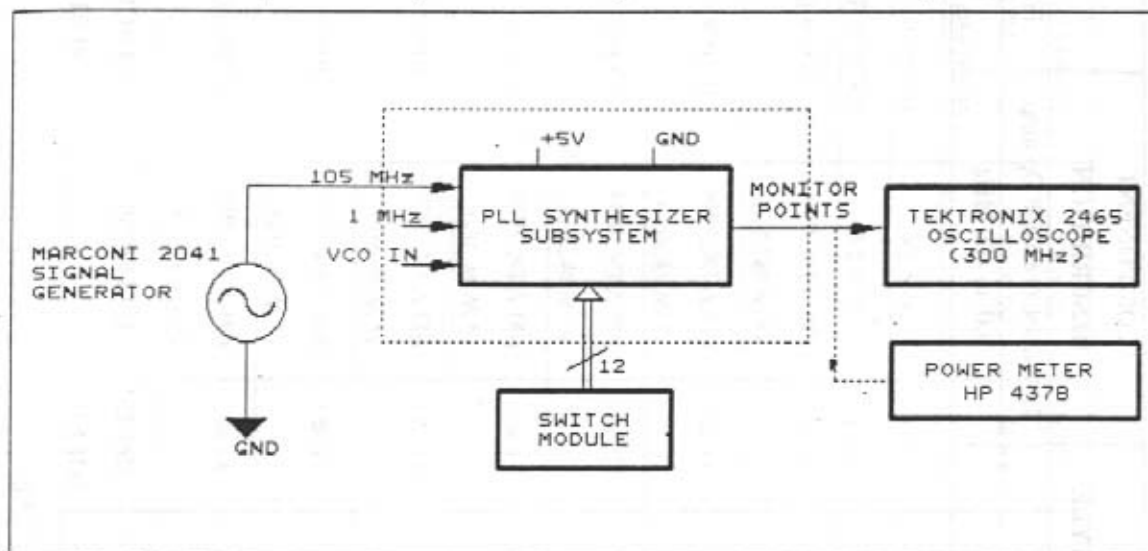

Fig. 6.1 Test setup for PLL Synthesizer Subsystem.

A supply of +5 V DC is applied to the Synthesizer Subsystem. Current drawn from the supply is noted. IC Q3216 is used in Direct Parallel mode. For loading parallel data inputs, through JP2 connector, binary switches (SPDT) are used.

The waveforms observed at various monitoring ports, M1 to M5 are shown in Fig. 6.2.

- Initially, 105 MHz signal is applied at the reference input terminal of Synthesizer Subsystem. The applied signal is monitored at monitoring port M2.

- Switches S1 and S2 are set to 1 and 0 respectively (For step size = 1 MHz), to convert reference input frequency, 105 MHz down to phase detector frequency (Fpd), 1 MHz. It is monitored at port M5 (Ref).

- Switches S1 and S2 are then set to 0 and 1 respectively (For step size = 5 MHz), to get Fpd = 5 MHz and is monitored at port M5.

- Keeping the same setup as above, synchronization signal is monitored at port M3 (SYNC). It should give a continuous HIGH output as shown in Fig. 6.2.
- Using Signal Generator, 1 MHz signal (power level = 0 dB) is applied at the '1 MHz' input terminal of PLL Synthesizer subsystem. Irrespective of the switch arrangement, output of Line Receiver (square wave of 1 MHz) is observed at port M1. The signal at port M3 is checked for synchronization pulses of 1 MHz.
- Output of 'AND' gate is monitored at port M4, for both 1 MHz and 5 MHz step size.
- Externally applied 1 MHz signal is removed. Using signal generator, signals of various frequencies (power level 0 dB) are applied to 'VCO IN' input terminal of Synthesizer Subsystem. VCO frequency division ratios M and A are calculated using following formulae.

$$N = Fvco / Fpd$$

Where, Fvco = externally applied frequency.

and   Fpd = 1 MHz, for frequency resolution of 1 MHz

           = 5 MHz, for frequency resolution of 5 MHz

As, $M = integer (N/10) - 1$

         $A = N-[10(M+1)]$

Binary equivalent of M and A are loaded using switch arrangement.

Fvco (kHz)	FPD = 1 MHz			FPD = 5 MHz		
	N	M	A	N	M	A
200	200	19	0	40	39	0
400	400	39	0	80	79	0
1490	1490	148	0	298	28	8

Table 6.1 Counter inputs for various frequencies

For the settings illustrated in Table 6.1, waveforms at various pins of connector JP1 (PDD, PDU, VCO DIV OUT, REF DIV OUT) are observed.
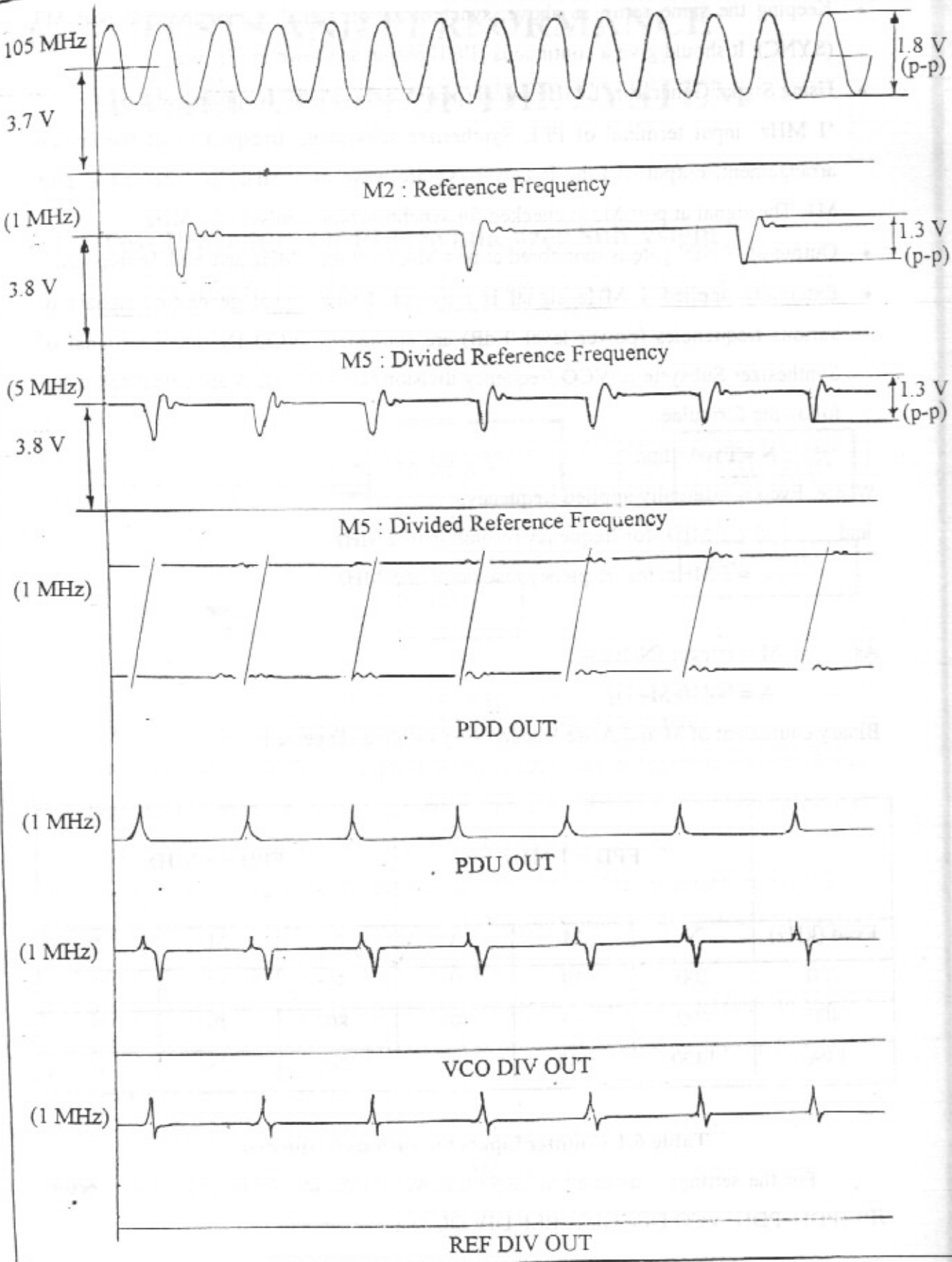
105 MHz

3.7 V — 1.8 V (p-p)

M2 : Reference Frequency

(1 MHz)

3.8 V — 1.3 V (p-p)

M5 : Divided Reference Frequency

(5 MHz)

3.8 V — 1.3 V (p-p)

M5 : Divided Reference Frequency

(1 MHz)

PDD OUT

(1 MHz)

PDU OUT

(1 MHz)

VCO DIV OUT

(1 MHz)

REF DIV OUT

Fig. 6.2 Performance Results of PLL Synthesizer Subsystem. (Not to the scale)
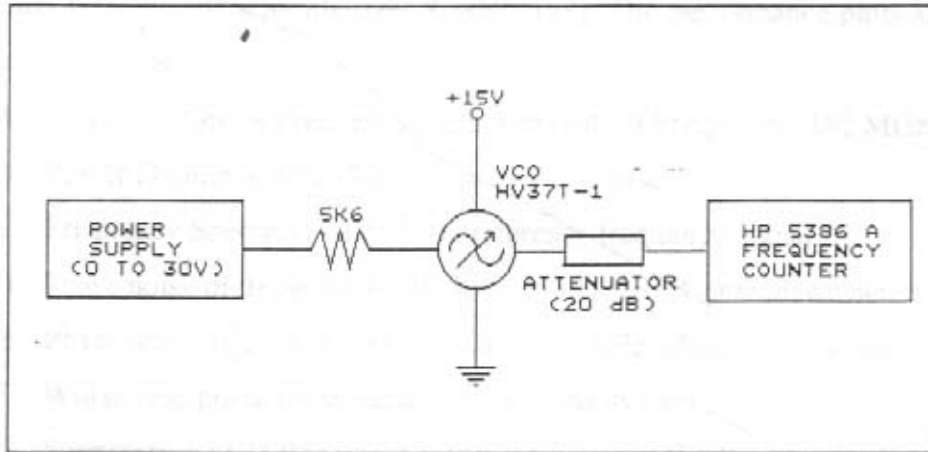
6.2 Characterization of VCO HV37T-1

Fig 6.3 Test setup for characterization of VCO HV37T-1

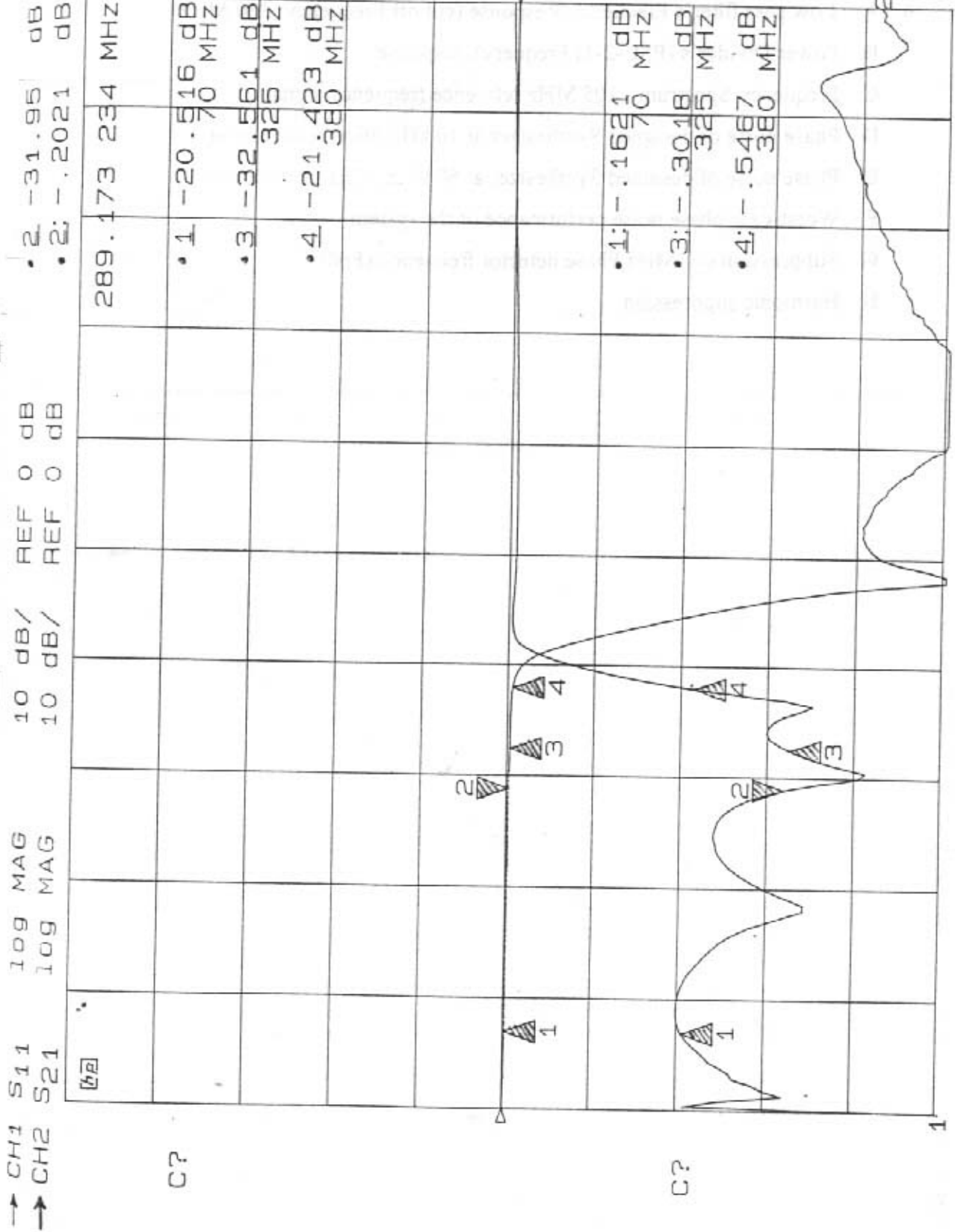The performance of VCO can be tested using the test set up shown in Fig. 6.3. Supply of +15 V DC is applied at the 'DC Voltage' pin of VCO HVT37-1. VCO can be tuned to a certain frequency in the range 200 MHz to 400 MHz by applying DC voltage at 'V-tune' pin of VCO, using a variable power supply (0-30 V). A resistor of 5.6 kΩ (any high value resistor) is used as a current limiting resistor. VCO output frequency is observed on frequency counter (HP 5386 A, 90 MHz to 3 GHz). Input power level of frequency counter is +7 dBm (max), whereas VCO output power level ranges from +10 dBm to +15 dBm for the frequency range of 200 MHz to 400 MHz. Hence a '20 dB' attenuator is used to make VCO and the frequency counter compatible. The performance characteristics of VCO (tuning voltage Vs frequency and output power Vs frequency) are as shown in Fig. 6.4a and 6.4b.

POWER(dBm)

FREQUENCY(MHz)

FREQUENCY(MHz)
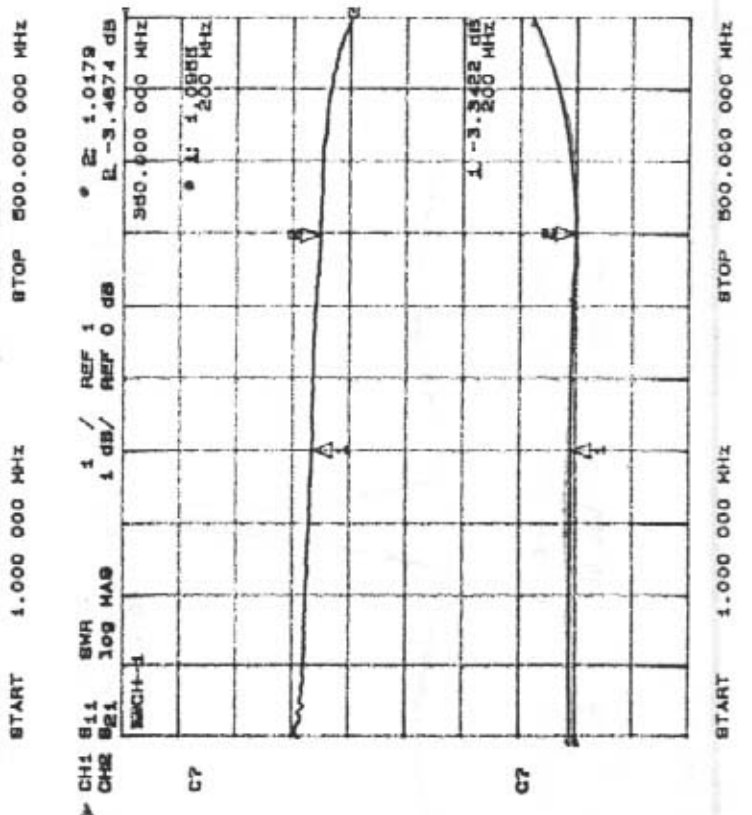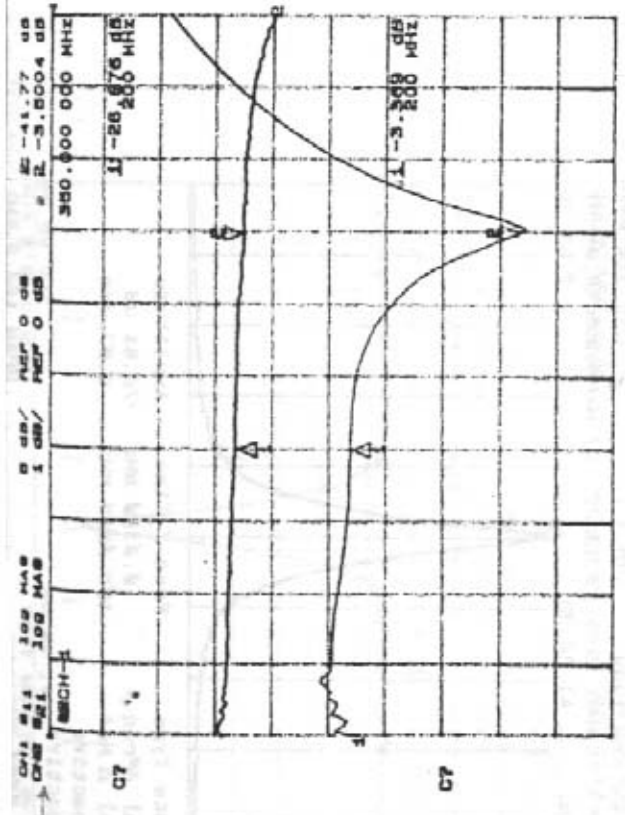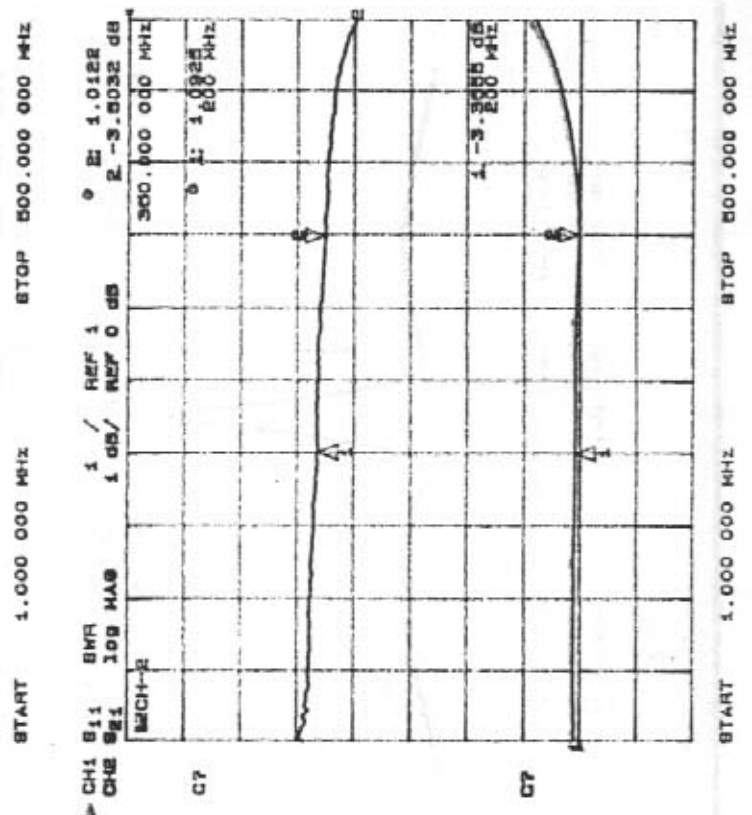
Fig 6.4 Performance Characterization
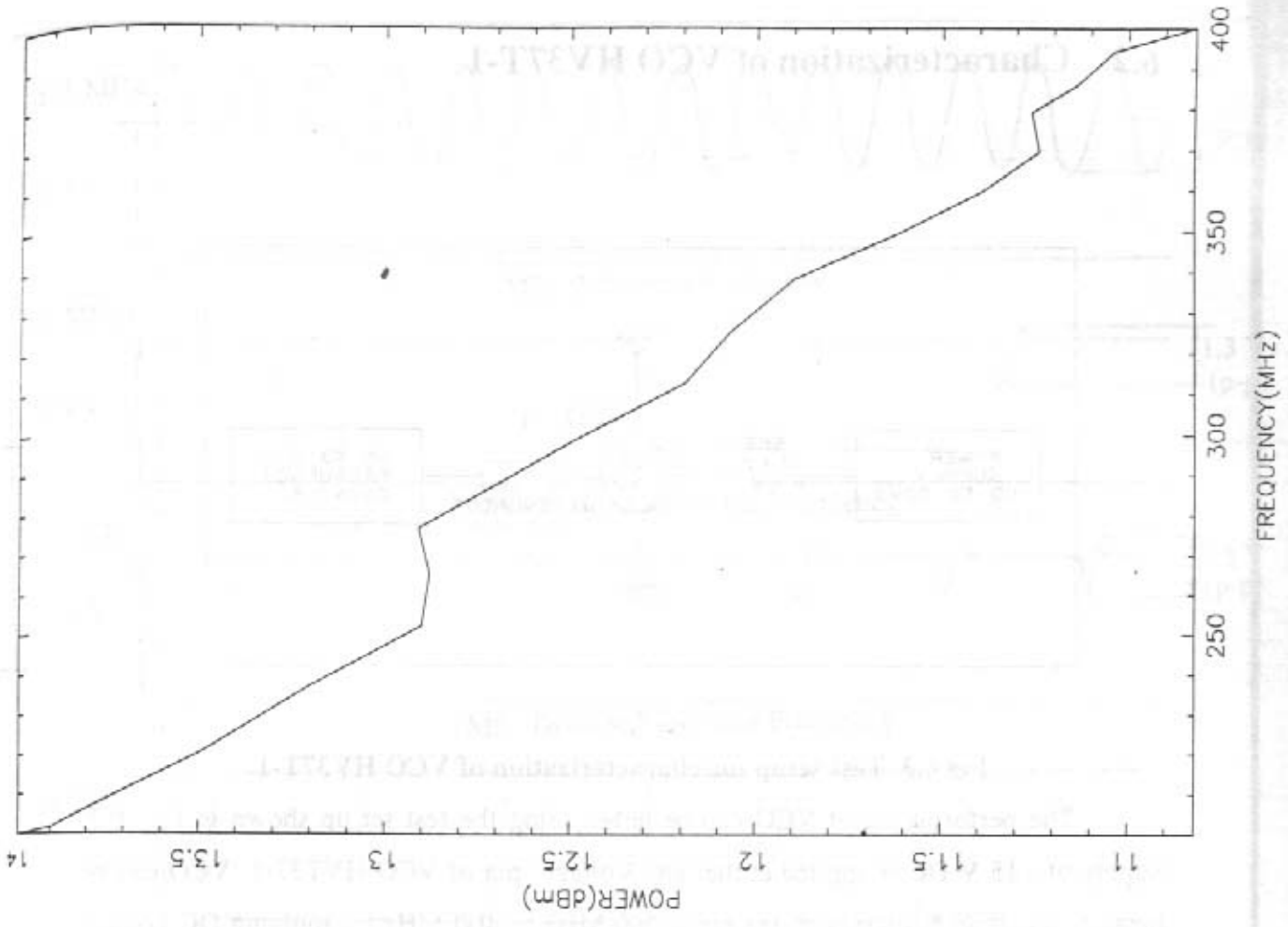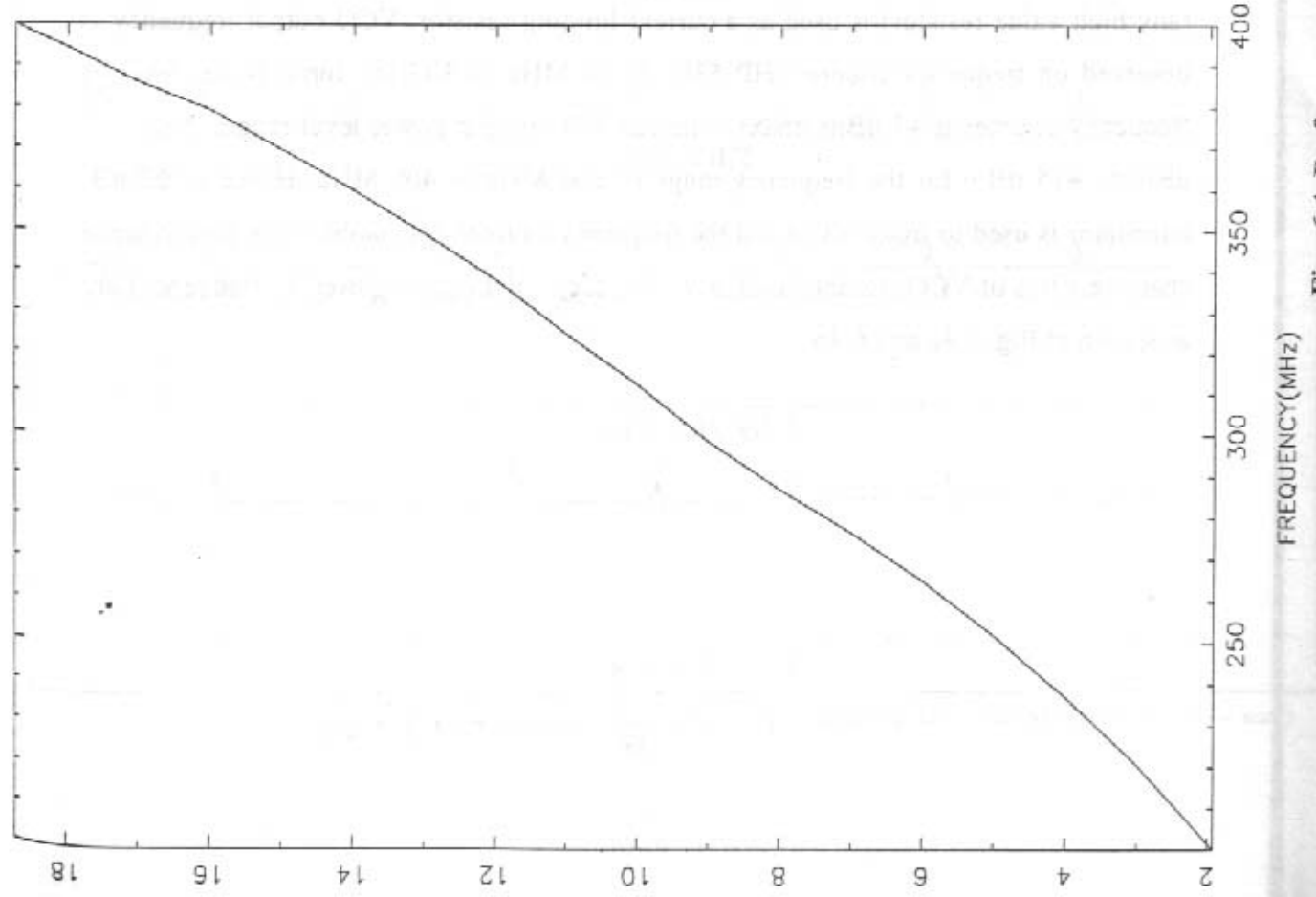
6.3   PERFORMANCE EVALUATION OF SYSTEM

Fig. 6.5 illustrates the performance of various subsystems viz. Power Divider, LPF and the Frequency Synthesizer System itself. The performance plots are arranged in following manner.

6.5 A. Low pass filter's Frequency Response (cut off Frequency, 380 MHz)

B. Power Divider's (PSC-2-1) Frequency response.

C. Frequency Spectrum - 105 MHz reference frequency signal.

D. Phase noise of designed Synthesizer at 10 kHz offset from carrier.

E. Phase noise of designed Synthesizer at 50 kHz offset from carrier.

F. Worst-case phase noise performance of the system.

G. Suppression of 1MHz Phase detector frequency (Fpd).

H. Harmonic suppression

→ CH1 S11   log MAG   10 dB/   REF 0 dB   .2 -31.95 dB
↑ CH2 S21   log MAG   10 dB/   REF 0 dB   .2 -.2021 dB

289.173 234 MHz

1: -20.516 dB   70 MHz
3: -32.561 dB   325 MHz
4: -21.423 dB   360 MHz

1: -.1621 dB   70 MHz
3: -.3018 dB   325 MHz
4: -.5467 dB   360 MHz

C?

C?

START   .300 000 MHz   STOP 1 000.000 000 MHz

12: 17: 05 02 APR 1999
13: 45: 06 31 MAR 1999 13: 53: 25 31 MARKERS 50.0 kHz
-77.62 dB
REF 10.0 dBm AT 20 dB
SMPL
LOG
10
dB/

Marker Trace Type	Freq / Time	Amplitude
1: (A) ΔFreq	0.0500 MHz	-77.62 dB
2: (A) Δ Ref	106.0010 MHz	0.22 dBm
3: Inactive		
4: Inactive		

CENTER 105.0000 MHz SPAN 200.0 kHz
RES BW 3.0 kHz VBW 3 kHz SWP 100 msec

12: 14: 01 02 APR 1999
13: 45: 06 31 MAR 1999 13: 53: 25 31 MARKERS 10.0 kHz
-70.61 dB
REF 10.0 dBm AT 20 dB
SMPL
LOG
10
dB/

Marker Trace Type	Freq / Time	Amplitude
1: (A) ΔFreq	0.0100 MHz	-70.61 dB
2: (A) Δ Ref	105.0000 MHz	0.07 dBm
3: Inactive		
4: Inactive		

CENTER 105.0000 MHz SPAN 100.0 kHz
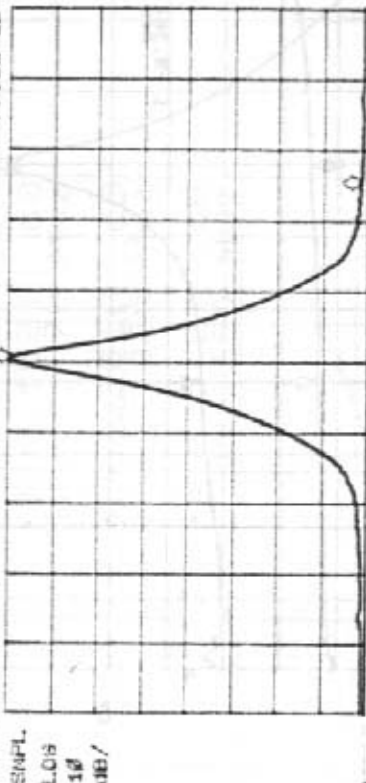RES BW 1.0 kHz VBW 1 kHz SWP 300 msec

Marker Trace Type | Freq / Time | Amplitude
1: (A) Freq | 0.0000 MHz | -60.66 dB
2: (A) Δ Ref | 210.0000 MHz | -4.27 dBm
3: Inactive
4: Inactive

CENTER 210.0000 MHz   SPAN 100.0 kHz
RES BW 1.0 kHz   VBW 1 kHz   SWP 300 msec

REF .0 dBm   AT 10 dB
SMPL
LOG
10
dB/

MKR Δ 10.0 kHz
-66.66 dB

Marker Trace Type | Freq / Time | Amplitude
1: (A) Freq | 0.0000 MHz | -60.81 dB
2: (A) Δ Ref | 250.0000 MHz | -4.63 dBm
3: Inactive
4: Inactive

CENTER 250.0000 MHz   SPAN 100.0 kHz
RES BW 1.0 kHz   VBW 1 kHz   SWP 300 msec

REF 10.0 dBm   AT 20 dB
LOG
10
dB/

-62.81 dB

Marker Trace Type | Freq / Time | Amplitude
1: (A) Freq | 0.0000 MHz | -62.99 dB
2: (A) Δ Ref | 300.0000 MHz | -5.60 dBm
3: Inactive
4: Inactive

CENTER 300.0000 kHz   SPAN 100.0 kHz
RES BW 1.0 kHz   VBW 1 kHz   SWP 500 msec

REF .0 dBm   AT 10 dB
LOG
10
dB/

-60.50 dB

Marker Trace Type | Freq / Time | Amplitude
1: (A) Freq | 0.0000 MHz | -57.15 dB
2: (A) Δ Ref | 350.0000 MHz | -6.54 dBm
3: Inactive
4: Inactive

CENTER 350.0000 MHz   SPAN 100.0 kHz
RES BW 1.0 kHz   VBW 1 kHz   SWP 300 msec

REF .0 dBm   AT 10 dB
LOG
10
dB/

-5.13 dB

(o)

Top-left plot:

Marker Trace Type | Freq / Time | Amplitude
1: (A) ΔFreq | 0.0385 MHz | -62.97 dB
2: (A) Δ Ref | 249.9995 MHz | -4.17 dBm
3: Inactive
4: Inactive

Bottom-left plot:

Marker Trace Type | Freq / Time | Amplitude
1: (A) ΔFreq | 0.0098 MHz | -50.87 dB
2: (A) Δ Ref | 200.0003 MHz | -3.70 dBm
3: Inactive
4: Inactive

Top-right plot:

Marker Trace Type | Freq / Time | Amplitude
1: (A) ΔFreq | 0.0295 MHz | -49.78 dB
2: (A) Δ Ref | 327.0000 MHz | -3.85 dBm
3: Inactive
4: Inactive

Bottom-right plot:

Marker Trace Type | Freq / Time | Amplitude
1: (A) ΔFreq | 0.0320 MHz | -50.96 dB
2: (A) Δ Ref | 300.0000 MHz | -3.93 dBm
3: Inactive
4: Inactive

Top-left plot:

REF .0 dBm   31 MAR 1999 13:53:25   3.000.000 MHz
     AT 10 dB   -71.76 dB

PEAK
LOG
10
dB/

Marker	Trace	Type	Freq / Time	Amplitude
1:	(A)	Freq	1.000 kHz	-71.76 dB
2:	(A)	Δ Ref	200.025 kHz	-3.91 dBm
3:		Inactive		
4:		Inactive		

CENTER 200.000 MHz   SPAN 5.000 MHz
RES BW 30 kHz   VBW 30 kHz   SWP 20.0 msec

Bottom-left plot:

12:53:20   02 APR 1999
REF .0 dBm   31 MAR 1999 13:53:25   31 MAR 1999.000 MHz
     AT 10 dB   -62.30 dB

PEAK
LOG
10
dB/

Marker	Trace	Type	Freq / Time	Amplitude
1:	(A)	Freq	1.000 kHz	-62.30 dB
2:	(A)	Δ Ref	270.025 MHz	-3.91 dBm
3:		Inactive		
4:		Inactive		

CENTER 270.000 MHz   SPAN 5.000 MHz
RES BW 30 kHz   VBW 30 kHz   SWP 20.0 msec

Top-right plot:

REF .0 dBm   31 MAR 1999 13:53:25   31 MAR 233.000 MHz
     AT 10 dB   -61.53 dB

PEAK
LOG
10
dB/

Marker	Trace	Type	Freq / Time	Amplitude
1:	(A)	Freq	1.000 kHz	-61.63 dB
2:	(A)	Δ Ref	233.025 kHz	-3.91 dBm
3:		Inactive		
4:		Inactive		

CENTER 233.000 MHz   SPAN 5.000 MHz
RES BW 30 kHz   VBW 30 kHz   SWP 20.0 msec

Bottom-right plot:

12:56:30   02 APR 1999
REF .0 dBm   31 MAR 1999 13:53:25   31 MAR 327.000 MHz
     AT 10 dB   -62.25 dB

PEAK
LOG
10
dB/

Marker	Trace	Type	Freq / Time	Amplitude
1:	(A)	Freq	1.000 kHz	-62.25 dB
2:	(A)	Δ Ref	327.025 kHz	-3.91 dBm
3:		Inactive		
4:		Inactive		

CENTER 327.000 MHz   SPAN 5.000 MHz
RES BW 30 kHz   VBW 30 kHz   SWP 20.0 msec

Top-left:

Marker Trace Type		Freq / Time	Amplitude
1:	(A) Freq	216.0 kHz	-4.00 dBm
2:	(A) Freq	432.6 kHz	-31.76 dBm
3:	(A) Freq	620.4 kHz	-66.19 dBm
4:	Inactive		

Top-right:

Marker Trace Type		Freq / Time	Amplitude
1:	(A) Freq	228.6 kHz	-4.12 dBm
2:	(A) Freq	460.6 kHz	-47.29 dBm
3:	(A) Freq	670.4 kHz	-64.72 dBm
4:	Inactive		

Bottom-left:

Marker Trace Type		Freq / Time	Amplitude
1:	(A) Freq	298.8 kHz	-3.89 dBm
2:	(A) Freq	600.6 kHz	-66.26 dBm
3:	(A) Freq	900.6 kHz	-65.95 dBm
4:	Inactive		

Bottom-right:
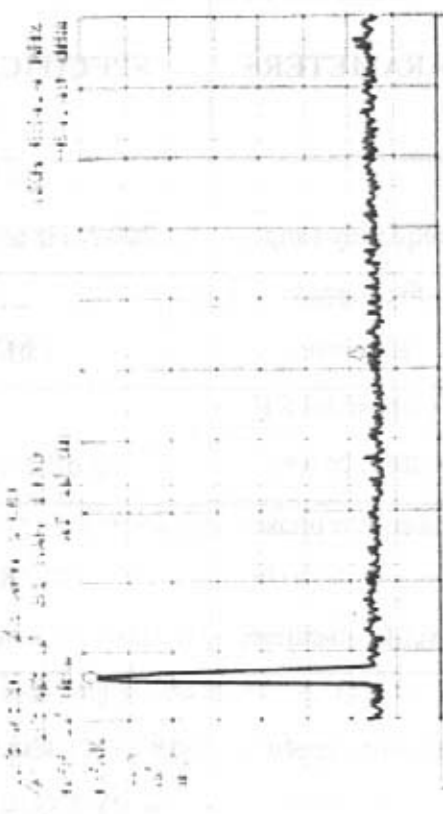
Marker Trace Type		Freq / Time	Amplitude
1:	(A) Freq	325.0 kHz	-3.78 dBm
2:	(A) Freq	654.4 kHz	-64.49 dBm
3:	Inactive		
4:	Inactive		

The following table summarizes performance test results :

PARAMETERS	SPECIFICATIONS	RESULTS
Frequency range	200 MHz to 400 MHz	200 MHz to 350 MHz *
Frequency resolution	1 MHz	1MHz
Synthesized RF output power	-3 dBm ±2 dBm	-3 dBm ±2 dBm
Minimum phase noise @ 10 kHz offset from carrier	-80 dBc/Hz	-80 dBc/Hz
Power supply	+18V DC, less than 150mA -18V DC, less than 100 mA +10V DC, less than 1A	+18V DC, 95 mA -18V DC, 42 mA +10V DC, 90 mA
Spectral Purity	Harmonic contents less than –30 dBc, Other Spurious products less than –40 dBc	Harmonic contents : For 210 MHz, -30 dBc 295 MHz, -60 dBc 340 MHz, -60 dBc Other Spurious Products less than –40 dBc
Suppression at 1 MHz (Fpd) offset from carrier	Less than –60 dBc	For 200 MHz, -70 dBc 270 MHz, -60 dBc 327 MHz, -60 dBc

*note : The maximum frequency that can be synthesized from the designed system is 350 MHz. This is due to the fact that the supply voltage that can be applied to OP-27 is 30 V (max). In the designed system, OP-27 is given supply of ±15 V, which restricts the

(max). In the designed system, OP-27 is given supply of ±15 V, which restricts the maximum tuning voltage at V-tune pin of VCO to 15 V. This imposes the limit on the maximum obtainable frequency.

Plot 6.5A shows performance characteristics of LPF

- Return loss ranges from -20 dB to -30 dB
- Insertion loss ranges from -0.15 dB to 0.5 dB

Plot 6.5B shows performance characteristics of Power Divider, PSC-2-1

- Return loss ranges from -25 dB to -40 dB
- Insertion loss ranges from -3.3 dB to -3.5 dB
- VSWR : 1.01 to 1.09

Plots from 6.5C to 6.5H show overall phase noise performance of the system at offsets of 10 kHz, 50 kHz, 1 MHz etc.

As mentioned in Section 2.2, at frequency offsets less than loop bandwidth, the Synthesizer output phase noise consists of reference Phase noise, Q3216 frequency divider/phase detector noise floor and the Op-amp active filter's noise.

Fig. 6.5D shows Synthesizer output Phase noise measured with 1 kHz resolution Bandwidth at Frequency offset of 10 kHz. The plot shows that, at 10 kHz offset, the output phase noise is about −67 dBc (Center Frequency, 210 MHz). Therefore, phase noise in 1 Hz bandwidth can be calculated as follows :

Phase noise = -67-10 log (1k) dBc/Hz

= -97 dBc/Hz @10 kHz offset

It should be noted that, the reference Phase noise power is multiplied by 20log(N) and low pass filtered by the loop. As divide ratio, N varies from Nmin to Nmax (i.e. 200 to 400); minimum degradation of about 4 dB will always be present in System performance. In our case, the phase noise degradation at 10 kHz offset is from −97 dBc/Hz to -88 dBc/Hz approximately.

As mentioned in the Appendix C, the phase noise of VCO HV37T-1 at 50 kHz offset is −110 dBc/Hz, typical. Also, the reference frequency (105 MHz) phase noise is about −110 dBc/Hz. So the maximum attainable phase noise is −110 dBc/Hz. In our case, the maximum phase noise obtained is about −100 dBc/Hz at 50 kHz offset.

7. CONCLUSION

The thesis dealt in detail the various conceptual design and realization aspects of UHF Fractional-N Frequency Synthesizers. The design incorporates the current 'State of the art' ICs. As highlighted in the chapter 'Tests and Performance Evaluation of the System', the Synthesizer meets the design specifications. Although, UHF synthesizer has been explained, the design can be used to build Synthesizers for any frequency range up to 1600 MHz using appropriate VCOs and YTOs. Qualcomm have now introduced an up graded version of the PLL Synthesizer IC Q3236 extending the frequency range to 2 GHz.

Bibliography

1. Fujitsu Prescalers and Phase-Locked Loops for VHF and UHF Frequency Synthesis, FUJITSU Microelectronics, March 1991, Edition 2.0, chapter 9.

2. Oscillators and filters subsystems, High performance Microwave products, SIVERSIMA AB, Sweden, Product Catalog.

3. Varactor designer kit for UHF and higher frequency VCOs, Semiconductor devices-RF through millimeter wave, ALPHA Manual, pp. 1-11.

4. Phase-lock VCOs for low noise UHF Synthesizers, 'Microwaves and RF' Journal, Aug 1989, pp. 99-109.

5. F. M. Gardener, 'Phase-Locked Loop Techniques', 2nd ed., John Wiley & Sons.

6. V. Manassewitsch, 'Frequency Synthesizer Theory And Design', 2nd ed., John Wiley & Sons, 1976.

7. Dr. Roland E. Best, 'Phase-Locked Loops, Theory, Design and Applications', Mc-Graw Hill, 1984.

8. Ulrich L. Rodhe, 'Microwave and Wireless Synthesizers Theory and Design', 1st edition, John Wiley and Sons, 1997.

9. VCO Designer's Handbook, MINI CIRCUITS Application Information VCO-97-1.

10. VCO Product Selection Guide licensed by Qualcomm, MICRONETICS, pp. 8-10

11. G. Chattopadhyay and T. L. Venkatasubramani, GMRT Local Oscillator System, Dec 31 1992, pp. 6-8.

APPENDICES

A. Q3216 PLL Frequency Synthesizer

B. Comparision Between IC Q3036 and IC Q3216

C. PLL Synthesizer Subsystem ICs

D. VCO HV37T-1

E. OP-27

F. Power Divider (PSC-2-1)

A.

FEATURES

- Backwards Compatible with the Q3036 PLL Chip
- MIL-STD-883 Screened Devices available
- < 0.6 W Power Consumption nominal
- On-chip +10/11 Prescaler
- Single +5V Supply Operation
- Wide Input Sensitivity Range: -10 to +5 dBm
- Programmable via 16 TTL/CMOS Compatible Parallel Inputs, 8-Bit Data Bus, or Serial Loading
- 100 MHz Phase/Frequency Detector
- High Gain Linearized Phase/ Frequency Detector [No Dead Zone]: 302 mV/Rad
- Out-of-Lock Indication
- VCO Division Ratios:
  For Serial and 8-bit Bus Mode:
    2 to 5135 up to 300 MHz or
    90 to 5135 to 1.6 GHz
  For Direct Parallel Mode:
    2 to 1295 up to 300 MHz or
    90 to 1295 to 1.6 GHz
- Reference Division Ratios of 1 to 16 in Direct Parallel Mode or 1 to 64 in Serial and 8-bit Bus Mode
- Programmability for Faster Multiplexing between Two Pre-loaded Frequencies
- Evaluation Boards Available - Q0410-1, -2

APPLICATIONS

- Lab Instrumentation
- Mobile/Airborne Communications
- Frequency Hopping Systems
- Digital Radios and Modems
- High Performance Test Equipment
- Local Oscillator Generation for VSAT, DBS, and GPS Applications RADAR and Missile Local Oscillators

GENERAL DESCRIPTION

The QUALCOMM Q3216 is a low power, single chip solution for Phase Locked Loop [PLL] Frequency Synthesizers. Requiring only a single +5V supply, the Q3216 contains all the necessary elements—with the exception of the VCO and loop filter components—to build a PLL Frequency Synthesizer operating from UHF through L-Band, and is also backwards compatible with the Q3036 I.C. as a replacable part.

The block diagram for the Q3216 is shown in figure 1. It's major components, described in detail in the following sections, are:

- high speed line receivers
- +10/11 dual modulus prescaler
- 9-bit M and 4-bit A pulse swallow counters
- 6-bit reference counter
- digital phase/frequency comparator
- out-of-lock detection circuitry
- TTL/+5V CMOS-compatible parallel, serial, or 8-bit data bus interface.

The Q3216 is fabricated using a three metalization layer, single polysilicon oxide-isolated Bi-CMOS process. Its architecture provides breakthrough prescaler performance for high frequency operation, permitting PLL designs with
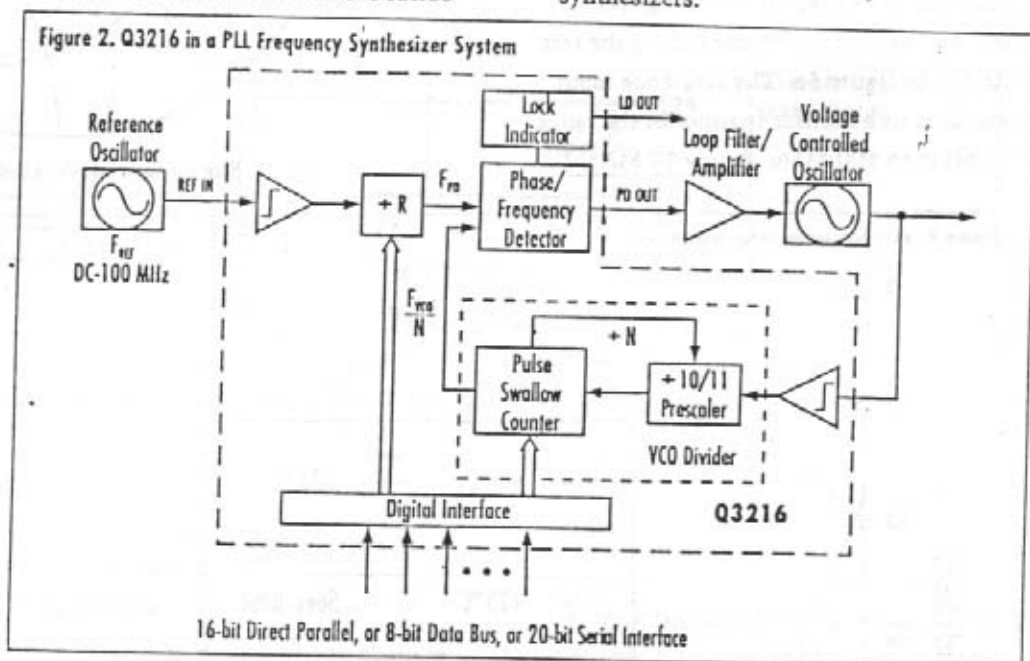
Figure 1. Q3216 Block Diagram
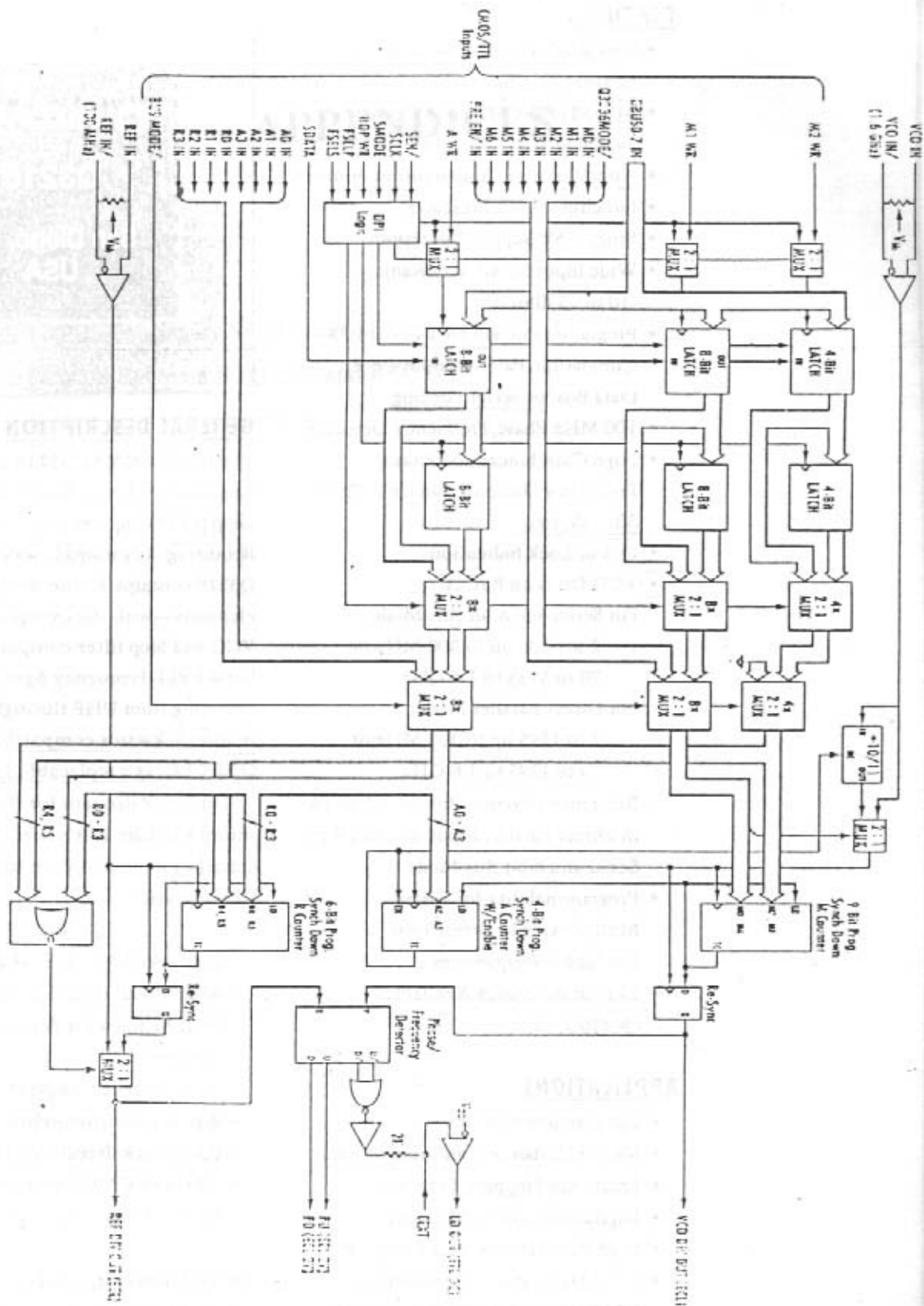
design makes possible wider loop bandwidths yielding faster settling times and lower VCO phase noise contributions.

The parallel interface permits hardwiring the Q3216 for applications without the requirement of a processor. The +10/11 prescaler can be bypassed selectively to make two divide modes possible. When the +10/11 prescaler is enabled, frequency divide ratios can be achieved from 90 to 5135, in unit steps, from DC to 1.6 GHz when operating in Serial or 8-bit Bus interface modes. Direct Parallel interface allows divide ratios

from 90 to 1295 in unit steps up to 1.6 GHz. In the non-prescaler mode, it is possible to divide inputs directly up to 300 MHz by 2 to 512, in unit steps when operating in Serial or 8-bit Bus interface and from 2 to 128 using Direct Parallel interface.

Similarly, the reference counter allows the reference input frequency to be divided directly in ratios of 1 to 64 with the Serial or 8-bit Bus interface and from 1 to 16 using Direct Parallel interface. As shown in figure 2, the Q3216's highly integrated architecture greatly simplifies the design of UHF through L-Band synthesizers.

Figure 2. Q3216 in a PLL Frequency Synthesizer System

16-bit Direct Parallel, or 8-bit Data Bus, or 20-bit Serial Interface

Q3216M-16L MILITARY VERSION DESCRIPTION

The Q3216M-16L is packaged in a 44-pin hermetically sealed ceramic leaded chip carrier (CLDCC). Device assembly is in accordance with MIL-STD-883 for Class B microcircuits. Screening and inspection of all devices is in accordance with Method 5004. Quality conformance inspection requirements of all devices are in accordance with Method 5005 of MIL-STD-883 for Class B microcircuits for Group A and Group B testing.

The maximum sustainable junction temperature for the device is +150°C. Based on testing, the Q3216M-16L can be safely rated for continuous operation in still, ambient air at 85°C. Higher ambient conditions may be possible if active cooling or other means to convect thermal energy away from the part is provided. It is the customer's responsibility to perform the necessary thermal calculations for operation above 85°C.

SOURCE

DIFFERENTIAL
INPUT MODEL
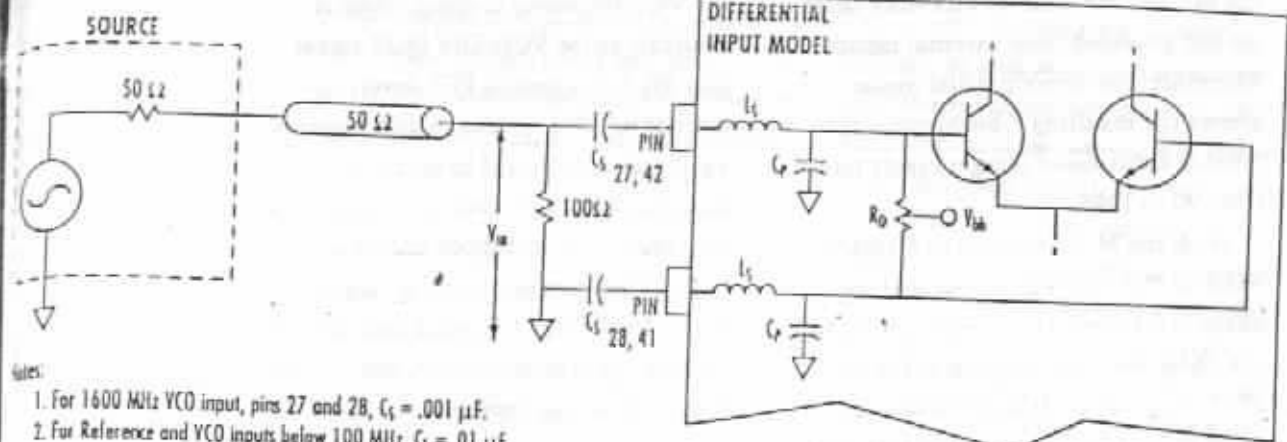
Notes:
1. For 1600 MHz VCO input, pins 27 and 28, C_s = .001 μF.
2. For Reference and VCO inputs below 100 MHz, C_s = .01 μF.

a) Single-Ended Input

SOURCE

DIFFERENTIAL
INPUT MODEL

Same as
Above
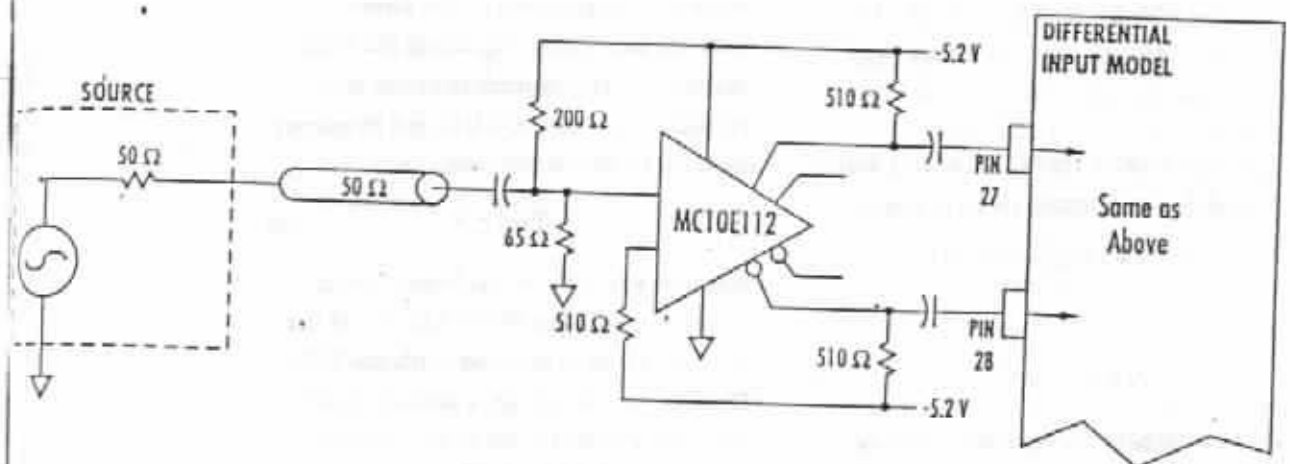
b) Differential (balanced) Input

VCO Divider

The VCO frequency division chain is used to divide the VCO 1N (pin 27) frequency, F_{VCO}, down to the phase detector frequency, F_{PD}. It operates in two modes. In the first mode, *prescaler mode* (PRE EN/ = LOW) up to 1.6 GHz, frequency division is accomplished with a pulse-swallow counter made up of the 10/11 front-end dual modulus prescaler (DMP), the 4-bit A counter and the 9-bit M counter. This mode, selected by the pulse-swallow counter, effectively implements a programmable divide-by N counter at the VCO frequency, even

though only the DMP is operating at that frequency. The total VCO input frequency division ratio, N, obtained from programming the binary M and A counters is given by:

$$N = F_{VCO}/F_{PD} = 10 \cdot (M + 1) + A,$$
$$\text{for } A \le M + 1, M \ne 0 \qquad (1)$$

When operating in the prescaler mode, programming of control inputs via the 8-Bit Bus or Serial Bus interface utilizes access to all nine M counter bits, M0 - M8, and provides continuous integer divide ratios from 90 to 5135. Programming of control inputs via the

Direct Parallel interface does not utilize the M7 and M8 counter bits since these are not provided from external inputs. Therefore, the direct parallel mode allows the resulting 7-bit M counter to provide continuous integer divide ratios from 90 to 1295.

With the M counter set to a binary value of "0", the VCO input division chain is disabled; this, in turn, will cause the phase detector outputs, PD U and PD D, to go to an ECL 2V HIGH and LOW state, respectively. However, the following non-continuous division ratios in the prescaler mode are possible:

$$N = 20, 21, 22, \qquad 60...66,$$
$$30, 31, 32, 33, \qquad 70...77,$$
$$40...44, \qquad 80...88.$$
$$50...55,$$

Given a value for N, the binary values, M and A, are determined as follows:

$$M = \text{integer } [N/10] - 1 \qquad (2)$$

and

$$A = N - 10 \cdot (M + 1) \qquad (3)$$

In the alternate mode, *non-prescaler mode*, (PRE EN/=HIGH), the prescaler is bypassed so that the VCO input frequency is divided directly by the M counter. The counter operates at frequencies up to 300 MHz. In this mode, frequency division ratio is determined by

$$(F_{VCO}/F_{PD}) = M + 1, \quad M \neq 0 \qquad (4)$$

where M = 1,...,511 is the binary value programmed to the M0 - M8 inputs of the M counter and the values programmed to the A0 - A3 inputs of the A counter are ignored. As in the previous mode, programming via the 8-Bit Bus or Serial Bus interface will allow divide ratios of 2 to 512, while programming via the Direct Parallel interface will allow divide

ratios of 2 to 128. Finally, the output of the VCO frequency division chain is available as the VCO DIV OUT signal (pin 30). It is a pseudo ECL-level emitter follower output, which requires a pull down resistor (510 ohms is recommended) and directly interfaces to ECL logic. It is referenced to +5V and GND. The waveform is a digital pulse with a frequency of F_{PD} and duty cycle of 10/N in the *prescaler mode*, and 1/N in the *non-prescaler mode*.

Reference Divider

The reference frequency division chain is used to divide the REF IN (pin 42) frequency, F_{REF}, down to the phase detector frequency, F_{PD}, using the 6-bit R counter. The counter operates at frequencies up to 100 MHz and frequency division ratio is determined by

$$(F_{REF}/F_{PD}) = R + 1 \qquad (5)$$

where R = 0,..., 63 is the binary value programmed to the R0 - R5 inputs of the R counter. As in the case with the VCO Divider, programming of control inputs via the 8-Bit Bus or Serial Bus interface utilizes access to all six R counter bits and permits divide ratios of 1 to 64. Programming of control inputs via the Direct Parallel interface does not utilize the R4 and R5 counter bits since these are not provided from external inputs. Therefore, this allows the resulting 4-bit R counter to provide divide ratios from 1 to 16. The divided result is available at REF DIV OUT (pin 39), and is similar to VCO DIV OUT.

Digital Phase/Frequency Detector

The Q3216 has a digital Phase/Frequency detector capable up to 100 MHz operation and a phase detector gain constant of 302 mV/Rad. This high gain suppresses the active loop filter noise floor.

Additionally, the high phase detector gain permits wider loop bandwidths, which yield faster settling times and lower VCO phase noise contributions. The outputs of the VCO and reference frequency divider chains are connected to an internal digital phase/frequency detector (PFD). The PFD is triggered by the rising edges of these signals and has three outputs. Refer to figure 6.

Two of these outputs make up a double-ended PFD output. The two signals corresponding to this output are PD U OUT (Phase Detector pulse Up) and PD D OUT (Phase Detector pulse Down). The first output, PD U OUT (pin 36), pulses HIGH approximately 1.9 V when the divided VCO lags behind the divided reference in phase or frequency. The pulse begins at the rising edge of the REF DIV input and is terminated on the rising edge of the divided VCO signal, VCO DIV. Conversely, PD D OUT (pin 37) pulses HIGH in the same manner when the divided VCO leads the divided reference in phase or frequency. The pulse begins at the rising edge of the VCO DIV input and terminates on the rising edge of the divided reference signal, REF DIV. Thus, the phase error is encoded as a pulse-width modulated waveform, whose DC average is proportional to its duty cycle which equals the phase error. In typical differential phase detector output applications, PD U OUT is subtracted from PD D OUT in a differential OP-AMP active loop integrator filter, as shown in Figure 13.

Therefore, it is only necessary that the differential output power between the two phase detector outputs, PU and PD, be linearly proportional to the phase difference between the VCO DIV and REF DIV input rising edges. A residual pulse width, t_{RP} is also added onto both phase detector outputs after the rising edge of

the lagging input to mitigate the usual "dead zone" nonlinearity. This works as follows: as long as this residual pulse is kept above a minimum duration, then the phase detector outputs will always reach full amplitude all the way down to zero phase difference, thereby maintaining output power which stays linearly proportionate to the time skew between the phase detector inputs.

The third output, LD OUT (pin 43), is used for an out-of-lock indication. It pulses LOW when either PD U OUT or PD D OUT is pulsing HIGH. Lock detection is performed by NORing the phase detector PD U and PD D output signals. The result is a signal which pulses for a duration equal to the time skew between the VCO DIV and REF DIV rising edges. These pulses are integrated with an internal 2K series resistor, and a shunt capacitor connected to the CEXT output (pin 34). When the PLL is out of lock and there is pulsing on the PFD outputs sufficient to bring the voltage on CEXT above an internal comparator threshold, then the open collector output, LD OUT, will turn on, sinking up to 25mA. LD OUT can be wired to an open-collector fault bus or used to drive an LED, indicating an out-of-lock condition. The Phase/Frequency Detector waveforms are shown in Figure 6.

It has been observed where certain conditions produce electrical overstress (EOS) to pin 43 and damage the LD OUT. Such an occurance would typically be the result of capacitive discharge with insufficient current limiting resistance with respect to LD OUT and how out-of-lock conditions are indicated within a particular system design. Careful attention to proper current limiting in this regard will eliminate any EOS potential.

10

BUSMODE/ INPUT	SMODE INPUT	DPI MODE
LOW	LOW	8-BIT BUS
LOW	HIGH	SERIAL BUS
HIGH	X	DIRECT PARALLEL INPUT

Digital Processor Interface (DPI) Modes

The Q3216 can be programmed using one of three operating modes including a *Direct Parallel Input Mode, 8-Bit Bus Mode,* or *Serial Bus Mode.* All of the DPI data and control inputs operate at either static or low speeds relative to the rest of the device and are to be compatible with CMOS/TTL levels, whose characteristics are described in Table 6. The DPI outputs consist of twenty counter programming bits, M0 - M8, A0 - A3, R0 - R5 as well as the prescaler enable control input, PRE EN/. An *Enhanced Operation Mode* option for the 8-bit bus and serial bus modes is provided to enable access to all of these counter programming bits and is described below. A *Frequency Multiplexing Mode* option for the 8-bit bus and serial bus modes is also provided to allow rapid toggling between stored programmed frequencies and is described beneath the following sections of these two respective interface modes.

The interface modes are selected in the following manner: When the external DPI control signal, BUSMODE/(pin 22), is HIGH, the DPI is in the direct parallel mode. When the BUSMODE/ input is LOW, the DPI is in either the 8-bit bus or serial bus mode, depending on the HIGH or LOW state, respectively, of the SMODE input (pin 21). Serial mode addressing is accomplished in a standard fashion using three signals: SDATA, SCLK, and SEN/. DPI mode selection is summarized in Table 1. In order to

consolidate the utility of as many of the package pins as possible, most of the CMOS/TTL inputs are multi-functional as denoted in Figure 10; this is possible because of some of the mutual exclusivity of the DPI modes and these inputs. Internally, these differing control signal inputs are logically OR'ed to avoid contention.

Enhanced Operation: "Q3036 Mode"

An enhanced operation mode control signal, Q3036 MODE/(pin 44), is referenced after QUALCOMM's original single-chip PLL, the Q3036, and allows the Q3216 to maintain identical DPI modes and divider ratios as the Q3036 for backwards compatibility, or be set for expanded divider capability and DPI operation. When the Q3036 MODE/ input is HIGH, this enables access to all twenty counter programming bits for operation only in the 8-bit bus or serial bus interface mode if the additional M7, M8 or R4, R5 counter bits are required for larger division ratios. This allows for programmability to the full range of divider ratios as described in the *Functional Overview* section under the *VCO Divider* and *Reference Divider* subsections. When the Q3036 MODE/ input is LOW, all of the counter programming bits except M7, M8, R4, and R5 are available in all three interface modes with a corresponding reduction in the available range of divider ratios as also discussed in the above-mentioned section. When operating with Q3036

II

MODE/ set LOW, the M7, M8, R4, and R5 inputs are set internally to the LOW state. As initially mentioned, this allows any previously designed synthesizer circuits using the Q3036 to be directly replaced with the Q3216 device.

All external CMOS/TTL inputs will register as a HIGH or LOW state when left floating, according to the LOW or HIGH state of the Q3036 MODE/ input, respectively.

8-bit Bus Mode

With the BUSMODE/ input LOW and the SMODE input LOW, the 8-bit bus mode is selected and the external DBUS0-7 inputs are latched into one of the three primary registers, with the A WR, M1 WR, or M2 WR external control inputs according to the timing requirements shown in Figure 8. In the 8-bit bus mode, the interface is double-buffered consisting of a set of primary registers and secondary

Table 2. 8-bit Bus Mode Primary Register Map

EXTERNAL INPUT	INTERNAL PRIMARY REGISTER MAPPING		
	A WR RISING EDGE	M1 WR RISING EDGE	M2 WR RISING EDGE
DBUS0	A0	M0	M7
DBUS1	A1	M1	M8
DBUS2	A2	M2	R4
DBUS3	A3	M3	R5
DBUS4	R0	M4	N/A
DBUS5	R1	M5	N/A
DBUS6	R2	M6	N/A
DBUS7	R3	PRE EN/	N/A

Direct Parallel Input Mode

With the BUSMODE/ input set HIGH and the Q3036 MODE/ input set LOW, all of the DPI outputs except M7, M8, R4, and R5 are taken directly from external inputs, as listed in the pin assignment/ descriptions, Table 8J. As can be seen from the Q3216 Block Diagram [Figure 1], BUSMODE/ is really the select input to a row of 20 x 2:1 MUXes, one each of whose inputs are connected to the external inputs, with the exception of the M7, M8, R4, and R5 signals. This mode allows the device to be hardwired for fixed frequency phase-locked oscillators as well as parallel-loaded fast frequency hopping applications.

registers. The primary registers are programmed in parallel fashion without affecting the inputs to the counters. The contents from the primary registers are loaded into the secondary registers on the rising edge of the HOP WR input and are then immediately available to the counters and prescaler as DPI outputs. The DPI outputs are simply the secondary register outputs. A mapping of the DBUS0-7 inputs to the primary registers for all twenty counter programming bits is shown in Table 2, and listed in the pin assignment/ descriptions, Table 8H.

3. Serial Mode Data Programming Sequence

BIT NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SDATA INPUT	R5	R4	M8	M7	PRE EN/	M6	M5	M4	M3	M2	M1	M0	R3	R2	R1	R0	A3	A2	A1	A0

With the BUSMODE/ input LOW and the SMODE input HIGH, the serial bus mode is selected and data is shifted serially into the SDATA input on the falling edge of the SCLK input, while the shift enable control input, SEN/, is LOW. In the same manner as the 8-bit bus mode, the interface is double-buffered consisting of a set of primary registers and secondary registers. The data for all twenty counter programming bits is shifted into the primary registers in accordance to the sequence shown in Table 3, starting with R5 and ending with A0. The contents from the primary registers are shifted into the secondary registers on the rising edge of both the SEN/ input and HOP WR input asserted together according to the timing requirements shown in Figure 9, and are then immediately available to the , counters and prescaler as DPI outputs. A list of the respective serial bus mode pin assignment/descriptions is shown in Table 8I.

8-bit Bus or Serial Bus Frequency Multiplexing: "Ping-Pong" Mode

The Ping-Pong mode is a subset of both the 8-bit bus and serial bus interface modes which enables the Q3216 to be multiplexed between two pre-loaded frequencies for applications involving random frequency hopping, low-data-rate FSK modulation, or half-duplex transceiving operation using a single synthesizer. ATE system environments requiring multiple frequencies also use fast switching synthesizers to greatly increase system throughput, and they are increasingly being used as the reference oscillator in commercial Magnetic Resonance Imaging systems. In either interface mode, this is carried out by toggling between two different VCO division ratios in the primary and

programming bits in the primary registers may be updated while the ones in the secondary registers are controlling the programmable divider and vice versa.

The so-called "ping-pong" frequency selection is controlled by the external input signal, FSELP in the 8-bit bus mode, and FSELS in the serial mode.

As noted in the *8-Bit Bus Mode* subsection, after the DBUS0-7 inputs are latched into the three primary registers, they are then only loaded into the secondary registers after the HOP WR input is asserted. This means that the contents of the primary registers can be updated with a new frequency word while the secondary registers retain control of the DPI outputs with the previously loaded data. An external frequency multiplexing control input, FSELP [pin 18], enables the device to be toggled between these two pre-loaded frequencies as noted in the pin assignment/descriptions, Table 8H. When the FSELP input is HIGH, the synthesizer output frequency is obtained from the frequency word stored in the primary registers, and when the FSELP input is LOW, the output frequency is obtained from the frequency word stored in the secondary registers. The DPI outputs are simply the multiplexed output of either the primary or secondary register outputs selected by the control signal FSELP.

As noted in the *Serial Bus Mode* subsection, after the data for all twenty counter programming bits is shifted into the primary registers, they are then only loaded into the secondary registers after the SEN/ and HOP WR inputs are asserted. In the same manner as in the 8-bit bus mode, an external frequency multiplexing control input, FSELS [pin 16], enables the device to be toggled

between these two pre-loaded frequencies as noted in the pin assignment/ descriptions, Table 8I. The synthesizer output frequency is simply the multiplexed output of either the primary or secondary register outputs selected by the HIGH or LOW state, respectively, of the control signal FSELS.

For Q3216 implementations using the Ping-Pong mode for FSK modulation of the synthesizer's output, the data rate limitation of the loop will be a function of the natural frequency, ω_n, since a second-order PLL is able to track for phase and frequency modulations of the reference signal as long as the modulation frequencies remain within an angular frequency band roughly between zero and ω_n. When using the Ping-Pong mode for a frequency hopping synthesizer, or as a transmit and receive synthesizer for half-duplex operation, the synthesizer's switching speed performance, otherwise know as it's settling time characteristics, will essentially govern the achievable switching or hop rate, although the 20-bit load period for the respective interface mode used should also be taken into account.

TECHNICAL SPECIFICATIONS

Tables 1 through 4 contain technical specifications fot the Q3216 PLL. Figures 6 and 7 contain timing specifications for the Q3216 PLL.

Table 4. Absolute Maximum Ratings: Q3216I-16N & Q3216M-16L

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	T_{STO}	-55	+150	°C	1
Junction Temperature	T_J	-55	+150	°C	1
Supply Voltage (relative to V_{EE})	V_{CC}	–	+7.0	V	1
Voltage on any Non Differential Input Pin (relative to V_{EE})	V_{IN}	-0.5	V_{CC} + 0.5	V	1
Continuous Output Current	I_{OUT}	25	–	mA	1, 2
Surge Output Current	I_{OUT}	200	–	mA	1, 2
AC Coupled Voltage on any Differential Input	V_{IN}	–	1275	mV_{PP}	1
Latchup Insensitivity	I_{TRIG}	± 200	–	mA	1, 3
ESD Protection	V_{ESD}	± 2000	–	V	1, 4

Notes:

1. Stresses above those listed in this table "Absolute Maximum Ratings" may cause permanent and functional damage to the Q3216 Device. This is a stress rating only. Functional operation of the Q3216 Device at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect Q3216 Device reliability.
2. ECL and ECL 2V outputs terminated with 510 Ω to V_{EE}.
3. Method meets the intent of JEDEC STD 17 Publication. This is the maximum allowable current flow through the input and output protection diodes.
4. Method meets the intent of MIL-STD-883, Method 3015.

Table 5. Operating Conditions

PARAMETER	SYMBOL	Q3216I-16N			Q3216M-16L			UNITS	NOTE
		MIN	TYPICAL	MAX	MIN	TYPICAL	MAX		
Operating Ambient Temperature	T_A	-40		+85	-55		+85	°C	
Operating Voltage (Relative to V_{EE})	V_{CC}	+4.5		+5.5	+4.5		+5.5	V	
Junction to Case Resistance	θ_K		19					°C/W	1
Junction to Ambient Resistance	θ_{JA}		51			51		°C/W	2

Notes:

1. θ_{JC} measured with package held against an "infinite" heatsink test condition.
2. θ_{JA} measured in still-air, room temperature test condition.

Table 6. DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
ECL HIGH Output Voltage	V_{OH}	$V_{CC} - 1150$	$V_{CC} - 850$	mV	1
ECL LOW Output Voltage	V_{OL}	$V_{CC} - 2030$	$V_{CC} - 1620$	mV	1
ECL 2V HIGH Output Voltage	V_{OH}	$V_{CC} - 1150$	$V_{CC} - 700$	mV	1
ECL 2V LOW Output Voltage	V_{OL}	$V_{CC} - 3250$	$V_{CC} - 2610$	mV	1
CEXT HIGH Output Voltage	V_{OH}	$V_{CC} - 1150$	$V_{CC} - 700$	mV	2
CEXT LOW Output Voltage	V_{OL}	$V_{CC} - 2100$	$V_{CC} - 1500$	mV	2
Open Collector LOW Output Voltage	V_{OL}	—	500	mV	3
Open Collector HIGH Output Current	I_{OL}	-2	+2	μA	4
CMOS/TTL HIGH Input Current	TTL I_{IH}	+225	+400	μA	5
CMOS/TTL LOW Input Current	TTL I_{IL}	-100	+1	μA	6
CMOS/TTL HIGH Input Voltage	V_{IH}	2.0	—	V	7
CMOS/TTL LOW Input Voltage	V_{IL}	—	0.800	V	7
Q3036 MODE/ HIGH Input Current	Q3036/ I_{IH}	+400	+800	μA	8
Q3036 MODE/ LOW Input Current	Q3036/ I_{IL}	-400	-200	μA	9
Supply Current ($V_{CC} - V_{EE}$)	I_{CC}	—	160	mA	10

Notes:

1. Outputs terminated through 510 Ω to V_{EE}.
2. Outputs measured directly with no termination resistance.
3. While Open Collector output is sinking 20 mA.
4. $V_{CC}^* = +5.5V$, $V_{OUT} = V_{CC} - 10$ mV.
5. $V_{CC}^* = +5.5V$, $V_{IN} = V_{CC} - 10$ mV, Input Q3036 MODE/ = V_{EE}^*.
6. $V_{CC}^* = +5.5V$, $V_{IN} = V_{EE} + 10$ mV, Input Q3036 MODE/ = V_{EE}^*.
7. All CMOS/TTL inputs will register as a HIGH or LOW state when left floating, according to the LOW or HIGH state of the Q3036 MODE/ input, respectively.
8. $V_{CC}^* = +5.5V$, $V_{IN} = V_{CC} - 10$ mV.
9. $V_{CC}^* = +5.5V$, $V_{IN} = V_{EE} + 10$ mV.
10. $V_{CC}^* = +5.5V$ (ECL, ECL 2V Outputs terminated through 510 Ω to V_{EE}.
*. All V_{CC} values relative to V_{EE}.

Figure 6. Phase/Frequency Detector Waveforms
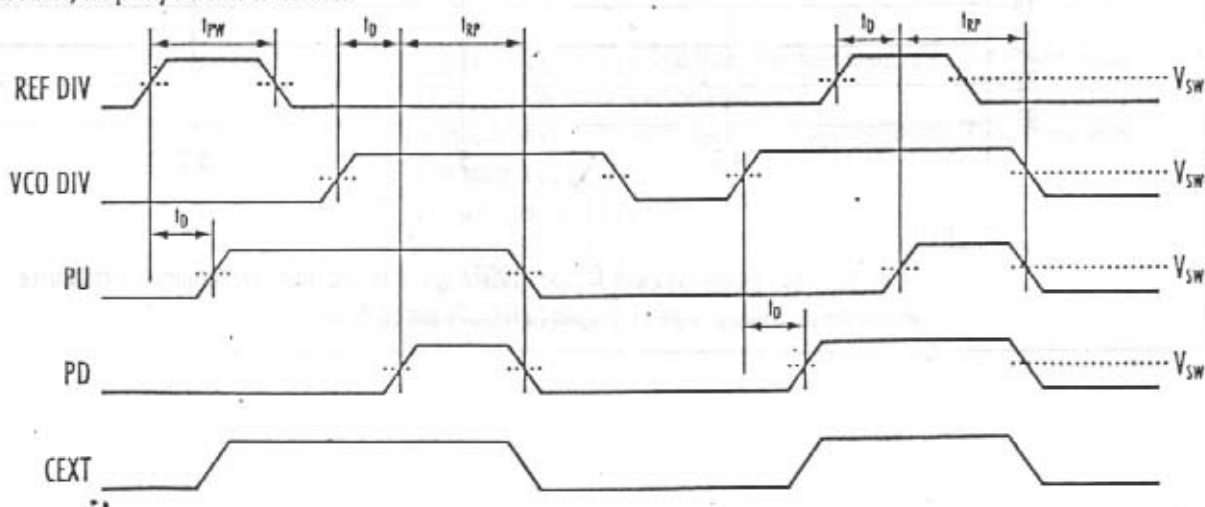
Note: V_{SW} is the CML logic voltage located at the 50% level between V_{OH} and V_{OL}.

Figure 7. Typical I_cc (Static) vs. V_cc

I_{cc} vs. V_{cc}

(graph with y-axis labeled "I_cc Static [mA]" ranging from 91 to 122, x-axis labeled "V_cc" ranging from 4 to 6)

@ + 85° C

@ + 25° C

@ - 40° C
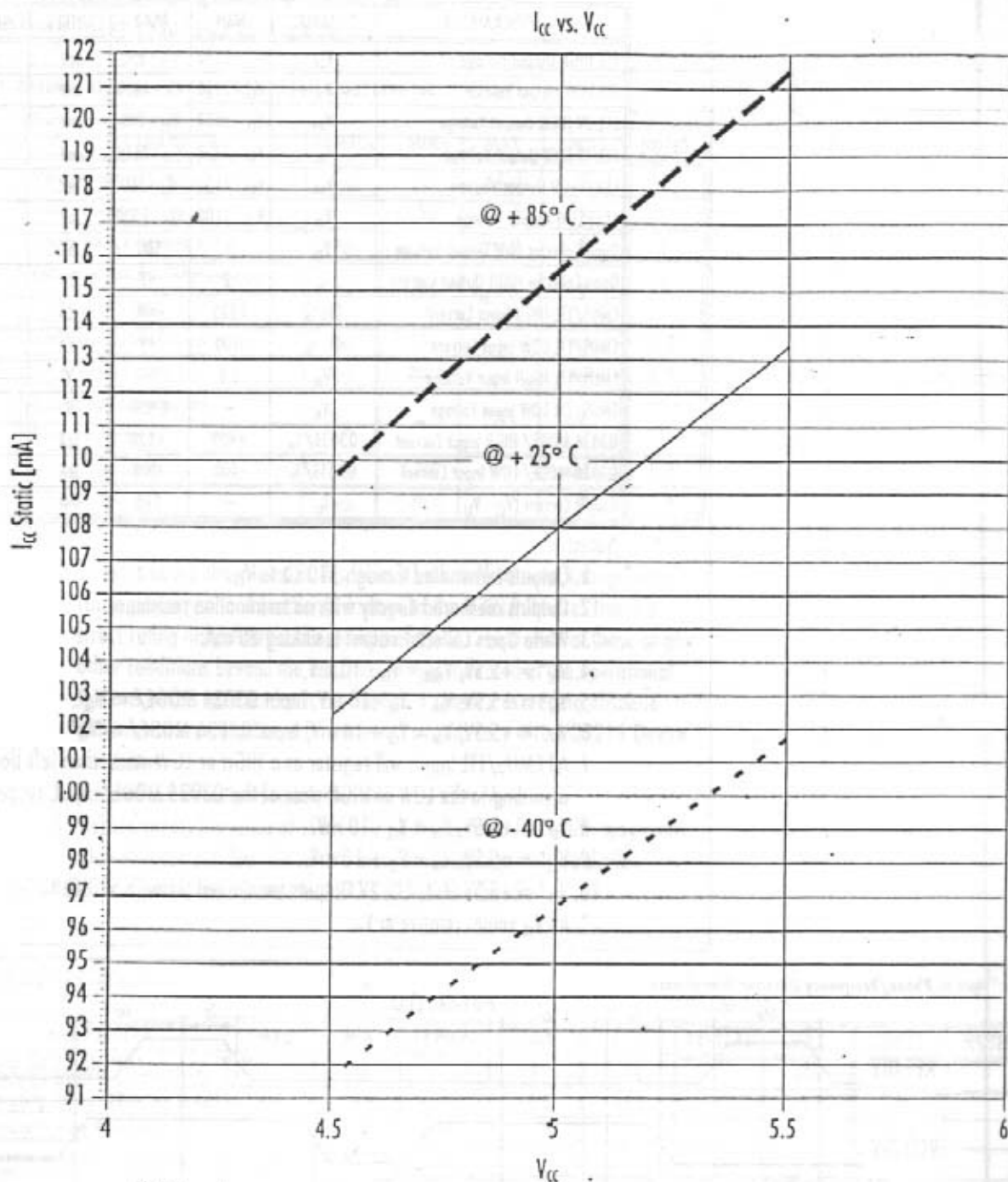
Note:

All measurements conducted with Q3036 MODE/ (pin 44) tied HIGH, no termination resistance on any outputs, and all inputs left open (internally pulled down).

Table 7. AC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
VCO IN, REF IN Differential Inputs Sinusoidal or Square Wave Input Sensitivity Input VSWR	V_{IN}	200 (-10)	1130 (+5) 3.6:1	mVpp dBm	1
VCO IN Frequency Range	F_{VCO}	20	1600	MHz	2,3
REF IN Frequency Range	F_{REF}	20	100	MHz	2,3
10/11 Prescaler Frequency	F_P	20	1600	MHz	2,3
M Counter Frequency	F_M	20	300	MHz	2,3
A Counter Frequency	F_A	20	160	MHz	2,3
R Counter Frequency	F_R	20	100	MHz	2,3
Phase Detector input pulse width, REF DIV, VCO DIV	t_{PW}	4	—	ns	6
Phase Detector output residual pulse width	t_{RP}	4	—	ns	5,6
Phase Detector propagation delay	t_D	2	—	ns	5,6
DBUS0-7 Valid to M1 WR, M2 WR, A WR rising	t_{SU}	50	—	ns	4
DBUS0-7 Valid after M1 WR, M2 WR, A WR rising	t_H	50	—	ns	4
SDATA Valid to SCLK falling	t_{SU}	50	—	ns	4
SDATA Valid after SCLK falling	t_H	50	—	ns	4
SEN/ setup to SCLK falling	t_{SU}	50	—	ns	4
SEN/ hold after SCLK falling	t_H	50	—	ns	4
SCLK falling, M1 WR, M2 WR, A WR rising to HOP WR, SEN/ rising	t_{WH}	50	—	ns	4
Pulse width SCLK, M1 WR, M2 WR, A WR, HOP WR, and SEN/	t_{PW}	50	—	ns	4
HOP WR falling to SCLK falling, M1 WR, M2 WR, A WR rising	t_{HW}	0	—	ns	4
CMOS/TTL Input Capacitance	C_{IN}	—	2	pF	—

Notes:

1. For VCO IN frequencies < 100 MHz, minimum sinusoidal input power applies to non-prescaler mode operation only.
2. For square wave inputs with edge rates of at least 200mV/25ns, there shall be no lower frequency limit.
3. Per input loading of Figure 5a.
4. Timing is referenced at the CMOS/TTL input logic voltage switching threshold.
5. Outputs PD D, PD U loaded per Figure 21.
6. Timing is referenced at the 50% level between V_{OH} and V_{OL}.

• Figure 8. Bus Mode Interface AC Timing Waveforms
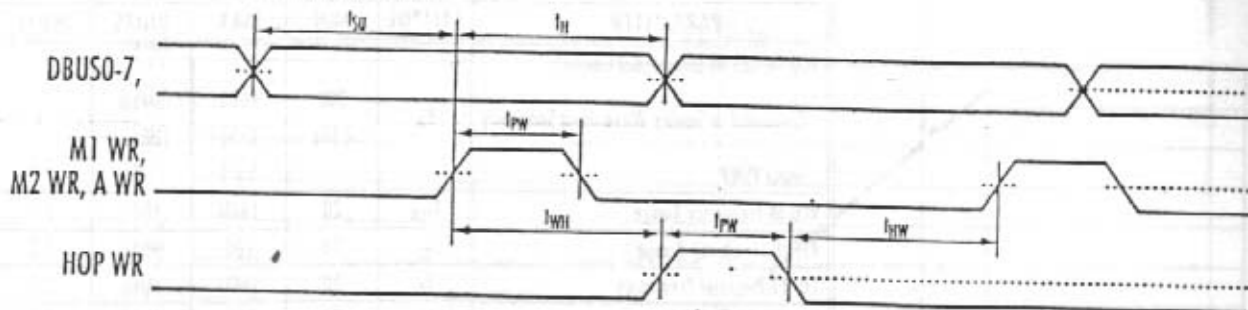
Note: V_{SW} is the CMOS/TTL INPUT logic voltage switching threshold.

Figure 9. Serial Mode Interface AC Timing Waveforms

Note: V_{SW} is the CMOS/TTL INPUT logic voltage switching threshold.

Figure 10 provides the pin configuration of the Q3216 PLL package and tables 8A-J provide summaries of the input/output signal pin assignments.

Figure 10. Q3216 44-pin Configuration
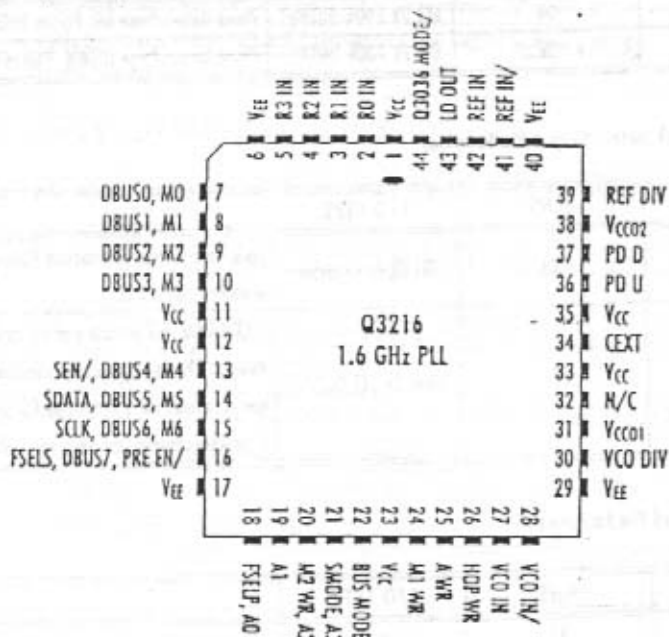
8A. Differential Line Receiver Input Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
VCO IN	27	Differential INPUT	VCO driven differential input.
VCO IN/	28	Differential INPUT	VCO driven complimentary differential input.
REF IN	42	Differential INPUT	Reference driven differential input.
REF IN/	41	Differential INPUT	Reference driven complimentary differential input.

8B. Enhanced Operation Mode Control Input Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
Q3036 MODE/	44	V_{CC}/V_{EE} INPUT	Q3036 MODE. When configured LOW (V_{EE}), internal M-Counter Bits [8:7] and R-Counter Bits [5:4] set to logic 0. External CMOS/TTL inputs "pulled up" internally through > 50 kΩ resistors. When configured HIGH (V_{CC}), internal M-Counter Bits [8:7] and R-Counter bits [5:4] programmable in serial or 8-bit bus mode. External CMOS/TTL inputs "pulled down" internally through > 50 kΩ resistors.

8C. Divider Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
VCO DIV	30	ECL 100 k OUTPUT	VCO Divided Output. Provides Output with frequency equal to VCO IN frequency divided by VCO IN division ratio.
REF DIV	39	ECL 100 k OUTPUT	Reference Divided Output. Provides Output with frequency equal to REF IN frequency divided by REF IN division ratio.

Table 8D. Phase Detector Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
PD U	36	ECL 2V 100k OUTPUT	Phase Detect Pulse UP. Pulses HIGH when VCO DIV lags REF DIV.
PD D	37	ECL 2V 100k OUTPUT	Phase Detect Pulse DOWN. Pulses HIGH when VCO DIV leads REF DIV.

Table 8E. Phase Lock Detect Output Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
LD OUT	43	TTL Open Collector	Lock Detect. High impedance during phase locked operation, Low impedance during phase unlocked operation.
CEXT	34	Series 2k ECL OUTPUT	C EXTERNAL. OR'd output of PD and PU provided by 100k ECL emitter follower terminated through 2k, on-chip, series resistance. External attachment of 0.1 μF capacitor acts to low pass filter OR'd output of PD and PU signals. Output drives inverting differential input of on-chip comparator used for switching LD OUT.

Table 8F. Unconnected Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
—	32	N/C	Unconnected Pin.

Table 8G. Voltage Supply Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
V_{CC}	1, 11, 12, 23, 33, 35	Power	Core circuitry V_{CC} POWER SUPPLY.
V_{CCO1}	31	Power	Output drivers V_{CC} POWER SUPPLY for VCO DIV OUT and CEXT.
V_{CCO2}	38	Power	Output drivers V_{CC} POWER SUPPLY for PD U OUT, PD D OUT, and REF DIV OUT.
V_{EE}	6, 17, 29, 40	Power	V_{EE} POWER SUPPLY.

Digital Processor Interface (DPI) 8-Bit Bus Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
BUSMODE/	22	CMOS/TTL INPUT	BUSMODE. Used with SMODE to select one of three possible DPI modes of operation.
SMODE	21	CMOS/TTL INPUT	SMODE. Selects SERIAL BUS MODE (BUSMODE/ Low, SMODE high) or 8-BIT BUS MODE (BUSMODE/ Low, SMODE Low)
DBUS7-DBUS0	16 (MSB), 15, 14, 13, 10, 9, 8, 7(LSB)	CMOS/TTL INPUT	DATA BUS bit 7 (MSB) - DATA BUS bit 0 (LSB)
M1 WR	24	CMOS/TTL INPUT	M1 WRITE. Rising edge active. Latches DATA BUS bits [7:0] (PRE EN/ and M[6:0]) to primary register.
M2 WR	20	CMOS/TTL INPUT	M2 WRITE. Rising edge active. Latches DATA BUS bits [3:0] (R[5:4] and M[8:7]) to primary register.
A WR	25	CMOS/TTL INPUT	A WRITE. Rising edge active. Latches DATA BUS bits [7:0] (R[3:0] and A[3:0]) to primary register.
HOP WR	26	CMOS/TTL INPUT	HOP WRITE. Rising edge active. Latches primary register data previously latched with M1 WR, M2 WR, and A WR, to secondary register.
FSELP	18	CMOS/TTL INPUT	Provides option of selecting DPI information stored in primary registers (FSELP = "1") or secondary registers (FSELP = "0").

Digital Processor Interface (DPI) Serial Bus Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
SDATA	14	CMOS/TTL INPUT	SERIAL DATA. Data is shifted serially into input SDATA on falling edge of SCLK signal.
SEN/	13	CMOS/TTL INPUT	SHIFT ENABLE. LOW for SERIAL DATA loading with input SDATA. SEN/ and HOP WR must be asserted HIGH when loading SERIAL DATA to secondary registers.
SCLK	15	CMOS/TTL INPUT	SHIFT CLOCK. Falling edge active. Shifts serial data into input SDATA with each falling edge (SEN/ = LOW).
HOP WR	26	CMOS/TTL INPUT	HOP WRITE. Rising edge active. Latches primary registers SERIAL DATA into secondary registers. SEN/ and HOP WR must be asserted HIGH when loading SERIAL DATA to secondary registers.
FSELS	16	CMOS/TTL INPUT	Provides option of selecting DPI information stored in primary registers (FSELS = "1") or secondary registers (FSELS = "0")

Digital Processor Interface (DPI) Direct Parallel Input Mode Pin Functions

SYMBOL	PINS	I/O TYPE	FUNCTION
M(6:0)	15 (MSB), 14, 13, 10, 9, 8, 7 (LSB)	CMOS/TTL INPUT	M-COUNTER BITS 6(MSB) - 0(LSB).
A(3:0)	21 (MSB), 20, 19, 18 (LSB)	CMOS/TTL INPUT	A-COUNTER BITS 3(MSB) - 0(LSB).
R(3:0)	5 (MSB), 4, 3, 2 (LSB)	CMOS/TTL INPUT	R-COUNTER BITS 3(MSB) - 0(LSB).
PRE EN/	16	CMOS/TTL INPUT	PRESCALER ENABLE. Enables Divide by 10/11 Prescaler (Active LOW).

Q3216
LOW POWER PLL
FREQUENCY SYNTHESIZER
TECHNICAL DATA SHEET
SUBJECT TO CHANGE WITHOUT NOTICE

22

QUALCOMM Incorporated, VLSI Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA,

E-mail: vlsi-products@qualcomm.com
Telephone: (619) 658-5005, Fax: (619) 658-1556

B. COMPARISON OF IC Q3036 AND IC3216

Parameters	Q3036	Q3216
Input Sensitivity Range:	-10 to +15 dBm	-10 to +5 dBm
Available Programmable Inputs (TTL/CMOS)	8-Bit parallel inputs	Parallel inputs, 8-Bit data bus, serial input
Maximum Phase Comparison Frequency Of Phase/Frequency Detector	50 MHz	100 MHz
Phase/Frequency Detector Gain	286 mV/Rad	302 mV/Rad (No Dead Zone)
VCO Division Ratios	2 to 128 upto 300 MHz 110 to 1285 upto 1.6 GHz	For serial and 8-Bit Bus Mode: 2 to 5135 upto 300 MHz 90 to 5136 to 1.6 GHz For Direct Parallel Mode: 2 to 1295 upto 300 MHz 90 to 1295 to 1.6 GHz
Reference Division Ratios	1 to 16	Serial and 8-Bit Bus Mode:1 to 64 Direct Parallel Mode:1 to 16
Pulse Swallow Counter	7-Bit M 4-Bit A	9-Bit M 4-Bit A
Reference Counter	4-Bit	6-Bit

Product Preview

- 500 ps Max. Propagation Delay
- V_{BB} Supply Output
- Dedicated V_{CCO} Pin for Each Receiver

The MC10E·100E116 is a quint differential line receiver with emitter-follower outputs. An internally generated reference supply (V_{BB}) is available for single-ended reception

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated V_{CCO} supply lead, providing optimum symmetry and stability.

The receiver design features clamp circuitry to cause a defined state if both the inverting and non-inverting inputs are left open; in this case the O output goes LOW, while the $\overline{O}$ output goes HIGH.

If both inverting and non-inverting inputs are at equal potential, the receiver does not go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW.

The device V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

The E116 features input pull-down resistors, as does the rest of the ECLinPS family.

MC10E116
MC100E116

QUINT DIFFERENTIAL
LINE RECEIVER

LOGIC SYMBOL

PINOUT: 28-LEAD PLCC (TOP VIEW)
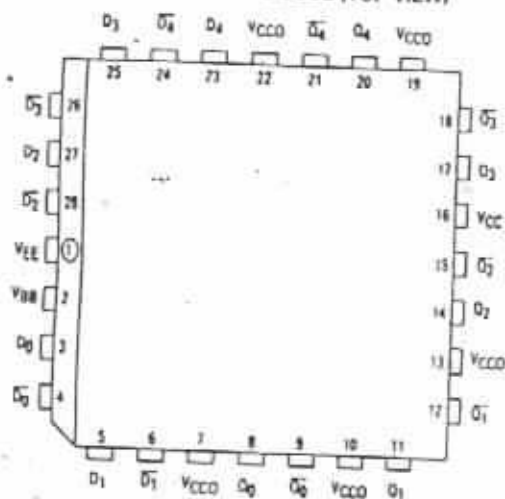
PIN NAMES

Pin	Function
D_0, $\overline{D_0}$–D_4, $\overline{D_4}$	Differential Input Pairs
O_0, $\overline{O_0}$–O_4, $\overline{O_4}$	Differential Output Pairs
V_{BB}	Reference Voltage Output

DC CHARACTERISTICS V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		29	35		29	35		29	35		
	100E		29	35		29	35		33	40		

AC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D	150		500	150		500	150		500	ps	
V_{PP}	[1]Minimum Input Swing	150			150			150			mV	
V_{CMR}	[2]Common Mode Range	-2.0		-0.6	-2.0		-0.6	-2.0		-0.6	V	

1. V_{PP} is used here as an AC spec., rather than just a measure of DC sensitivity. V_{PP} min. defines the differential input swing below which AC performance starts to significantly degrade.

2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation and performance are obtained when the most positive side of the differential input signal is within the V_{CMR} range, and the input swing is greater than V_{PP}.

Advance Information

- 800 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)

MC10E131
MC100E131

4-BIT
D FLIP-FLOP

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

PINOUT: 28-LEAD PLCC (TOP VIEW)
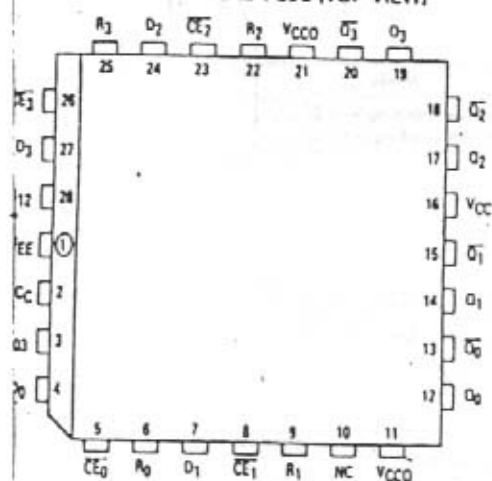
LOGIC SYMBOL

NAMES

Pin	Function
D_0–D_3	Data Inputs
$\overline{CE}_0$–$\overline{CE}_3$	Clock Enables (Individual)
R_0–R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (paired)
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Inverting Outputs

DC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max), V_{CC} = V_{CCO} = GND

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current										μA	
	C_C			350			350			350		
	S			450			450			450		
	R			300			300			300		
	$\overline{CE}$			300			300			300		
	D			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		58	70		58	70		58	70		
	100E		58	70		58	70		67	81		

AC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max. Toggle Frequency	800	1000		800	1000		800	1000		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	$\overline{CE}$	275		700	275		700	275		700		
	C_C	325		775	325		775	325		775		
	R	275		725	275		725	275		725		
	S	275		725	275		725	275		725		
t_s	Setup Time, D	350			350			350			ps	
t_h	Hold Time, D	350			350			350			ps	

FUNCTION TABLE

Pin	State	Mode
C_C	L	Individual clocking with $\overline{CE}_n$
$\overline{CE}$	L	Common clocking with C_C

MOTOROLA
SEMICONDUCTOR ▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬
TECHNICAL DATA

Product Preview

- 500 ps Max. Propagation Delay

The MC10E/100E101 is a quad 4-input OR/NOR gate.

PINOUT: 28-LEAD PLCC (TOP VIEW)
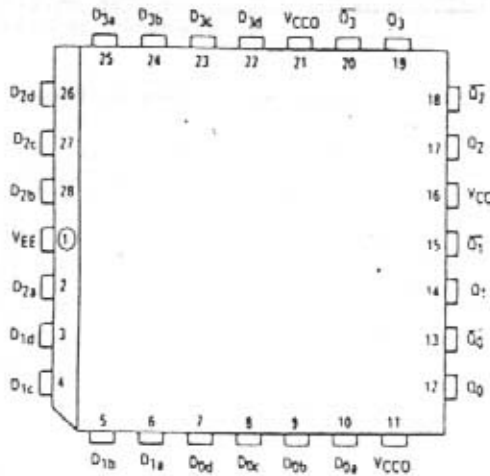
LOGIC SYMBOL
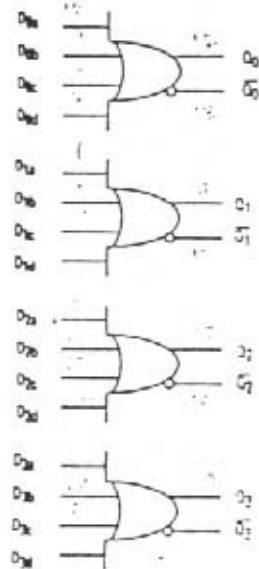
PIN NAMES

Pin	Function
$D_{0a} - D_{3d}$	Data Inputs
$Q_0 - Q_3$	True Outputs
$\overline{Q_0} - \overline{Q_3}$	Inverting Outputs

RISTICS: V_{EE} ... V_{EE} (max) ... V_{CC} ... ...

Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
HIGH Current			150			150			150	μA	
Supply Current		30	36		30	36		30	36	mA	
		30	36		30	36		35	42		

RISTICS: V_{EE} V_{EE} (min) to V_{EE} (max), V_{CC} · V_{CCO} GND

Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
ation Delay to Output	150		500	150		500	150		500	ps	

Product Preview

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and TC Generation
- Asynchronous Master Reset

The MC10E 100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10KH family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically re-load upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

MC10E016
MC100E016

8-BIT SYNCHRONOUS BINARY UP COUNTER

PINOUT: 28-LEAD PLCC (TOP VIEW)
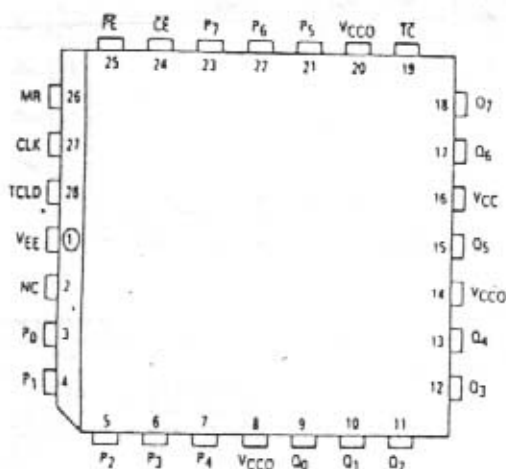
FUNCTION TABLE

CE	PE	TCLD	MR	CLK	Function
L	L	X	L	Z	Load Parallel (P_n to O_n)
H	L	X	L	Z	Load Parallel (P_n to O_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	Z	Reset (O_n = LOW, $\overline{TC}$ = HIGH)

Z = clock pulse (low to high),
ZZ = clock pulse (high to low)

PIN NAMES

Pin	Function
P_0-P_7	Parallel Data (Preset) Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input

DC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		151	181		151	181		151	181		
	100E		151	181		151	181		174	208		

AC CHARACTERISTICS: V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND

Symbol	Characteristic	T_A = 0°C			T_A = 25°C			T_A = 85°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q	450		1000	450		1000	450		1000		
	MR to Q	450		1000	450		1000	450		1000		
	CLK to $\overline{TC}$	400		900	400		900	400		900		
	MR to $\overline{TC}$	400		900	400		900	400		900		

Product Preview

- 600 ps Max. Propagation Delay
- OR-NOR Function Outputs

The MC10E/100E104 is a quint 2-input AND-NAND gate. The function output F is the OR of all five AND gate outputs, while $\bar{F}$ is the NOR.

MC10E104
MC100E104

QUINT 2-INPUT
AND/NAND GATE

PINOUT: 28-LEAD PLCC (TOP VIEW)
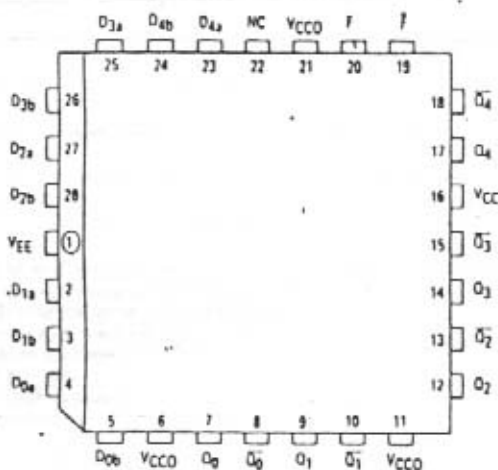
LOGIC SYMBOL
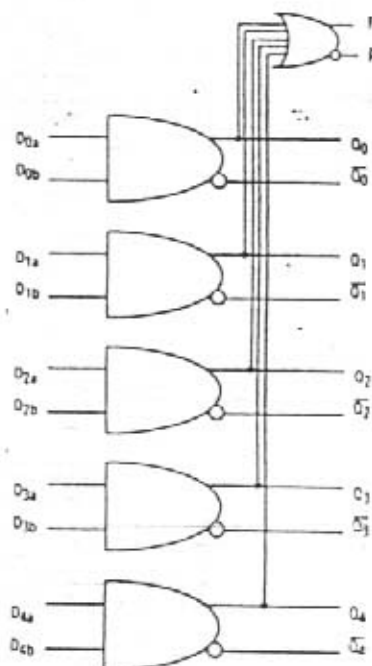
PIN NAMES

Pin	Function
D_{0a}–D_{4b}	Data Inputs
Q_0–Q_4	AND Outputs
$\bar{Q}_0$–$\bar{Q}_4$	NAND Outputs
F	OR Output
$\bar{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \cdot D_{0b}) + (D_{1a} \cdot D_{1b}) + (D_{2a} \cdot D_{2b}) + (D_{3a} \cdot D_{3b}) + (D_{4a} \cdot D_{4b})$$

DC CHARACTERISTICS $V_{EE} = V_{EE}$ (min) to V_{EE} (max); $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current D			200			200			200	μA	
I_{EE}	Power Supply Current 10E 100E		38 38	46 46		38 38	46 46		38 44	46 53	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}$ (min) to V_{EE} (max); $V_{CC} = V_{CCO} = GND$

Symbol	Characteristic	$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q D to F	200 300		600 800	200 300		600 800	200 300		600 800	ps	

Magnum Microwave
Voltage Controlled Oscillator

Electrical Specifications[1]:

HV37T-1

Parameter	Specifications
Frequency Range	200 to 400 MHz
Power Output at 25°C (50 ohm load)	+10 dBm, min.
Power Output Variation vs. Temperature	±.5 dB, typ.
Frequency Drift vs. Temperature[2]	10 MHz, typ.
Frequency Pulling (12 dB Return Loss)	1.0 MHz, typ.
Frequency Pushing	1.5 MHz/V, typ.
Tuning Voltage Limits	0 to +20 VDC
SSB Phase Noise (50 kHz Offset)	–110 dBc/Hz, typ.
Harmonics[3]	–10 dBc, typ.
Spurious	–70 dBc, max.
Bias Voltage[4]	+15 VDC ±1%
Bias Current[5]	30 mA, typ.
Operating Temperature	–55 to +100 °C

Outline : F1, TO-8
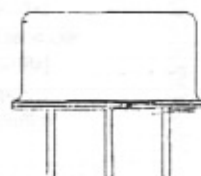
Notes:

1. Specifications guaranteed over the operating temperature range. Those specifications indicated as typical are not guaranteed. Plots exemplify typical performace at +25°C.
2. Total frequency drift over the full temperature range.
3. Worst case harmonics over the frequency range
4. Alternate bias voltages available.
5. Lower bias current available.
6. Surface mount package available
7. Military screening available.

Typical Performance at 25°C
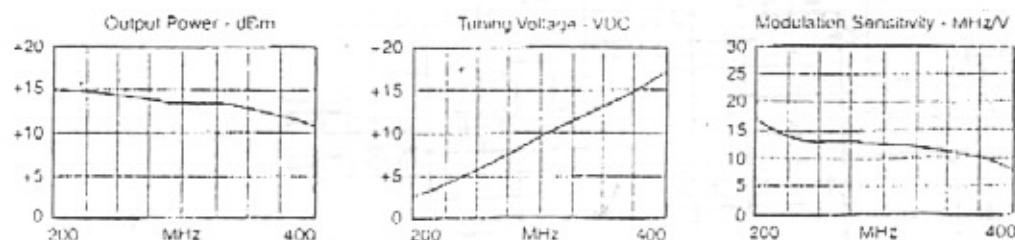
Output Power - dBm

Tuning Voltage - VDC

Modulation Sensitivity - MHz/V

Outline : F1, TO-8

HV37T-1
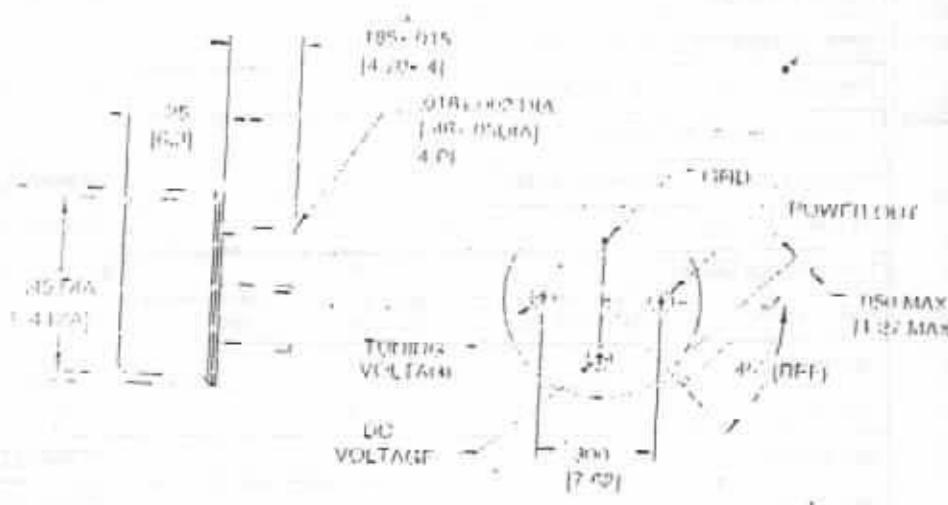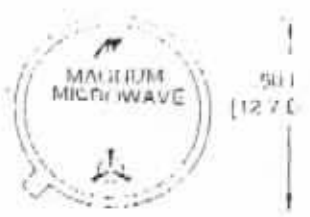
Precision Monolithics Inc.

FEATURES

Low Noise .... 80nV$_{p-p}$ (0.1Hz to 10Hz)
.... 3nV/$\sqrt{Hz}$
.... 0.2μV/°C
Low Drift
High Speed .... 2.8V/μs Slew Rate
.... 8MHz Gain Bandwidth
Low Vos 10μV
Excellent CMRR .... 126dB at V$_{CM}$ of ± 11V
High Open-Loop Gain .... 1.8 Million
Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets
Available in Die Form

ORDERING INFORMATION [1]

T$_A$ = 25°C V$_{OS}$ MAX (μV)	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP27AJ	OP27AZ	–	–	MIL
25	OP27EJ	OP27EZ	OP27EP	–	IND/COM
60	OP27BJ	OP27BZ	–	OP27BRC/883	MIL
60	OP27FJ	OP27FZ	OP27FP	–	IND/COM
100	OP27CJ	OP27CZ	–	–	MIL
100	OP27GJ	OP27GZ	OP27GP	–	XIND
100	–	–	OP27GS††	–	XIND

† For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
†† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$ at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level

signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ± 10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ± 10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS

TO-99
(J-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)

OP-27BRC/883
LCC PACKAGE
(RC-Suffix)

SIMPLIFIED SCHEMATIC

NON INVERTING INPUT (+)

INVERTING INPUT (−)

OUTPUT

* R1 & R2 ARE PERMANENTLY ADJUSTED AT WAFER TEST FOR MINIMUM OFFSET VOLTAGE

7/89, Rev. A2

(PMI)

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Input Voltage (Note 1)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	−65°C to +150°C

Operating Temperature Range

OP-27A, OP-27B, OP-27C (J, Z, HC)	−55°C to +125°C
OP-27E, OP-27F (J, Z)	−25°C to +85°C
OP-27E, OP-27F (P)	0°C to +70°C
OP-27G (P, S, J, Z)	−40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature	−65°C to +150°C

| PACKAGE TYPE	θ_{jA} (Note 3)	θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (HC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. θ_{jA} is specified for worst case mounting conditions, i.e., θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{jA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Input Offset Voltage	V_{OS}	Note 1	—	±10	25	—	20	60	—	30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	Notes 2, 3	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	µV/mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	$e_{n\text{p-p}}$	0.1Hz to 10Hz Notes 3, 5	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	µV$_{p-p}$
Input Noise Voltage Density	e_n	$f_O = 10Hz$, Note 3	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/$\sqrt{Hz}$
		$f_O = 30Hz$, Note 3	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		$f_O = 1000Hz$, Note 3	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10Hz$, Notes 3, 6	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/$\sqrt{Hz}$
		$f_O = 30Hz$, Notes 3, 6	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		$f_O = 1000Hz$, Notes 3, 6	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	Note 7	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4V$ to $\pm18V$	—	1	10	—	1	10	—	2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$, Note 4	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/µs

7/89, Rev. A

0.1Hz TO 10Hz p-p NOISE TESTER FREQUENCY RESPONSE

VOLTAGE NOISE DENSITY vs FREQUENCY

A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA

INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

TOTAL NOISE vs SOURCE RESISTANCE

VOLTAGE NOISE DENSITY vs TEMPERATURE

VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE

CURRENT NOISE DENSITY vs FREQUENCY

SUPPLY CURRENT vs SUPPLY VOLTAGE

OPERATIONAL AMPLIFIERS/BUFFERS

5

7/89, Rev. A2

TYPICAL PERFORMANCE CHARACTERISTICS

OFFSET VOLTAGE DRIFT OF
EIGHT REPRESENTATIVE UNITS
vs TEMPERATURE
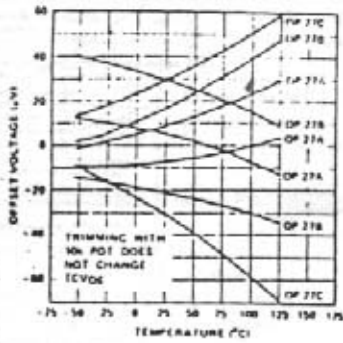
LONG-TERM OFFSET
VOLTAGE DRIFT OF SIX
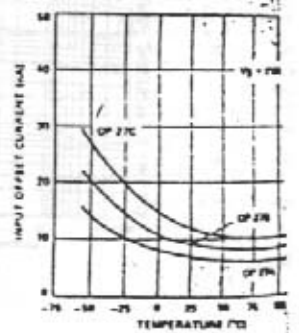REPRESENTATIVE UNITS
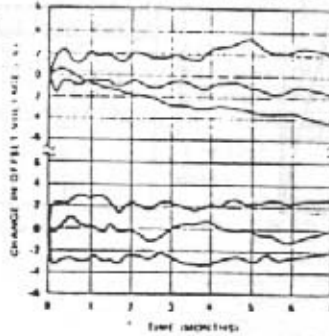
WARM-UP OFFSET
VOLTAGE DRIFT
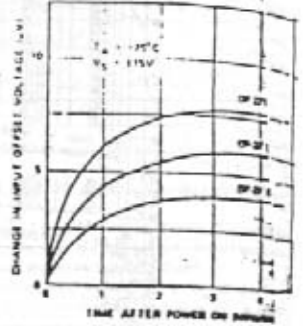
OFFSET VOLTAGE CHANGE
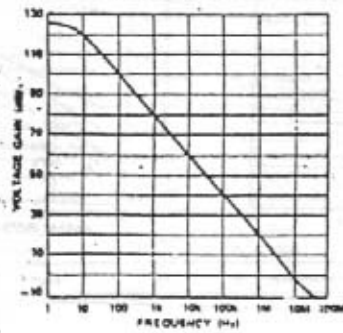DUE TO THERMAL SHOCK
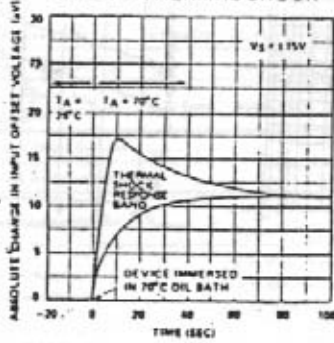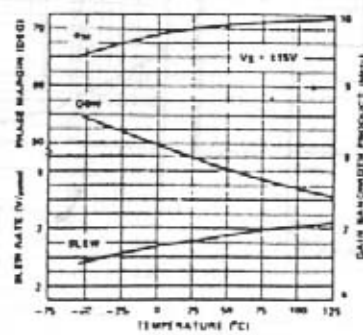
INPUT BIAS CURRENT
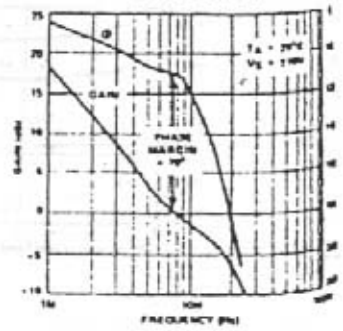vs TEMPERATURE
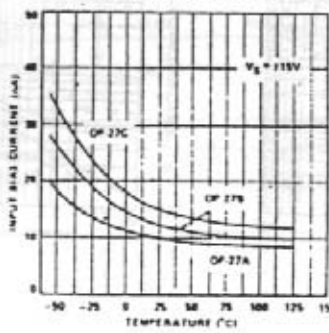
INPUT OFFSET CURRENT
vs TEMPERATURE

OPEN-LOOP GAIN vs
FREQUENCY

SLEW RATE, GAIN-BANDWIDTH
PRODUCT, PHASE MARGIN vs
TEMPERATURE
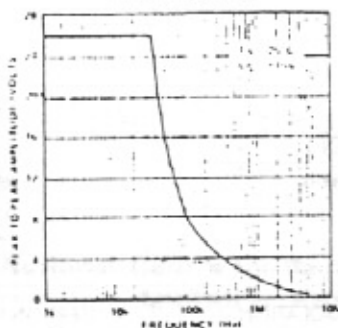
GAIN, PHASE SHIFT vs
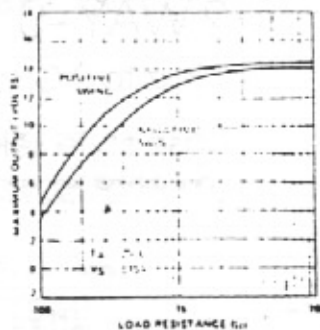FREQUENCY

PERFORMANCE CHARACTERISTICS

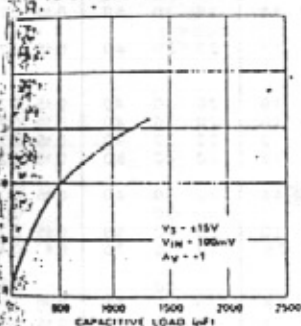### N-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE
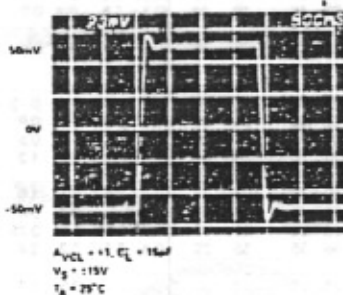
MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE
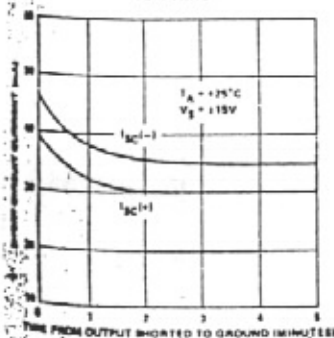
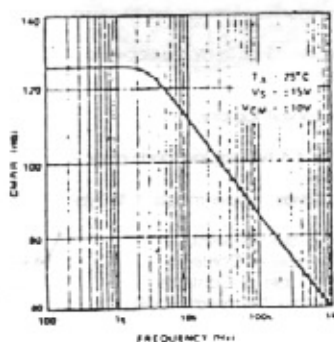### SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

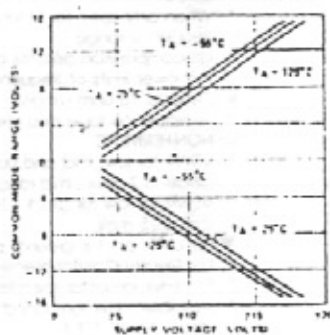### SMALL-SIGNAL TRANSIENT RESPONSE

LARGE-SIGNAL TRANSIENT RESPONSE

SHORT-CIRCUIT CURRENT vs TIME

CMRR vs FREQUENCY
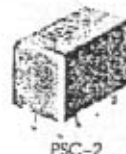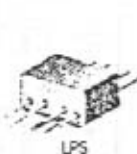
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

7/89, Rev. A2

Power Splitter/Combiners

2 WAY–0°

4 KHz to 2 GHz

case style selection
outline drawings see Table of Contents

LPS PSC-2 LRPS

MODEL NO.	FREQ. RANGE MHz	ISOLATION dB						INSERTION LOSS, dB Above 3dB						PHASE UNBALANCE Degrees			AMPLITUDE UNBALANCE dB			PRICE $	DISTRIBU
		L		'M		U		.L		'M		U		L	'M	U	L	'M	U		FACTORY
	f_L–f_U	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Max.	Typ.	Max.	Typ	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Qty. (1–9)	(1–9)
LRPS ○☐ LRPS-2-1	5–500	50	25	33	24	30	23	0.25	0.5	0.3	0.6	0.5	1.2	1.0	2.0	3.0	0.15	0.2	0.3	8.95	●
case ○○○130○☐ LRPS-2-4	10–1000	25	20	23	16	19	14	0.3–0.5		0.4	0.9	0.8	1.5	1.0	3.0	5.0	0.15	0.2	0.4	19.95	●
LPS LPS-109	10–500	35	25	30	25	30	25	0.3	0.5	0.4	0.6	0.5	1.1	2.0	3.0	4.0	0.15	0.2	0.3	17.95	●
case 8B48																					
PSC-2 PSC-2-1	0.1–400	20	15	25	20	25	20	0.2	0.5	0.4	0.75	0.6	1.0	2.0	3.0	4.0	0.15	0.2	0.3	10.95	●
case A01 PSC-2-1W	1–650	25	20	35	20	25	20	0.3	0.6	0.5	0.9	0.7	1.0	2.0	3.0	4.0	0.15	0.2	0.3	16.95	●
(PSC-2-2	0.004–60	27	20	30	20	27	20	0.3	0.5	0.3	0.6	0.6	1.0	2.0	3.0	4.0	0.15	0.25	0.3	23.95	●
PSC-2-4	10–1000	30	25	25	20	25	20	0.6	1.0	0.6	1.2	0.7	1.3	2.0	4.0	8.0	0.15	0.2	0.4	23.95	●
PSC-2-5	10–1400	28	18	22	17	24	17	0.3	0.6	0.6	1.0	0.9	1.6	2.0	3.0	4.0	0.15	0.2	0.4	29.95	●
PSC-2-4S	700–900			20	17					0.2	0.4				3.0			0.2		22.95	●
■ PSC-2-1-75	0.25–300	20	15	30	20	20	15	0.4	0.75	0.4	0.75	0.4	1.0	2.0	3.0	5.0	0.15	0.2	0.3	13.45	●
case A06 ■ PSC-2-1-75A	1–200	35	27	46	35	36	25	0.1	0.3	0.2	0.4	0.35	0.6	1.0	1.0	2.0	0.1	0.15	0.15	14.45	●
■ PSC-2-1V-75	40–450			31	27					0.5	1.0				4.0			0.3		14.45	●
■ PSC-2-1W-75	30–600	30	22	—	—	30	20	0.4	0.8	—	—	0.6	1.2	2.0	—	4.0	0.20	—	0.3	18.95	●
(■ PSC-2-2-75	0.008–60	35	20	40	25	30	22	0.1	0.4	0.15	0.4	0.3	0.8	1.0	1.0	1.0	0.15	0.15	0.15	23.95	●
■ PSC-2-4-752	10–850	31	20	32	23	23	15	0.3	0.5	0.4	0.6	0.5	1.0	2.0	5.0	10.0	0.1	0.2	0.5	23.95	●
■ PSC-2375	55–85			35	25					0.3	0.5				1.0			0.1		23.95	●

L = low range (f_L to 10 f_L) M = mid range (10 f_L to f_U/2) U = upper range (f_U/2 to

NOTES:
* When only spec for M range given, specification applies to entire frequency range.
◇ 1dB compression derates approximately 13 dB from the upper to the lower limits of frequency range L.
■ Denotes 75 ohm models
○ Available on tape and reel. Please consult factory.
�'ᐧ NON HERMETIC
: VSWR for low, mid and upper range, 1.1 typical, low and upper range, 1.2 max., mid range 1.15 max.
∴ VSWR for low range, 1.1 typical, 1.3 max., upper range, 1.15 typical, 1.25 max
▼ For LRPS, pin 1 is ground, pins 2 and 5 are not used.
1. For Quality Control procedures, see Table of Contents.
2. For environmental specifications, see Table of Contents.
3 Absolute maximum rating: All models are 1W, internal load dissipation 0.125W