A Project Report on

DIGITAL SIGNAL PROCESSING IN RADIO ASTRONOMY APPLICATIONS

SUMAN CHAKRABORTI

UNDER THE GUIDANCE OF

YASHWANT GUPTA

GIANT METRE-WAVE RADIO TELESCOPE (GMRT)

NATIONAL CENTRE FOR RADIO ASTROPHYSICS (NCRA)

TATA INSTITUTE OF FUNDAMENTAL RESEARCH (TIFR)

ABSTRACT

The Project assigned to me was to synchronize 2 pulses , one coming from the GPS receiver of periodicity 1ppm and user controlled PC Signal. For that I needed to set up a pulse stretcher circuit using 555 Timer circuit. The datasheets of different ICs of 555 Timers was studied and finally IC DM74123 was chosen as best suiting our needs. The circuit was properly implemented on a PCB and desired output was obtained .However the Actual GPS Pulse was not put to use. In place of that both the required was obtained from the MCM Card.The results obtained was in affirmation with the theory.

Acknowledgement

I would like to extend my thanks to my Guide Prof Yashwant Gupta for his incessant interest in my regular day to day work whenever it was possible for him. My heartfelt thanks to Mr B. Ajith Kumar for the patience and step by step assistance he extended towards me in completing the project. Mr T.L. Venkatasubramani also helped me in getting acquitanted with the GMRT system.

My respect to Prof Rajaram Nityananda for providing us all the support and entrusting his belief in assigning the Project.

I am indebted to Mr Navnath shinde in helping me getting introduced to the various appratus in the Analog Lab.

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Sincere thanks to Dr Sabyasachi Pal(NCRA) for his extremely enjoyable chats every now and than giving us a detailed insight on the Physics behind our work.We got to know much from him on radioastronomy.

My thanks to my Teachers at The Institute of Radio Physics and Electronics , especially to Prof P.K.Basu . Finally my thanks to my friends Ashok, Partha, Soumo and my senior Mr Somak Bhattacharyya for assisting me in my project.

SUMAN CHAKRABORTI

Contents

Chapter 1

An Introduction to GMRT

Brief Introduction of GMRT

fig1.1.Giant Antenna of GMRT

Giant Meter wave Radio Telescope (GMRT) is a project run by the National Centre for Radio Astrophysics(NCRA) under Tata Institute of Fundamental Research(TIFR) INDIA. It is one of the largest radio telescope observatory in the world operating at meter-wavelengths. GMRT is situated at Khodad 80 km North of Pune .It has 30 fully steerable giant parabolic dishes of 45 m diameter each,spread over distance of about 25 km in a Y shape array.

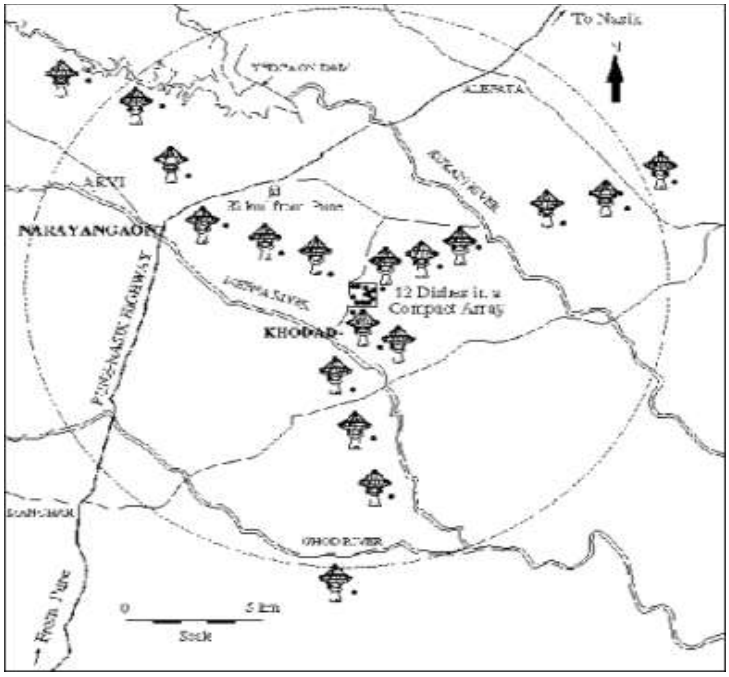


fig1.2.location of GMRT antennas (30 dishes)

Among these thirty dishes fourteen are located more or less randomly in a compact central array in the region of about 1 sq km. The remaining sixteen antennas are spread out along the 3 arms of the 'Y' -shaped configuration over a much larger region. Currently GMRT operates in five different bands centered at 150, 233,327,610 and 1420 Mhz . At all these feeds the dual polarization outputs are available .The metre wavelength part of the radio spectrum has been particularly chosen for study with GMRT because man-made radio interference is considerably lower in this part of the spectrum in India. Although there are many outstanding astrophysics problems which are best studied at metre wavelengths, there has, so far, been no large facility anywhere in the world to exploit this part of the spectrum for astrophysical research .

Chapter 2

Analytical Background of the Scheme

2.1 GMRT Receiver System

The GMRT currently operates at five different frequencies ranging from 150 MHz to 1420 MHz. Some antennas have been equipped with receivers which work up to 1750 MHz. Above this frequency range however, the antenna performance degrades rapidly both because the reflectivity of the mesh falls and also because of the deviations of the plane mesh facets from a true parabola. A 50 MHz receiver system is also planned, which is not yet operational. All the feeds provide dual polarization outputs. Here, the RF signals in two polarizations are passed through two channels each of maximum band width of 32 MHz. Then each of these signals are down converted to 70 MHz first and then up converted to 130 MHz & 175 MHz respectively in the IF system using LO signals . The signals are then combined & sent to Central Electronics Building(CEB) through optical fibre link. Signals are then processed in the Baseband system, where each polarization is converted into two sidebands of 16 MHz bandwidth. Thus a total of 4 baseband channels are available from each antenna which are sampled & digitized with ADC with sampling frequency 32 MSPS. The signals are further processed using hardware based correlator.

Now an upgraded GMRT receiver system is being planned with improved sensitivity, instantaneous bandwidth & more facilities. In the new scheme a wider bandwidth signal will be digitized with less electronics at the remote antenna sites. The current idea is to send the entire RF spectrum received at the feeds to the CEB & further processing is to be done there. The possibility of direct down conversion and digitization of the signals is being investigated with the concept of Bandpass Sampling.

The basic block diagram of GMRT receiver system is shown in the figure below.

10

- **Current receiver system**

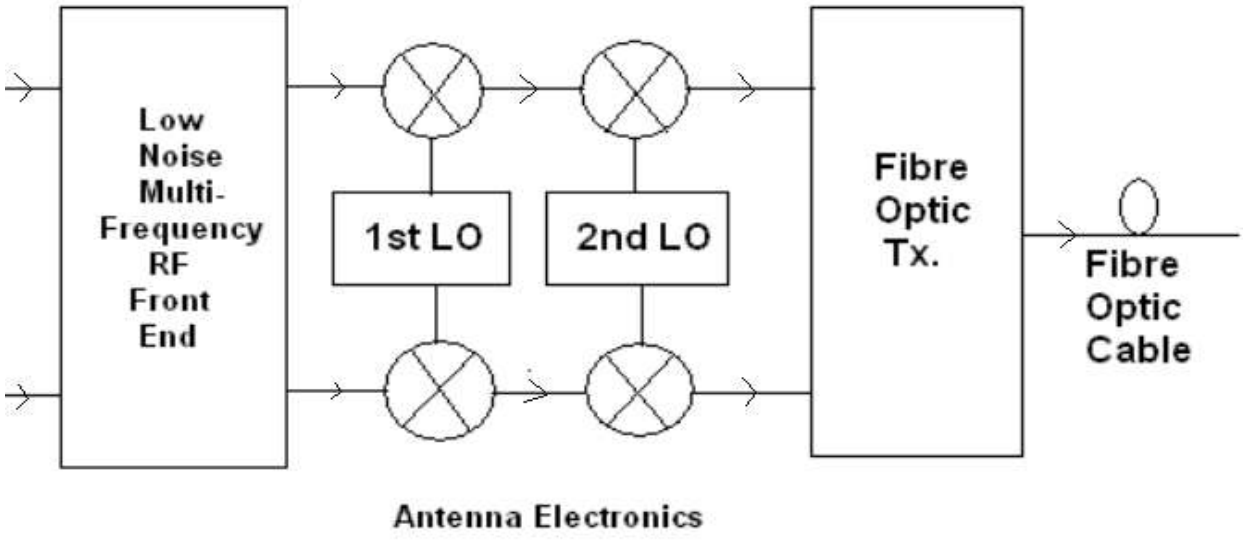


fig2.1

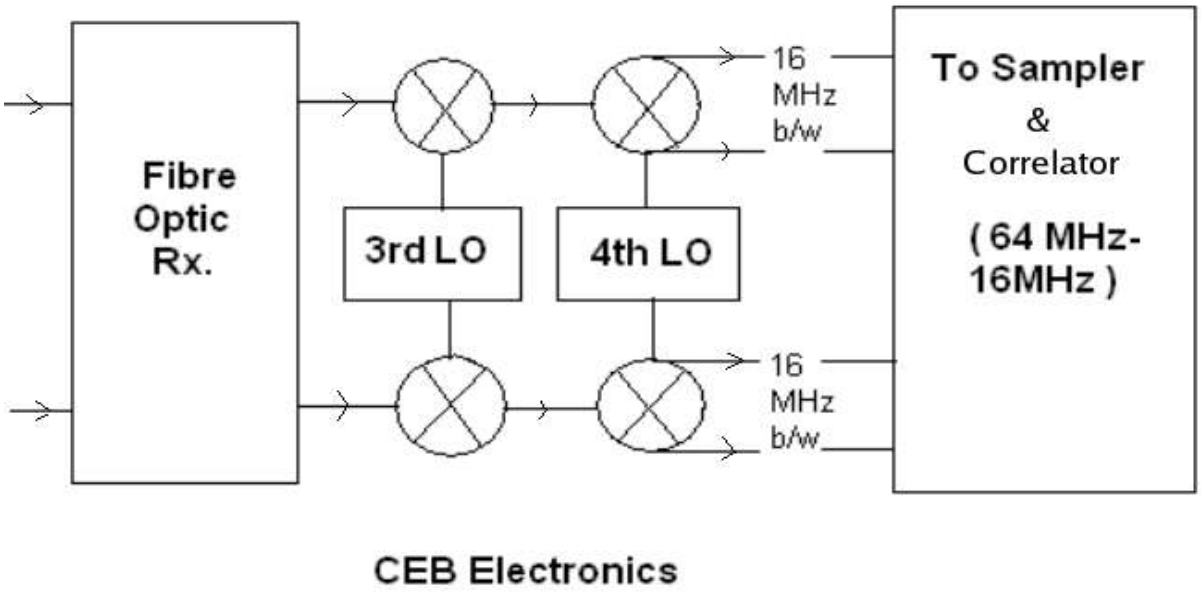


fig2.2

2.2 SOFTWARE BACKEND

2.2.1 Description of the Software Backend

A software based correlator is currently being developed as an alternative to the existing hardware correlator. In the new system being planned RF signals from the antennas received at the CEB at IF of 130 & 175 MHz are converted to suitable frequency and then digitized using PC based ADCs. The digitized data is further processed in powerful computers using software.The software backend at GMRT used for interferometric observation is a 32 MHz wide FX correlator which can go up to 100 MHz.

Each antenna is dual polarized and each polarized signal (which has a maximum bandwidth of 32 MHz) is digitized in separate ADC channel. So 30 antennas needs 30*2=60 ADC inputs of 32 MHz bandwidth with a sampling frequency is 66MHz. So there is no need to split the received signal into USB & LSB as in the current receiver.

PCI based quad input ADCs are used for digitizing the data. In the software backend 16 such ADC cards are used, eight for each polarization channel. Each ADC card is installed in a separate PC, thus a total of 16 PCs are used for data acquisition and another 32 PC s are used for data processing.

The 16 data acquisition PC s are to be provided with same clock pulse signal and should be triggered together.

2.2.2 Advantages of the Software Back end

The software back end system is better than the hardware system because of the following reasons :

1. Bandwidth of the software system can reach up to a maximum of 100 MHz but at present up to 32 MHz is used .
2. Reconfiguring of the system is easier than that of the hardware portion.
3. Standard components are used & only changes in the program are to be made for any discrepancies rather than discrete hardware components .

2.2.3 Background of the Scheme

The 30 antennas of GMRT received the information from a source in form of analog waveform. Then the received signal is digitized using ADCs. All the antennas in GMRT are tracking the same information at a time. So, the received signal, which is analog in nature, is converted to its corresponding digital form at a time. It is very important that all the 16 ADCs are triggered at a time to calculate the correct correlation values.

The trigger signal for this data acquisition PCs are to be synchronized to the nearest 1ppm pulse. In GMRT, the 1ppm signal from a GPS receiver is used for this purpose.

The ADC s are triggered by generating a user controlled signal. But the problem is that there is always some random delay between the GPS signal and the PC signal that is generated by computer programming. Using computer programming we can control the delay but cannot synchronize the trigger pulse to the 1ppm from GPS.

Also the delay between the GPS signal and the PC signal is not constant . But the delay can be varied up to 100 ms using programming.

Chapter 3

Project Objective

3.1 Project Objective:

There are two signals one coming form GPS receiver and another is generated by computer programming. Generally the GPS pulse is coming with a periodicity *1ppm(pulse per minute)*.But the problem is that the signal that generated by computer programming(PC signal) is not synchronized with the 1 ppm signal that comes form GPS receiver. Our objective is to design a circuit , which is able to make this two pulse synchronized.

The basic block diagram of this circuit is shown in fig.3.1

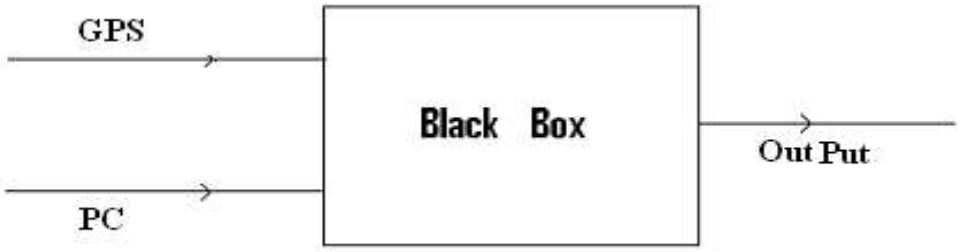


fig.3.1:Block Diagram

Also the nature of incoming pulses and required output pulse is shown below

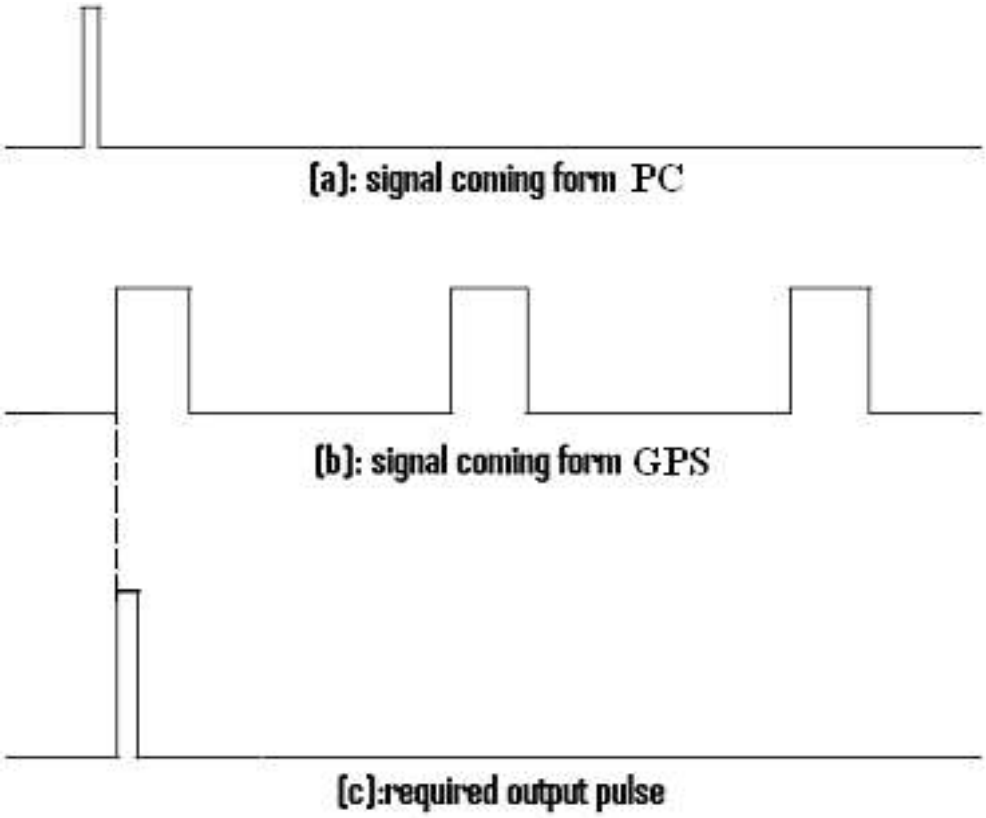


fig.3.2:Nature of Pulses

It is already mentioned that the two signals are not synchronized *i.e.* there are always some delay between the PC and GPS pulses. Generally the PCs programmed in such a way that the rising edge of GPS signal appear earlier than the rising edge of PC signal. But It is required that the rising edge of output pulse should be synchronized with the rising edge of GPS pulse. It will occur if the two pulses are send through an **AND** gate. But the scheme is not so simple that it looks. Another problem is still there. The problem is that the time delay is not constant. It may changes with time. To remove this problem at first we have to stretch the PC signal, then send the GPS signal and delayed PC signal through AND gate.

So the basic block diagram is shown in the *Fig3.3*

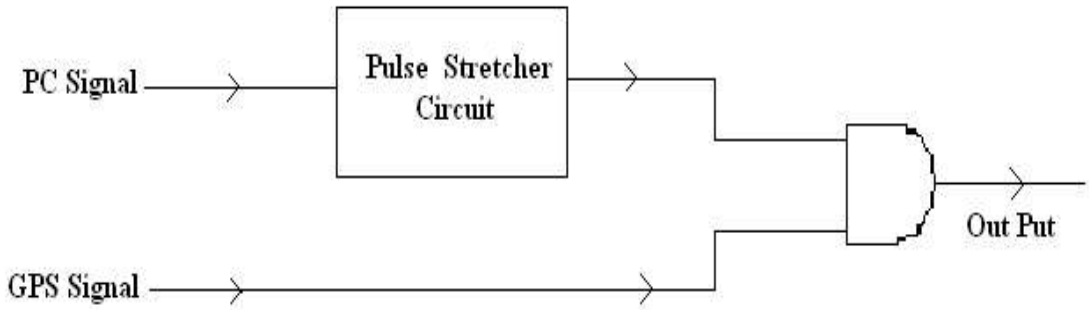
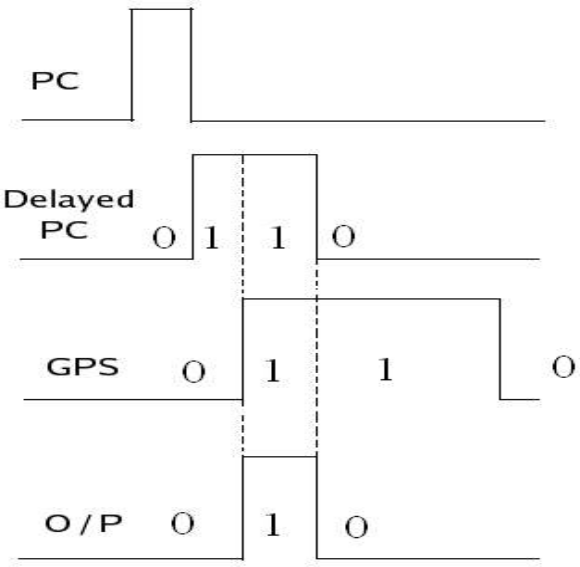


fig3.3:Basic Block Diagram



Truth table

Inputs		*Output*
PC	GPS	
0	0	0
0	1	0
1	0	0
1	1	1

fig3.4. Truth Table

So our first target is to design a **Pulse Stretcher Circuit** and we can design it using a **555 Timer** very easily and then pass the stretched output pulse and the GPS pulse through an AND gate.

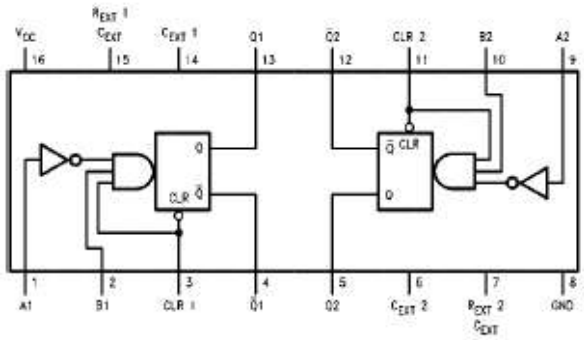
Chapter 4

Circuit Design and Measurements

4.1 555 Timer IC

There are many types of 555 Timer IC available in market. We can choose any of them four our job .I choose the IC DM74123 because it is available in laboratory.

Connection Diagram



Triggering Truth Table

Inputs			Response
A	B	CLR	
X	X	L	No Trigger
↓	L	X	No Trigger
↓	H	H	Trigger
H	↑	X	No Trigger
L	↑	H	Trigger
L	H	↑	Trigger

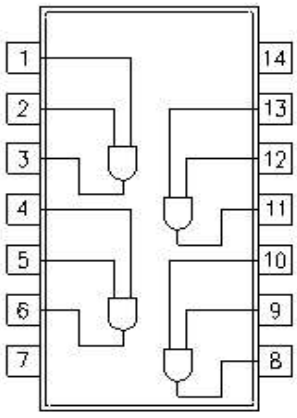
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

fig4.1

4.2 AND Gate IC

This is also a easily available IC. I choose IC 7408 for my job.

Connection diagram



7408

Pin Number Description
1 A Input Gate 1
2 B Input Gate 1
3 Y Output Gate 1
4 A Input Gate 2
5 B Input Gate 2
6 Y Output Gate 2
7 Ground
8 Y Output Gate 3
9 B Input Gate 3
10 A Input Gate 3
11 Y Output Gate 4
12 B Input Gate 4
13 A Input Gate 4
14 Positive Supply

fig4.2

4.3 Pulse stretcher circuit using IC 74123

4.3..1 Aim:

- To stretch a 20 ms pulse to a 100 ms pulse.
- To check the output pulse width with the variation of input pulse width.
- To check the output pulse width with time for a fixed input pulse width*(say 20ms)*

4.3.2 Pulse specification:

- Pulse width =20ms
- Pulse period = 1ppm(60 sec)
- Pulse amplitude =3volt

4.3.3 Calculation :

According to the datasheet of **IC 74123** the output time delay depends on the externally connected resistance R_x and the capacitance $C_{x.}$ The output pulse width of the circuit can be expressed as,

$t_A = k*R_x*C_x*(1+0.7Rx)$

Here t_A=100ms=$100*10^{-3}$ sec

Let the value of the capacitor C_x=10μF=$10*10^{-6}$ F

So the value of the resistance Rx =35.714 kilo ohm

The circuit diagram of Pulse stretcher circuit is shown in next page.

4.3.4 Neat circuit diagram:

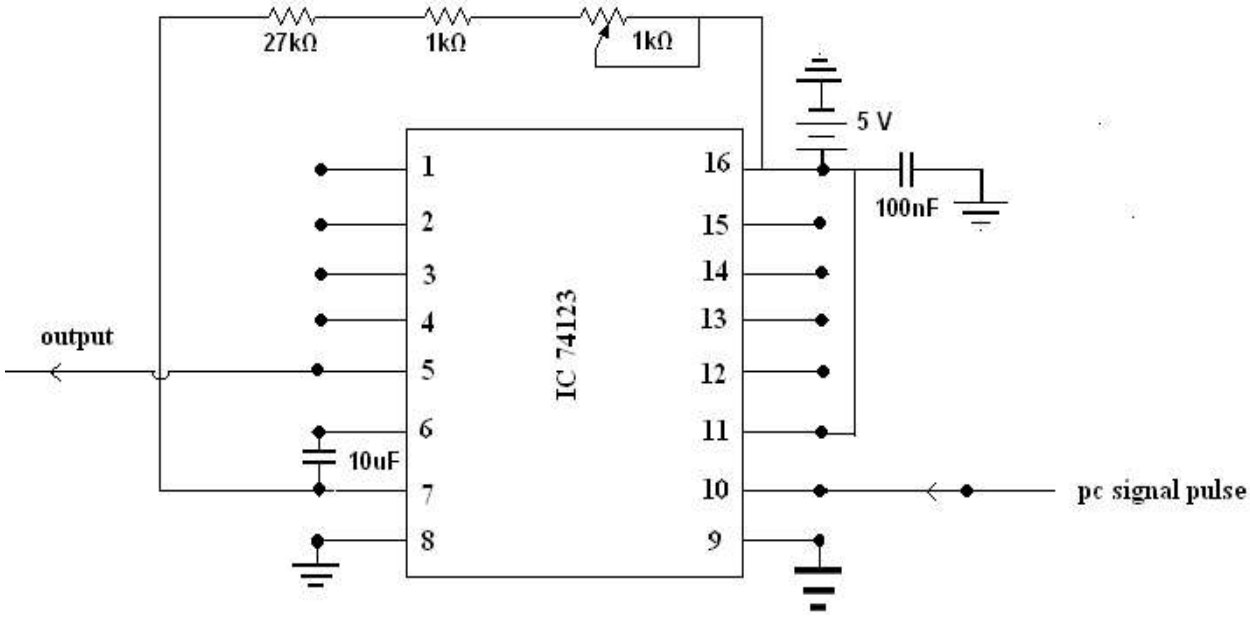


fig.4.3

4.3.5 Practically used value:

- Standard 555 chips create significant "glitch" on the supply when their output changes state .This is rarely a problem in simple circuits with no other IC, but as we require a better performance ,so a **'smoothing capacitor' should** be connected across the $+V_s$ and 0V supply terminal.
- The value of the smoothing capacitor=100nF.
- The value of external capacitor is C_x=10μF.
- Input terminal = 10^{th} Pin.(B)
- As we design the circuit for Positive edge triggering so we put the 9^{th} Pin (A) at ground(0v) and 11^{th} Pin at higher state($+V_s$).

4.3.6 **Experimental Data:**

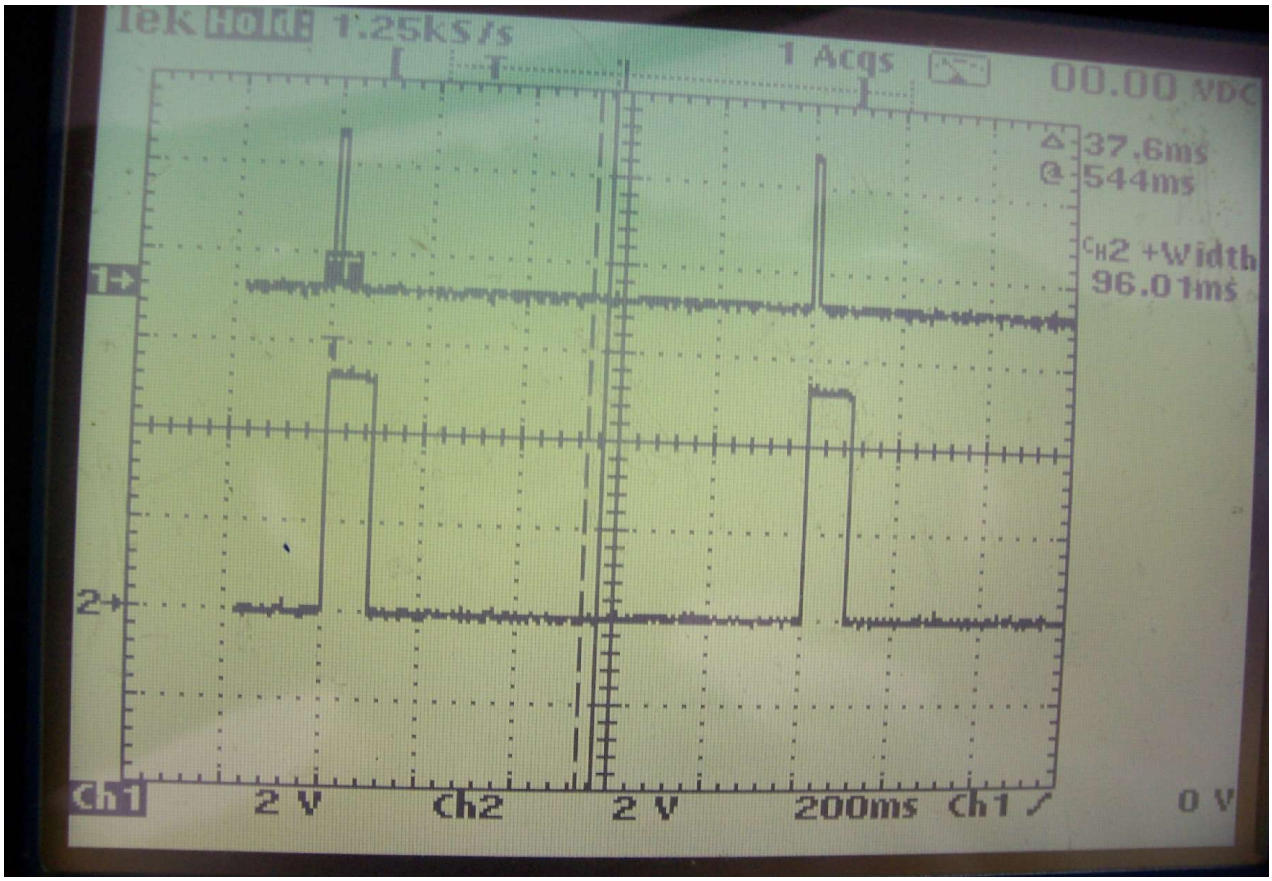
(A)Table to chose the value of external resistance R_x.

Table -A

Resistance in kilo ohm	Pulse width in ms
35.0	122.0
28.5	108.9
27.0	96.1
28.5	106.0
28.5	112.0
28.5	112.0
28.5	111.9
28.5	112.0

- So the practically chosen value is 28.5 kilo ohm.
- It is very difficult to maintain the output pulse width at exactly 100 ms using discrete resistance,as all the resistance value are not available. So we keep the output pulse width at a value nearly equal to 100 ms.

Output of the Pulse stretcher circuit



Channel 1--- Input Pulses

Channel2--- Output stretched Pulse

(B)To observe the output pulse width for different input pulse width:

Table (B)

Input Pulse width	Output pulse width in ms
50 ms	112.0
	112.0
	108.0
	111.9
30 ms	112.0
	112.1
	112.0
	112.0
20 ms	112.0
	112.0
	112.0
	111.9
10 ms	112.0
	108.0
	112.0
	112.0
1ms	112.0
	112.1
	111.9
	111.9

10µs	112.0
	112.0
	111.9
	112.0
Input Pulsewidth	Output Pulsewidth
5µs	111.9
	112.0
	112.0
	112.0
2µs	112.0
	111.9
	108.9
	112.0

- So the output pulse width remain constant within a wide range of input pulse width and it will remain constant upto 65 ns(*according to datasheet of* ***IC74123***)

4.4 Design of the Pulse synchronization circuit :

As we already mentioned that our main target is to synchronize the user generated pulse generated by computer programming with the pulses coming from GPS receiver. So the basic block diagram of such a system is given below ,

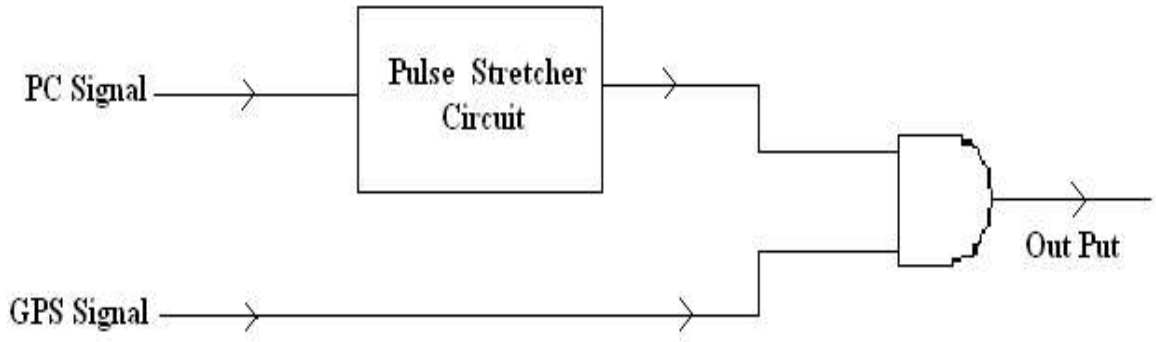


fig.4.4

Now replacing by the Pulse Stretcher circuit the block diagram changes to,

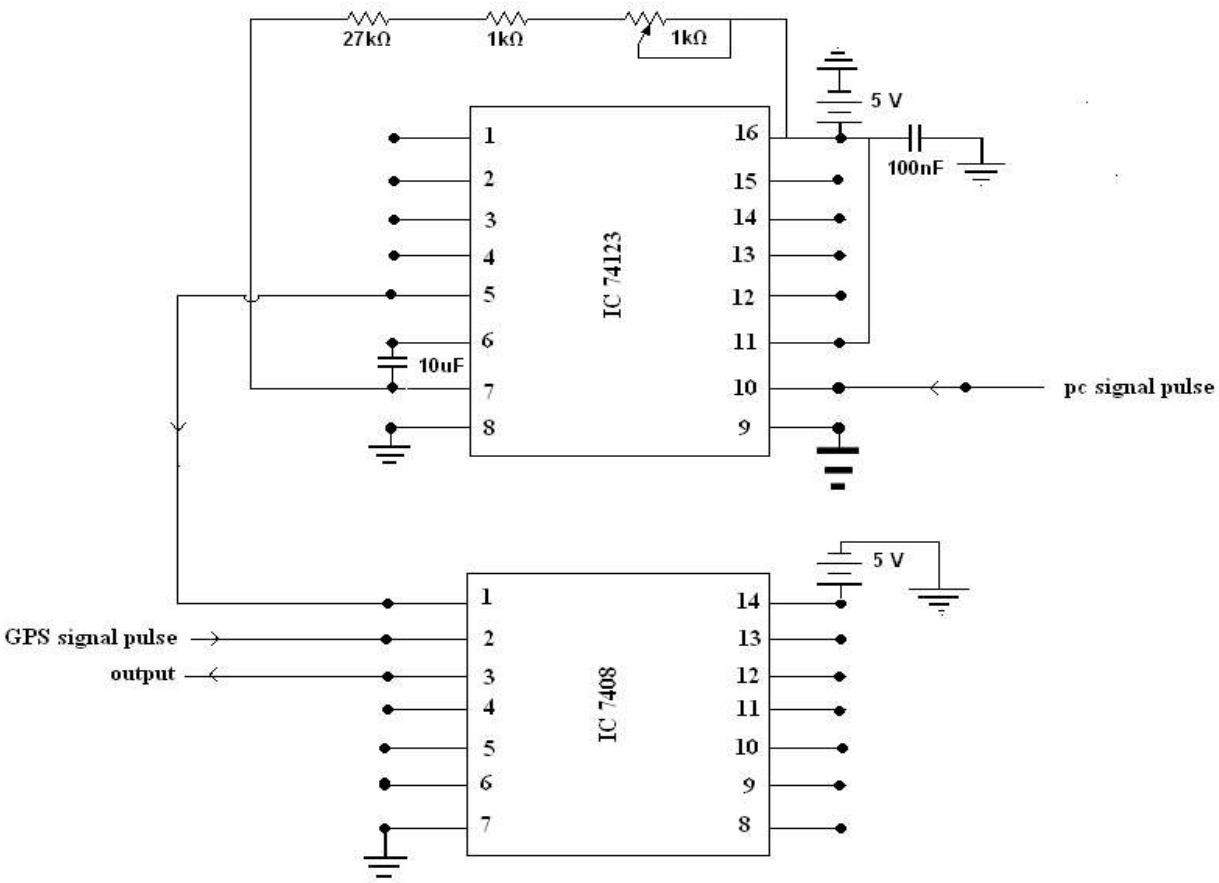


fig4.5

6.2.1 Experimental Data:

(A) To observe the output pulse width for different input pulse width:

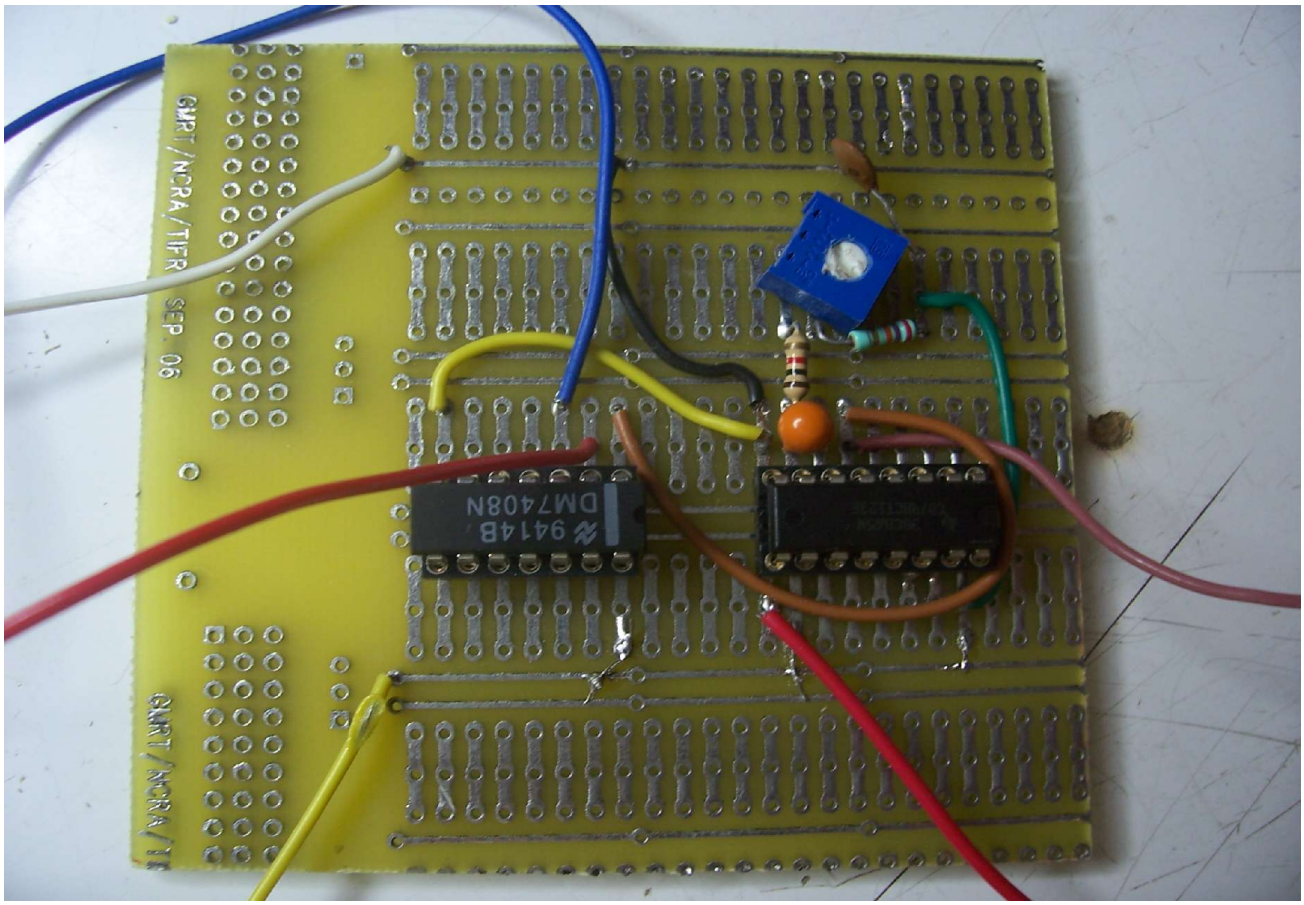
- Putting the one of the input of AND gate at the high state :

Table (A)

Input pulse width	Output pulse width in ms
50 ms	112.0
	112.0
	108.0
20 ms	112.0
	112.0
	112.0
10 ms	112.0
	108.0
	112.0
1ms	112.0
	111.9
	111.9
10μs	112.0
	111.9
	112.0
5μs	111.9
	112.0
	112.0
2μs	112.0
	111.9
	112.0

- So the output pulse width remain constant within a wide range of input pulse width .

Prototype of the circuit



Circuit implemented on a PCB

(B) Measurement of Time delay between input and output with change in input pulse width.

Table (B)

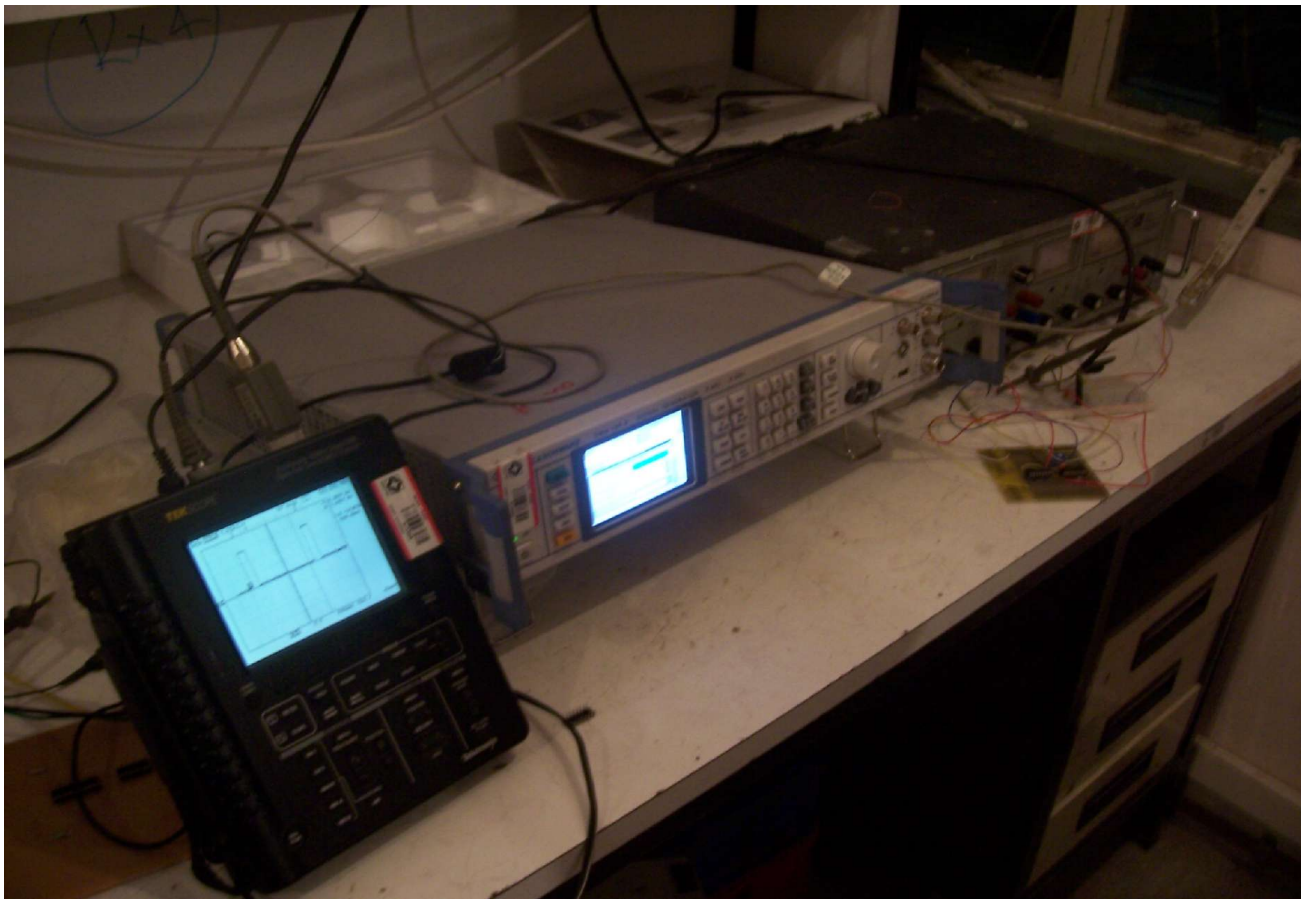
Input pulse width	Time delay in ns
50 ms	23.4
20ms	23.4
10 ms	23.4
1 ms	23.4
10 μs	23.4
5 μs	23.4
2 μs	23.4

- So the time delay remain constant within a wide range of input pulse width.

6.3 Design Problem Faced and Solution

Initially a PCB Layout was made which was not giving the necesaary output .The reason was that the PCB chosen at first was of a poor quality, there were soldering problems which gave rise to stray capacitive and resistive effects thus hindering the desired 100ms response.
However this was overcome by choosing a better PCB and making fine solders which resulted in marked improvement in the output response and one could get 112.0ms response ..... earlier it was a constantly varying response with wide range of fluctuations.

Arrangement to Test the Pulse Stretcher circuit



Chapter 5

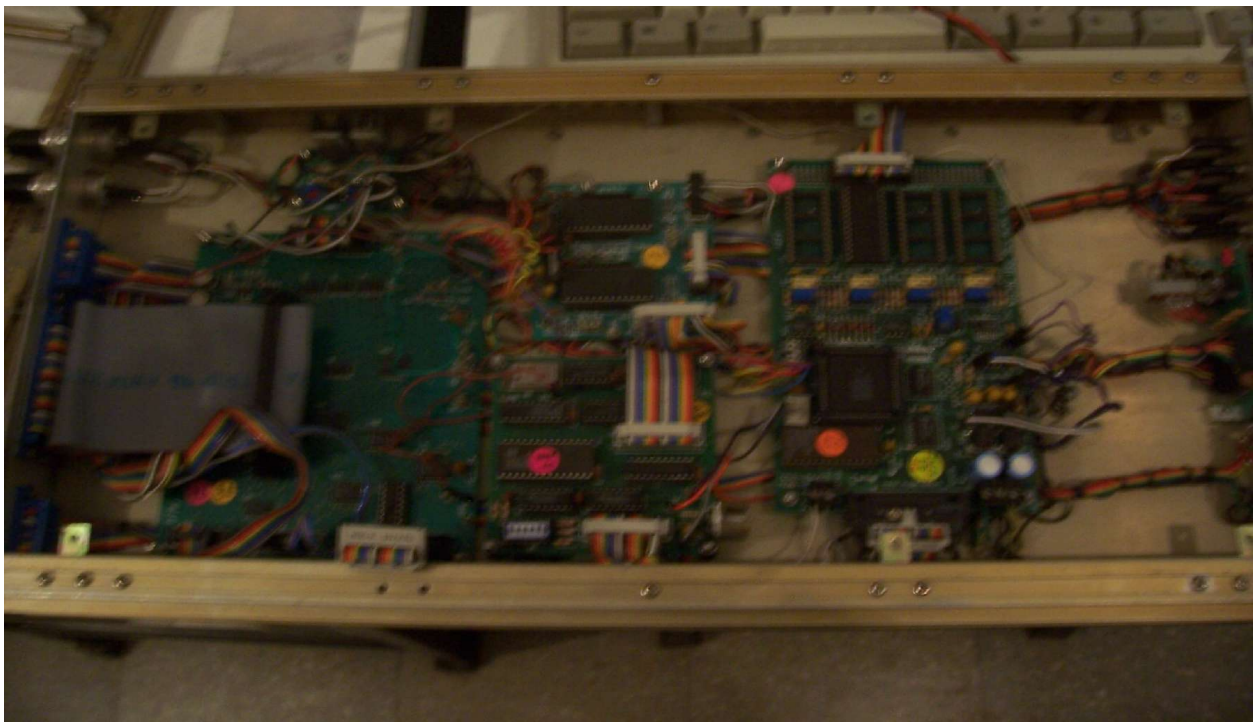
Testing and verification

5.1 Introduction:

Now to check the circuit we need two signal one coming from the GPS receiver and another is generated by some computer programming. We tested the same signals in the Lab by using two signals generated from the Monitor and Control Modules (MCM Cards). This Provide more flexibility for varying the input signal parameters.

MCMs are general purpose microcontroller based cards which provides 16 TTL control outputs and can monitor upto 64 Analog Signals. these MCMs are the interface to all the settable GMRT subsystems like the frontends, the LOs, the attenuators etc.

Picture of MCM card



5.2 Generation of the Test Signal

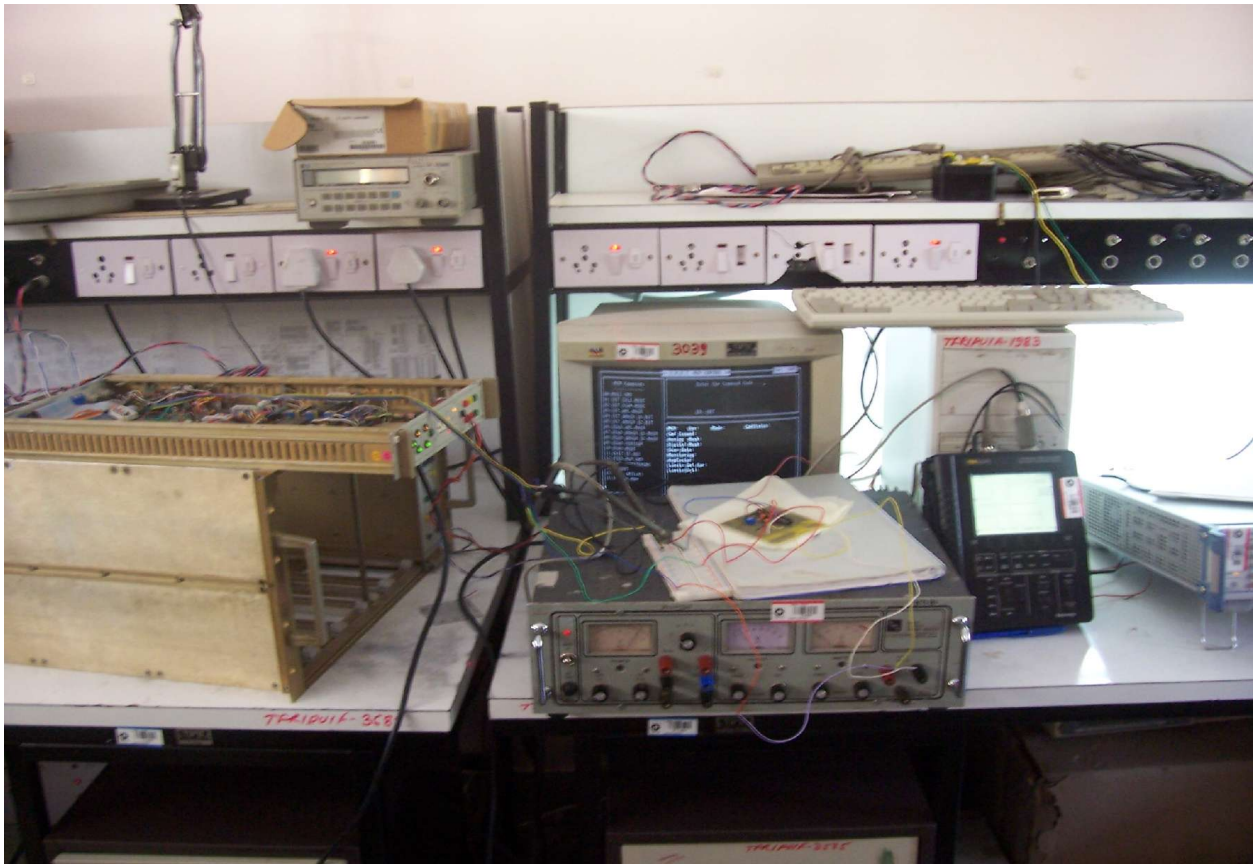
The required signal is generated at the output of the MCM card by feeding it with a computer generated program created and run as an executable file .The Port two address of the MCM Card was chosen to generate the signal. The program is executed in such a way that it generate only three pulse in a particular sequence at a time.

The program consisting of HEX code given in DOS prompt is given below:-

```
:2
0000 0000
8000 8000
C000 C000
4000 4000
4000 4000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
8000 8000
C000 C000
4000 4000
4000 4000
0000 0000
```

0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
8000 8000
C000 C000
4000 4000
4000 4000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
0000 0000
q

Picture of the Total Setup to test the circuit :-



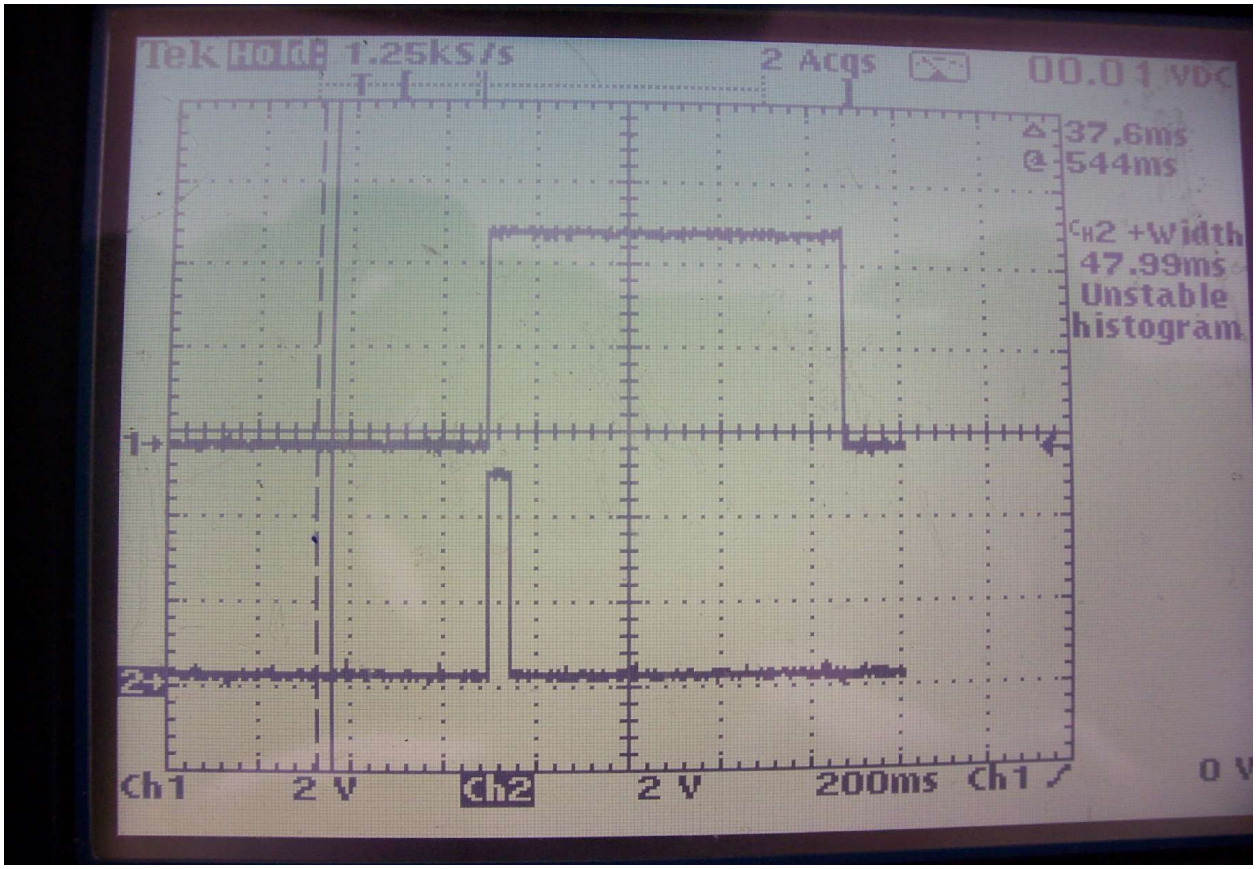
5.3 Test Results :-

Signal Specifications at the output of the MCM Card :

Trigerred (PC) Signal Width = 96 ms

ppm Signal Width (GPS) = 757 ms

Pulse Period =4.38 s



Output Waveform on the Digital Signal Oscilloscope (DSO) Meter

Channel 1------- GPS pulse

Channel 2------Output pulse

- So It is clear from the picture that the rising edge of the output pulse is synchronized with the rising edge of the GPS pulse.

5.3 Explanation of Output Waveform :-

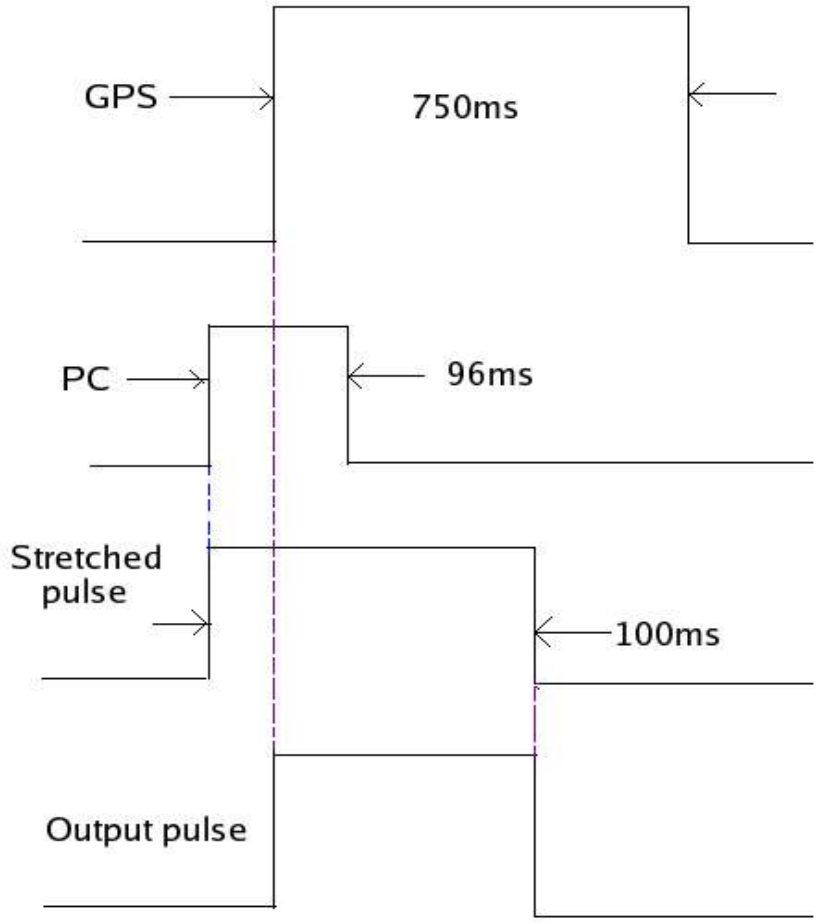


fig5.1

The above diagrams shows a schematic representation of the demo signals that we could generate from the MCM card. Over here the rising edge of the PC signal is delayed from the GPS signal by a certain amount and the PC signal falls before the fall of the GPS signal. The final output that have been obtained by AND ing the stretched PC signal and the GPS signal is perfectly synchronized with the rising edge of the GPS signal.

APPENDIX

(A)Datasheet of **DM74123**

DM74123
Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

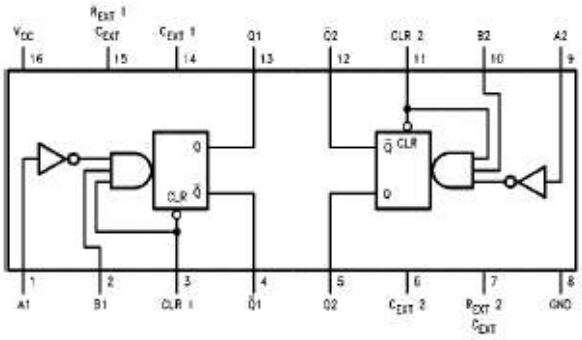
The DM74123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin (A) is an active-LOW transition trigger input and pin (B) is an active-HIGH transition trigger input. A LOW at the clear (CLR) input terminates the output pulse: which also inhibits triggering. An internal connection from CLR to the input gate makes it possible to trigger the circuit by a positive-going signal on CLR as shown in the Truth Table.

To obtain the best and trouble free operation from this device please read the Operating Rules as well as the One–Shot Application Notes carefully and observe recommendations.

Features

- DC triggered from active-HIGH transition or active-LOW transition inputs
- Retriggerable to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations
- DTL, TTL compatible
- Input clamp diodes

Connection Diagram



Triggering Truth Table

Inputs			Response
A	B	CLR	
X	X	L	No Trigger
↓	L	X	No Trigger
↓	H	H	Trigger
H	↑	X	No Trigger
L	↑	H	Trigger
L	H	↑	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-LOW transition or active-HIGH transition inputs or be reduced by use of the active-LOW transition clear input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current (Figure 1). However, its use in general is not recommended with retriggerable operation.
3. The output pulse width (T_W) for C_X > 1000 pF is defined as follows:

   $T_W = K R_X C_X(1 + 0.7/R_X)$

   1. where: [R_X is in Kilo-ohm]

      [C_X is in pico Farad]

      [T_W is in nano second]

      [$K \approx 0.28$]

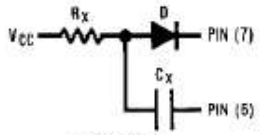


FIGURE 1.

4. For C_X < 1000 pF see Figure 2 for T_W vs. C_X family curves with R_X as a parameter:

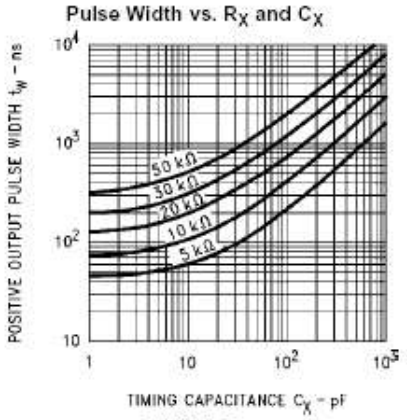
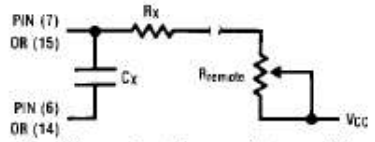


FIGURE 2.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



Note: "R_{remote}" should be as close to the one-shot as possible.

FIGURE 3.

6. The retriggerable pulse width is calculated as shown below:

   $T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$

   The retriggered pulse width is equal to the pulse width plus a delay time period (Figure 4).

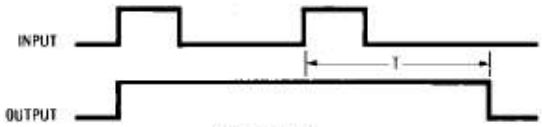


FIGURE 4.

7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

Note: For further detailed device characteristics and output performance please refer to the One-Shot Application Note, AN-366.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.8	mA
I_{OL}	LOW Level Output Current				16	mA
t_W	Pulse Width (Note 2)	A or B HIGH	40			ns
		A or B LOW	40			
		Clear LOW	40			
T_{WQ} (Min)	Minimum Width of Pulse at Q (Note 2)	A or B			65	ns
R_{EXT}	External Timing Resistor		5		50	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			µF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal (Note 2)				50	pF
T_A	Free Air Operating Temperature		0		70	°C

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.5	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.4V	Data			40	µA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)(Note 6)			46	66	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time.

Note 5: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs OPEN, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ K\Omega$.

Note 6: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs OPEN, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

(B) **Datasheet of IC 7408**

74AC08 • 74ACT08
Quad 2-Input AND Gate

General Description

The AC/ACT08 contains four, 2-input AND gates.

Features

- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24 mA

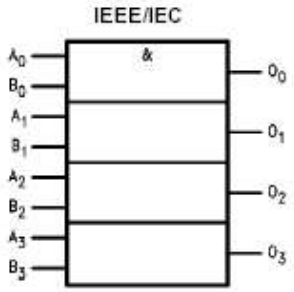
Ordering Code:

Order Number	Package Number	Package Description
74AC08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC08SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC08MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74AC08PC_NL (Note 1)	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT08SCX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT08MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT08PC_NL (Note 1)	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

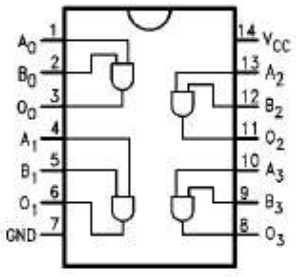
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Use this number to order device.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.46		$I_{OH} = -12$ mA
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 3)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.44		$I_{OL} = 12$ mA
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 3)
I_{IN} (Note 5)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 4)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.5	7.0	1.0	7.5	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

- **Picture of arrangement of signal generator using MCM card**