DESIGN AND REALIZATION OF CRYOGENICALLY COOLED SiGe BASED LOW NOISE AMPLIFIER

PROJECT REPORT

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CERTIFICATE

This is to certify that this project report entitled **DESIGN AND REALIZATION OF CRYOGENICALLY COOLED SiGe BASED LOW NOISE AMPLIFIER** is a bonafide record of work done by **Akshay Sharma and Gaurav Upadhyay** under my supervision at the **Giant Meterwave Radio Telescope – National Centre for Radio Astrophysics, Pune** from 07-02-2011 to 01-06-2011, in partial fulfillment of the requirements for the award of degree of **Bachelor of Technology** of the **Indian Institute of Space Science and Technology, Thiruvananthapuram**.

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ABSTRACT

Low noise amplifier is an essential component of a radio telescope. The noise performance of this amplifier governs the overall noise figure of the sensitive receiver system of the radio telescope. Low noise amplifiers (LNA) have always employed the most advanced technology such as InP(Indium Phosphide) and GaAs HEMTs (High Electron Mobility Transistor) and SiGe HBT (Heterojunction bipolar transistor). By cryogenically cooling these devices, very low noise temperature can be achieved over a long bandwidth. Although HEMTs can provide an excellent low noise performance at cryogenic temperatures, their performance is limited due to intrinsic transconductance fluctuations. On the other hand, bipolar devices do not suffer from this problem. Although their noise performance at room temperature is poor, these devices perform better than conventional HEMT LNAs when cooled to cryogenic temperatures. Over time Si-Ge bipolar transistors have improved considerably to compete with InP and GaAs HEMTs for cryogenic microwave Low Noise Amplifiers. Although SiGe based LNAs are common, little work has been done about their performance at cryogenic temperatures. The aim of this project is to realize a SiGe HBT and then study its characteristics at cryogenic temperatures. This project is aimed to verify this special property of SiGe transistor. This is done by realizing a working LNA, with given specifications and then testing and comparing its noise performance at different temperatures. In this report, we will discuss the theoretical background about SiGe HBTs and their expected performance at cryogenic temperatures. This will be followed by the design approach and strategy used to pursue the goals laid out for the project. This will include the simulation performed using various design environments like AWR's Microwave office and GENESYS by Agilent Technologies. The simulated values will be contrasted against the results obtained from testing the real LNA. The LNA is to be tested at room temperature first and then cooled to 77K using liquid nitrogen as a coolant medium. Allowing the device to gradually warm up will give us the valuable information about the behavior of device's Gain and noise temperature performance at different ambient temperatures. This information is collected and then processed to give out the curves and relations which show how ambient temperature affects the LNA performance parameters.

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LIST OF ABBREVIATIONS

AWR	Advanced Wave Research
BJT	Bipolar Junction Transistor
FET	Field Effect Transistor
GMRT	Giant Meterwave Radio Telescope
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
LNA	Low Noise Amplifier
NCRA	National Centre for Radio Astrophysics
NF	Noise Figure
NFA	Noise Figure Analyzer
SMART	Stretch Mesh Attached to Rope Trusses
VNA	Vector Network Analyzer

CHAPTER ONE

INTRODUCTION

1.1 ABOUT GMRT

GMRT (Giant meter-wave Radio Telescope) is a Radio Telescope consisting of 30 fully steerable parabolic dish antennas, each 45 m in diameter, installed across the region of about 25 km, near the village Khodad, Narayangaon Taluk, about 90 km north of Pune. It has been designed to operate at a range of frequencies form 30 MHz to 1450 MHz. The antennas have been constructed using a novel technique (nicknamed SMART) and their reflecting surface consists of panels of wire mesh. These panels are attached to rope trusses, and by appropriate tensioning of the wires, the desired parabolic shape is achieved.

GMRT is among the most powerful Radio Telescopes in the world at meter wavelengths, established for frontline research in Astronomy and Astrophysics. The number and configuration of the dishes was optimized to meet the principal astrophysical objectives which require sensitivity and high angular resolution as well as ability to image radio emission from diffused extended regions. Twelve of the thirty dishes are located more or less randomly in a compact central array in a region of about 1 sq km. The remaining eighteen dishes are spread out along the 3 arms of an approximately `Y'-shaped configuration over a much larger region, with the longest interferometric baseline of about 25 km.

Radio astronomy is the study of universe at radio wavelengths. The field of radio astronomy was started in 1923, when Karl Jansky discovered that his antenna was receiving radiation from outside the Earth's atmosphere. He noticed that this radiation appears at the same sidereal time on different days and that its source must hence lie far outside the solar system. Further observations enabled him to identify this radio source as the center of the galaxy.

The whole goal of the radio astronomy is to receive, process, and interpret the cosmic signals. Radio waves from the distant cosmic source received by the antenna create a fluctuating voltage at the antenna terminals. This voltage is first amplified by the front end (or RF) amplifier. The signal is weakest here, and hence it is very important that the amplifier introduce as little noise as possible. Front end amplifiers hence usually use low noise solid state devices to build the Low Noise Amplifiers (LNA). The LNAs are generally built using advanced technology devices like HEMTs (High Electron Mobility Transistors) and HBTs (Heterojunction Bipolar Transistors).

Giant Meter-wave Radio Telescope (GMRT) Front Ends have been designed to operate at 5 frequency bands centered at 50 MHz, 150 MHz, 235 MHz, 327 MHz, 610 MHz and L-Band extending from 1000 to 1450 MHz. The L-Band is split into four sub-bands centered at 1060 MHz, 1170 MHz, 1280 MHz and 1390 MHz, each with a bandwidth of 120 MHz. The 150 MHz, 235 MHz and 327 MHz bands have about 40 MHz bandwidth and the 610 MHz band has about 60 MHz bandwidth. The low noise front end of the receiving system of GMRT has been designed to receive dual polarization. Lower frequency bands from 150 to 610 MHz have dual circular polarization channels (Right Hand Circular and Left Hand Circular polarization) which have been conveniently named as CH1 and CH2, respectively.

CHAPTER TWO

OBJECTIVES

The aim of the project is to design a Low Noise Amplifier using SiGe Heterojunction Bipolar Transistor with following requirements:

1. LNA should have bandwidth wide enough to cover the range 500 MHz to 2000 MHz.

2. LNA should have noise temperature less than that of current HEMT LNA (35 K)

3. LNA should have following s- parameters

S_{21} (signifies gain)	>30 dB
S_{12} (return gain)	< -50dB
S_{11} (input return loss)	<-10dB
S_{22} (output return loss)	<-10dB.

4. Testing the above parameters and noise temperature at cryogenic temperature (77 K)

5. Recording the noise figure and gain at different temperatures. (Warming up phase)

CHAPTER THREE

THEORY

This section of the report will give the necessary theory required to understand the various concepts that are useful for a better understanding of the work done in the project. Since the performance parameters of the device are mentioned mainly in terms of S- parameters, a small introduction will refresh the memory.

3.1 S-PARAMETERS OF 2-PORT NETWORKS

An amplifier operating under linear (small signal) conditions is a good example of a non-reciprocal network and a matched attenuator is an example of a reciprocal network. In the following cases we will assume that the input and output connections are to ports 1 and 2 respectively which is the most common convention. The nominal system impedance, frequency and any other factors which may influence the device, such as temperature, must also be specified.

Complex linear gain

The complex linear gain G is given by

$$G = S_{21}.$$

That is simply the voltage gain as a linear ratio of the output voltage divided by the input voltage, all values expressed as complex quantities.

Scalar linear gain

The scalar linear gain (or linear gain magnitude) is given by

$$|G| = |S_{21}|.$$

That is simply the scalar voltage gain as a linear ratio of the output voltage and the input voltage. As this is a scalar quantity, the phase is not relevant in this case.

Scalar logarithmic gain

The scalar logarithmic (decibel or dB) expression for gain (g) is

$$g = 20\log_{10}|S_{21}| \text{ dB.}$$

This is more commonly used than scalar linear gain and a positive quantity is normally understood as simply a 'gain'. A negative quantity can be expressed as a 'negative gain' or more usually as a 'loss' equivalent to its magnitude in dB.

Insertion loss

In case the two measurement ports use the same reference impedance, the insertion loss (*IL*) is the dB expression of the transmission coefficient $|S_{21}|$. It is thus given by:

$$IL = -20\log_{10}|S_{21}| \text{ dB.}$$

Input return loss

Input return loss (RL_{in}) is a measure of the reflected energy from a transmitted signal. It is commonly expressed in positive dB's. The larger the value, the less energy that is reflected. When expressed in logarithmic magnitude, is given by

$$RL_{\text{in}} = |20\log_{10}|S_{11}|| \text{ dB.}$$

By definition, return loss is a positive scalar quantity implying the 2 pairs of magnitude (|) symbols. The linear part, $|S_{11}|$is equivalent to the reflected voltage magnitude divided by the incident voltage magnitude.

Output return loss

The output return loss (RL_{out}) has a similar definition to the input return loss but applies to the output port (port 2) instead of the input port. It is given by

$$RL_{\text{out}} = |20\log_{10}|S_{22}|| \text{ dB.}$$

Reverse gain and reverse isolation

The scalar logarithmic (decibel or dB) expression for reverse gain (g_{rev}) is:

$$g_{\text{rev}} = 20\log_{10}|S_{12}| \text{ dB.}$$

Often this will be expressed as reverse isolation (I_{rev}) in which case it becomes a positive quantity equal to the magnitude of g_{rev} and the expression becomes:

$$I_{\text{rev}} = |g_{\text{rev}}| = |20\log_{10}|S_{12}|| \text{ dB.}$$

3.2 STABILITY

When embarking on any amplifier design it is very important to spend time checking on the stability of the device chosen, otherwise the amplifier may well turn into an oscillator. The main way of determining the stability of a device is to calculate the Rollett's stability factor (K), which is calculated using a set of S-parameters for the device at the frequency of operation. The conditions of stability at a given frequency are $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$, and must hold for all possible values Γ_L & Γ_S obtained using passive matching circuits. We can calculate two Stability parameters K & $|\Delta|$ to give us an indication to whether a device is likely to oscillate or not or whether it is conditionally/unconditionally stable.

The K factor represents a quick check for stability at given frequency and given bias condition. Unconditional stability is the goal of LNA designer. Unconditional stability means that with any load presented to the input or output of the device, the circuit will not become unstable (will not oscillate). The stability of the LNA is characterized by Rollett Factor (K) which is given by

$$\text{If } \Delta = S11 * S22 - S21 * S12$$

Then

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 * |S_{21}| * |S_{12}|}$$

For unconditional stability K should be greater than one for the operating frequencies and in the frequencies where the circuit has substantial gain.

Using AWR Design Environment, K factor stability can be calculated easily and can be represented in the graph. Figure 4.9 shows the K factor for the range of operating frequency. As we can see from the graph, the K factor is greater than 2 for the frequency range. Which implies that amplifier is stable and won't go into oscillation.

3.3 DEVICE PHYSICS

This section of report will deal with the physics behind Si-Ge Heterojunction Bipolar Transistors and will establish the reason of their better performance as compared to traditional bipolar junction transistor. Later in the section, changes that occur in physical properties of a HBT with change in temperature will be discussed.

3.3.1 BIPOLAR JUNCTION TRANSISTOR

The device consists of a pair of p-n junctions that have been stacked together such that they are sharing a single p-doped region. The doping of the devices is such that one of the n-doped regions, called the emitter, is very heavily doped whereas the other n-doped region, called the collector, is only moderately doped. Finally, the p-doped region in the center of the device is called the base, and is doped at an intermediate level.

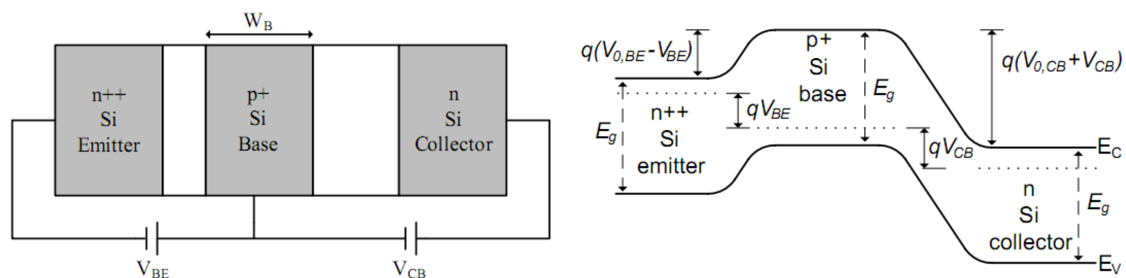


Fig. 3.1 Basic BJT structure and energy band diagram

The operation of a bipolar device under forward active operation can be understood conceptually by studying the energy band diagram shown above. The emitter region is heavily doped meaning that there are a large number of ionized impurities, leading to a large number of electrons in the conduction band. Thus, there will be a diffusion current of electrons injected from the emitter to the base with magnitude equal to the number of electrons that have enough thermal energy to overcome the base–emitter electrostatic-potential-barrier which has height equal to $q\left(V_{0,BE} - V_{BE}\right)$.

If the base is sufficiently short, we can neglect recombination in the base and assume that all of the electrons that diffuse into the base are swept into the collector via the electric field across the collector-base junction. Thus, as the distribution of thermal energy among the electrons in the conduction band is approximately Boltzmann distributed the collector current density is exponentially dependent on the barrier height.

$$J_C \approx \frac{kT_a \mu_{nb} n_{io}^2}{W_B N_{AB}^-} e^{qV_{BE}/kT_a} = N_{DE}^+ \frac{kT_a \mu_{nb}}{W_B} e^{-q(V_{0,BE} - V_{BE})/kT_a},$$

……….1

Where μ_{nb} is the minority carrier mobility in the base of the transistor. Similarly, due to the base doping level, there will be a large number of ionized acceptor impurities in the base valence band leading to a diffusion current of holes from the base to the emitter. Once again ignoring recombination current in the base, the base current density can be written as

$$J_B \approx \frac{kT_a \mu_{pe} n_{io}^2}{L_{PE} N_{DE}^+} e^{qV_{BE}/kT_a} = N_{AB}^- \frac{kT_a \mu_{pe}}{L_{PE}} e^{-q(V_{0,BE} - V_{BE})/kT_a},$$

……..….2

Where μ_{pe} and L_{PE} are the hole mobility and diffusion length in the emitter. Thus, for a standard

npn bipolar transistor, the dc current gain is approximated as:

$$\beta_{DC} \equiv \frac{J_C}{J_B} \approx \frac{\mu_{nb}}{\mu_{pe}} \frac{L_{PE}}{W_B} \frac{N_{DE}^+}{N_{AB}^-},$$

…………………….…………………….3

Where W_B is the base width and L_{PE} is the diffusion length for holes injected into the emitter referring to equation 3 β_{DC} is determined by three ratios:

1) μ_n/μ_p. As mobility is a material property, it is assumed that this is not a tunable parameter for standard bipolar devices. Usually = 2.8 for low doping region.

2) L_{PE}/W_B. This ratio tends to increase with technology node, but otherwise cannot be easily engineered.

3) N_{DE}/N_{AB}. The emitters of modern silicon bipolar transistors are formed by depositing a layer of n-doped Polysilicon layer on top of the base layer and then performing diffusion through an annealing step to form an n-doped single crystal layer between the deposited Polysilicon layer and the base. Thus, the doping level in the emitter is not easily tuned. On the other hand, controlling the base doping is possible. Therefore, this ratio can be controlled. But increasing this ratio will increase the sheet resistance of the device so we have to tradeoff between the DC-Gain and resistance.

3.3.2 Si-Ge HETEROJUNCTION BIPOLAR TRANSISTORS

As discussed above, a fundamental shortcoming of Si bipolar transistors is the inherent tradeoff that must be made between the dc current gain and the base resistance. Increasing β_{DC} requires reducing N_{AB}, which in turn increases the base resistance. As it turns out, one can circumvent this limitation by introducing Ge into the base material. If the emitter material were to have a wider bandgap than the base material, the result would be that minority carriers injected from the emitter to the base would see a smaller barrier than the minority carriers back injected from the base to the emitter, resulting in an exponential increase in β_{DC} if the difference in the emitter and base bandgaps is ΔE_g eV, then the value of β_{DC} for a device with a wide-bandgap emitter will be a factor of $e^{\Delta Eg /kTa}$ times larger than that of a identically doped device without a wide-bandgap emitter. The bandgap of Ge is 0.67 eV, which is significantly less than 1.11 eV (the bandgap of silicon). Thus, by introducing a small amount of Ge to the base, it is possible to reduce the bandgap in the alloy considerably from that of pure silicon. Furthermore, by grating the Ge content as a function of depth into the base, the bandgap can be reduced along the base, resulting in the reduction of transit time

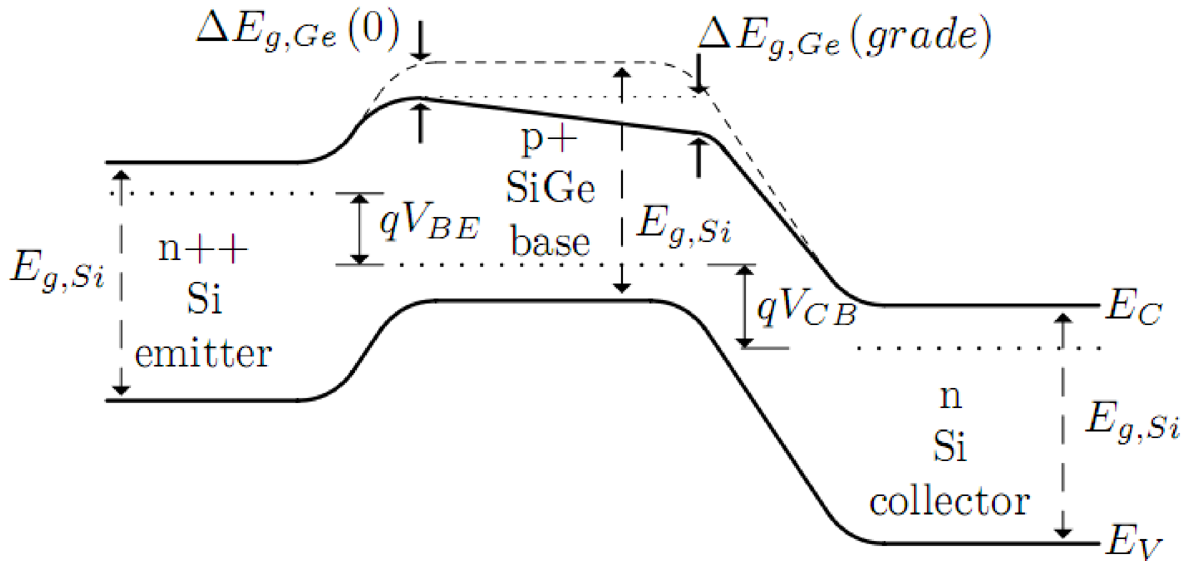


Fig. 3.2 Energy band diagram for Si Ge HBT.

The collector current density of a SiGe HBT is given as

$$J_C \approx n_{io,Si}^2 \tilde{\gamma}\tilde{\eta} \frac{\mu_{nb,Si}}{N_{AB}^- W_b} \Delta E_g\,(grade) e^{\Delta E_g^{app}/kT_a} e^{\Delta E_{g,Ge}(0)/kT_a} \left(e^{qV_{BE}/kT_a} - 1\right)$$

……4

Where $\eta = (\mu_{nb})_{SiGe} / (\mu_{nb})_{Si} > 1$, $\gamma = (N_C N_V)_{SiGe} / (N_C N_V)_{Si} < 1$

The base current of a SiGe HBT is the same as that of an identically doped silicon BJT and can be written as:

$$J_B \approx \frac{kT_a \mu_{pe} n_{io}^2}{L_{PE} N_{DE}^+} e^{qV_{BE}/kT_a} = \frac{q}{G_e} e^{qV_{BE}/kT_a},$$

…………………………………………5

Where $Ge = N^+_{DE} \; L_{PE}/D_{PE}\, n^2_{io,e}$

Thus, the dc current gain of a SiGe HBT can be written as:

$$\beta_{DC} \approx \frac{\mu_{nb,Si} L_{pe} N_{DE}^{+}}{\mu_{pe} W_B N_{AB}^{-}} \widetilde{\gamma}\widetilde{\eta} \frac{\Delta E_g, Ge\,(grade)}{kT_a} e^{\Delta E_{g,app}/kT_a} e^{\Delta E_g(0)/kT_a}$$

$$= \beta_{DC,Si} \left(\widetilde{\gamma}\widetilde{\eta} \frac{\Delta E_g, Ge\,(grade)}{kT_a} e^{\Delta E_{g,app}/kT_a} e^{\Delta E_g(0)/kT_a} \right).$$

…………6

In order to evaluate equation 6 it is necessary to know the appropriate expressions for the apparent- and Ge-induced bandgap narrowing. The Ge induced bandgap reduction for a compressively strained SiGe film at room temperature can be estimated as a function of the Ge content, x, as

$$\Delta E_{g,Ge} \approx 0.96x - 0.43x^2 + 0.17x^3,$$ ………………………………7

and the room temperature value of $\Delta E_{g,app}$ can be estimated as a function of dopant concentration as

$$\Delta E_{g,app} \approx 18 \times 10^{-3} \ln \left\{ \frac{N_{AB}^{-}}{N_{DE}^{+}} \right\}.$$ ………………………………………8

Using equations 6, 7 and 8and assuming that γ and η are close to unity, we can quickly estimate the effect of the Ge content on β. For instance, for the case in which $N^{-}_{AB} = 5 \times 1018$ cm^{-3}, $N^{+}_{DE} = 1020$ cm^{-3}, the Ge content is 20% at the emitter side of the base, and there is a 10% Ge grating, then an improvement of over 400 in the dc current gain is obtained. It is clear that introduction of Ge into the base of a bipolar transistor affects the dc current gain quite favorably.

3.4 PERFORMANCE OF SiGe TRANSISTORS AT CRYOGENIC TEMPERATURES

The operating characteristics of SiGe transistors are tightly coupled to the underlying material properties. In order to understand the operation of SiGe devices at cryogenic temperatures, it is therefore necessary to study the temperature dependence of the physical properties of Si materials as well as those of SiGe alloys

3.4.1 PROPERTIES OF SILICON AT CRYOGENIC TEMPERATURES

Bandgap: Intrinsic Si

Understanding the temperature dependence of the bandgap of intrinsic silicon material is extremely important, as the diffusion currents in a bipolar device are exponentially related to Eg. Bandgap and temperature don't follow an exclusive relation from theory, but a high order polynomial can be fitted to the experimental values. This gives the relation:

$$E_g \approx 1.17 + 5.65 \times 10^{-6} T_a - 5.11 \times 10^{-7} T_a^2 - 8.03 \times 10^{-10} T_a^3 + 2.50 \times 10^{-12} T_a^4$$

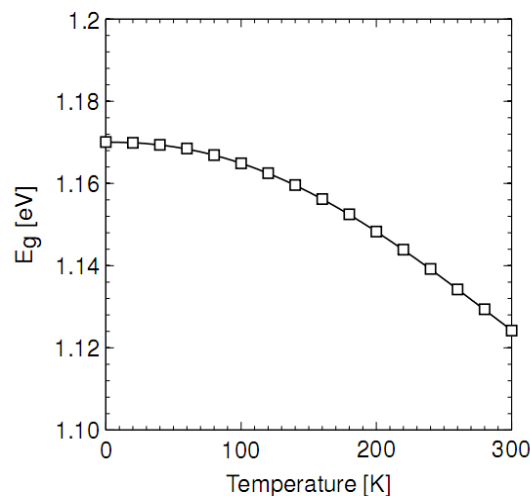


Fig. 3.3 Bandgap Vs ambient temperature. Squares represent experimental data and solid curve is the polynomial fit.

Carrier Concentration: Intrinsic Si

The intrinsic carrier concentration is given by the well-known formula

$$n_{io} = \sqrt{N_C N_V}\, e^{-E_g/2kT_a}, \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 9$$

Where

$$N_C \equiv 2\left(\frac{2\pi m_{de}^{*} k T_a}{h^2}\right)^{3/2} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 10$$

And

$$N_V \equiv 2\left(\frac{2\pi m_{dh}^{*} k T_a}{h^2}\right)^{3/2}. \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 11$$

Thus

$$n_{io} \approx 4.82e15 T_a^{3/2} \sqrt{6\frac{m_t^*}{m_0}\sqrt{\frac{m_l^*}{m_0}}\left[\left(\frac{m_{lh}^*}{m_0}\right)^{3/2} + \left(\frac{m_{hh}^*}{m_0}\right)^{3/2} + \left(\frac{m_{soh}^*}{m_0}\right)^{3/2}\right]}\, e^{-E_g/2kT_a}. \qquad \ldots\ldots 12$$

The intrinsic carrier concentration is exponentially proportional to temperature via the energy bandgap and linearly related to $T^{3/2}$a and the effective masses. As the effective masses were shown to be only weakly temperature dependent, the conclusion is that n_{io} goes as roughly $T^{3/2}_a$ exp $\{-Eg (T_a) /2kT_a\}$.

Carrier Mobility

Carrier mobility is an important consideration as it determines the effective velocity of carriers under the influence of electric fields. Mobility is directly related to scattering mechanisms, which include scattering due to lattice vibrations or phonons (μ_{ps}), ionized impurities (μ_{ii}), velocity saturation (μ_{vs}), carrier-to-carrier collisions (μ_{cc}), and neutral impurities (μ_{ni}). Of these mechanisms, μ_{vs}, μ_{cc}, and μ_{ni} are independent whereas μ_{ps} and μ_{ii} are coupled to each other. Thus the total electron or hole mobility can be obtained by considering each of the effects in parallel as:

$$\mu = \left(\frac{1}{\mu_{psii}} + \frac{1}{\mu_{vs}} + \frac{1}{\mu_{cc}} + \frac{1}{\mu_{ni}} \right)^{-1}$$

……………………………………………13

Where μ_{psii} is the mobility considering only phonon and ionized impurity scattering. As evidenced by equation.

3.4.2 PROPERTIES OF SiGe TRANSISTORS AT CRYOGENIC TEMPERATURES

Doping-Induced Apparent Bandgap Narrowing

The collector current in a SiGe HBT depends upon the apparent bandgap narrowing which can be written

$$\Delta E_{g,app} \approx 18.7 \times 10^{-3} \ln \left\{ \frac{N_{AB}^{-}}{N_{DE}^{+}} \right\}.$$

……………………………………………14

and occurs due to heavy doping in the base and emitter. As $\Delta E_{app,g}$ depends on the natural logarithm of the ratio of ionized impurities in the base to that in the emitter, the net effect is that the bandgap actually looks wider in terms of the barrier that the electrons being injected into the base must overcome. Furthermore, since this is a bandgap effect, it is exponentially enhanced with decreasing temperature. As it turns out, this, as opposed to carrier freeze-out, is actually the limiting factor in the operation of modern silicon BJTs at cryogenic temperatures [30]. Fortunately, the bandgap narrowing that the Ge induces is sufficient to

compensate out the apparent bandgap narrowing. Nevertheless, it offsets the effect of the Ge and, in the case of a triangular Ge profile (i.e., no Ge content on the base side of the base–emitter depletion region), it is a limiting effect.

DC Terminal Currents

Base Current

From equation 5 the base current can be written as

$$J_B(T_a) \approx \frac{kT_a \mu_{pe}(T_a)\, n_{io}^2(T_a)}{L_{PE}(T_a)\, N_{DE}^+(T_a)} e^{qV_{BE}/kT_a} = J_{B0}(T_a)\, e^{qV_{BE}/V_T}.$$

……………………...15

Of particular interest is the change in base saturation current, JB_0, with cooling. The fractional change in base saturation current with cooling from 300 K can be written as

$$\frac{J_{B0}(T_a)}{J_{B0}(300)} = \left(\frac{T_a}{300}\right)^4 \left(\frac{\mu_{pe}(T_a)}{\mu_{pe}(300)}\right) \left(\frac{L_{PE}(300)\, N_{DE}^+(300)}{L_{PE}(T_a)\, N_{DE}^+(T_a)}\right) \frac{e^{-E_g(T_a)/kT_a}}{e^{-E_g(300)/(k300)}}.$$

………..16

In order to arrive at an explicit temperature dependence for J_{B0}, it is necessary to write the temperature dependences of μ_{pe}, L_{PE}, N^+_{DE}, and Eg. μ_{pe} can be assumed to be only weakly temperature dependent. N^+_{DE} is nearly independent of ambient temperature. since N^+_{DE} is nearly independent of temperature and μ_{pe} is only weakly dependent on temperature, a reasonable approximation is that L_{PE} (Ta) ∝ √Ta. And the bandgap can be written as a function of temperature as $Eg \approx 1.17 + 5.65 \times 10^{-6} T_a - 5.11 \times 10^{-7} T_a^2 - 8.03 \times 10^{-10} T_a^3 + 2.50 \times 10^{-12} T_a^4$

Thus, equation16 can be rewritten as:

$$\frac{J_{B0}(T_a)}{J_{B0}(300)} = 7.83 \times 10^{18} \left(\frac{T_a}{300}\right)^{7/2} e^{-E_g(T_a)/kT_a}.$$

…………………………..17

Collector Current

The same procedure can be repeated for the collector current saturation coefficient, JC0, in order to determine its temperature dependency. The value of JC0 (Ta) normalized to JC0 (TRT) is given as

$$\frac{J_{C0}(T_a)}{J_{C0}(300)} \approx \left(\frac{T_a}{300\ K}\right)^3 \frac{\tilde{\gamma}(T_a)}{\tilde{\gamma}(300)} \frac{\tilde{\eta}(T_a)}{\tilde{\eta}(300)} \frac{\mu_{nb,Si}(T_a)}{\mu_{nb,Si}(300)} \frac{N_{AB}^{-}(300)}{N_{AB}^{-}(T_a)} \frac{e^{E_g(300)/k300}}{e^{E_g(T_a)/kT_a}} \frac{e^{\Delta E_{g,app}/kT_a}}{e^{\Delta E_{g,app}/k300}} \frac{e^{\Delta E_{g,Ge}(0)/kT_a}}{e^{\Delta E_{g,Ge}(0)/k300}}.$$

………….18

Since e $\gamma = \mu nb,SiGe/\mu nb,Si$, its value is assumed to be temperature independent. $\eta = (N_C N_V)_{SiGe} / (N_C N_V)_{Si}$ is assumed to be only weakly temperature dependent [90]. Thus, it will be considered constant as a function of temperature. As discussed above, the mobilities are not strongly dependent upon temperature as the doping level in the base is quite high. Thus, assuming the base is doped well above the Mott transition, equation 17 can be simplified to

$$\frac{J_{C0}(T_a)}{J_{C0}(300)} \approx 7.83 \times 10^{18} \left(\frac{T_a}{300}\right)^3 e^{-E_g(T_a)/kT_a} \frac{e^{(\Delta E_{g,app}+\Delta E_{g,Ge}(0))/kT_a}}{e^{(\Delta E_{g,app}+\Delta E_{g,Ge}(0))/k300}}.$$

……..19

DC Current Gain

βDC is critical in determining the low-GHz range noise performance of modern SiGe bipolar transistors. The temperature dependence of βDC can be evaluated by taking the ratio of equation 17 to equation 19

$$\frac{\beta_{DC}(T_a)}{\beta_{DC}(300)} \approx \sqrt{\frac{300}{T_a}} \frac{e^{\Delta E_{g,app}+\Delta E_{g,Ge}(0)/kT_a}}{e^{\Delta E_{g,app}+\Delta E_{g,Ge}(0)/k300}}.$$

………………………………..20

Therefore, the dc current gain is exponentially enhanced by cooling provided that $\Delta E_{g,app} + \Delta E_{g,Ge}(0) > 0$. Furthermore, as the enhancement is related to the Ge concentration at the edge of the base–emitter space charge region, this effect is expected to vary greatly among various SiGe HBT technology platforms.

Noise Figure

Noise figure of the device decreases with decrease in ambient temperature. The three noise parameters that decide noise figure are Fmin, Zopt and Rn.

Fmin is here expressed as Tmin. The two are related as

$$T_e = T_o(F-1) \qquad \text{.....21}$$

Where To is 290 K.

Derivation of the Noise parameters can be found in reference 1 of the report. Here we are mentioning the final approximate values of the parameters to give a basic understanding of dependence of noise parameters on temperature.

$$T_{MIN,LF} \approx T_a \frac{n_{cx}}{\sqrt{\beta_{DC}}}, \qquad \text{.....22}$$

$$R_{OPT,LF} \approx \frac{\sqrt{\beta_{DC}}}{G_m}, \qquad \text{.....23}$$

$$X_{OPT,LF} \approx 0 \qquad \text{.....24}$$

$$R_{n,LF} \approx \frac{T_a}{T_0} \frac{n_{cx}}{2G_m} \qquad \text{.....25}$$

Where

$n_c = I_C/g_m V_T$ and

$G_m = g_m/(1 + g_m r_e)$

As we have seen earlier, DC gain of the device increases with decrease in temperature. Therefore Tmin decreases with decrease in temperature directly as well as because of DC current gain. Noise parameters of a SiGe HBTare completely determined by its extrinsic

transconductance Gm, extrinsic collector current ideality factor, ncx, and dc current gain, β_{DC}.So noise figure can be approximated to

$$N_{LF} \approx \frac{T_{min,LF}}{2T_0}. \qquad \ldots\ldots\ldots\ldots 26$$

3.5 MICROSTRIP THEORY

Microstrip is a type of electrical transmission line which can be fabricated using printed circuit board (PCB) technology, and is used to convey microwave-frequency signals. It consists of a conducting strip separated from a ground plane by a dielectric layer known as the substrate. Microwave components such as antennas, couplers, filters, power dividers etc. can be formed from microstrip, the entire device existing as the pattern of metallization on the substrate. Microstrip is thus much less expensive than traditional waveguide technology, as well as being far lighter and more compact.

The disadvantages of microstrip compared with waveguide are the generally lower power handling capacity, and higher losses. Also, unlike waveguide, microstrip is not enclosed, and is therefore susceptible to cross-talk and unintentional radiation.

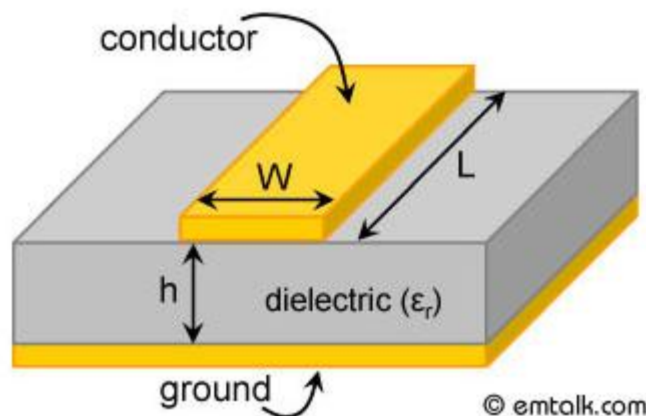


Fig. 3.4 A typical Microstrip

A closed-form approximate expression for the quasi- static characteristic impedance of a microstrip line was developed by Wheeler:

$$Z_{\text{microstrip}} = \frac{Z_0}{2\pi\sqrt{2(1+\varepsilon_r)}}\ln\left(1+\frac{4h}{w_{\text{eff}}}\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{w_{\text{eff}}}+\sqrt{\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{w_{\text{eff}}}\right)^2+\pi^2\frac{1+\frac{1}{\varepsilon_r}}{2}}\right)\right)$$

where w_{eff} is the *effective width*, which is the actual width of the strip, plus a correction to account for the non-zero thickness of the metallization. The effective width is given by

$$w_{\rm eff} = w + t\frac{1+\frac{1}{\varepsilon_r}}{2\pi}\ln\left(\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2+\left(\frac{1}{\pi}\frac{1}{\frac{w}{t}+\frac{11}{10}}\right)^2}}\right)$$

with

Z_0 = impedance of free space,

ε_r = dielectric constant of substrate,

w = width of strip,

h = thickness ('height') of substrate and

t = thickness of strip metallization.

Effective dielectric constant

As a part of the fields from the microstrip conductor exist in air, the effective dielectric constant ε_e is somewhat less than the substrate's dielectric constant (ε_r). The effective dielectric constant ε_e of microstrip is calculated by:

$$when\ \left(\frac{W}{H}\right) < 1$$

$$\varepsilon_e = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left[\left(1+12\left(\frac{H}{W}\right)\right)^{-1/2}+0.04\left(1-\left(\frac{W}{H}\right)\right)^2\right]$$

$$when\ \left(\frac{W}{H}\right) \geq 1$$

$$\varepsilon_e = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left(1+12\left(\frac{H}{W}\right)\right)^{-1/2}$$

After using this equation the width of microstrip line was calculated with the help of data from the data sheet.

3.6 TOOLS AND EQUIPMENTS USED

In the project we have used a number of tools to realize the final design and test its validity. These tools include various softwares used to simulate and design the circuit and analyzers to test the final device. A brief description of these tools and equipments are highlighted in this section.

3.6.1 AWR'S MICROWAVE OFFICE

AWR'S Microwave office is the main simulation and circuit development environment we have used. Some of its features are listed here.

- Microwave Office by AWR (Applied Wave Research, USA)
- Can be used to design circuits composed of schematics and electromagnetic (EM) structures
- Generate layout representations
- Can perform simulations using AWR's simulation engines
- Can tune or optimize the designs and changes are automatically and immediately reflected in the layout

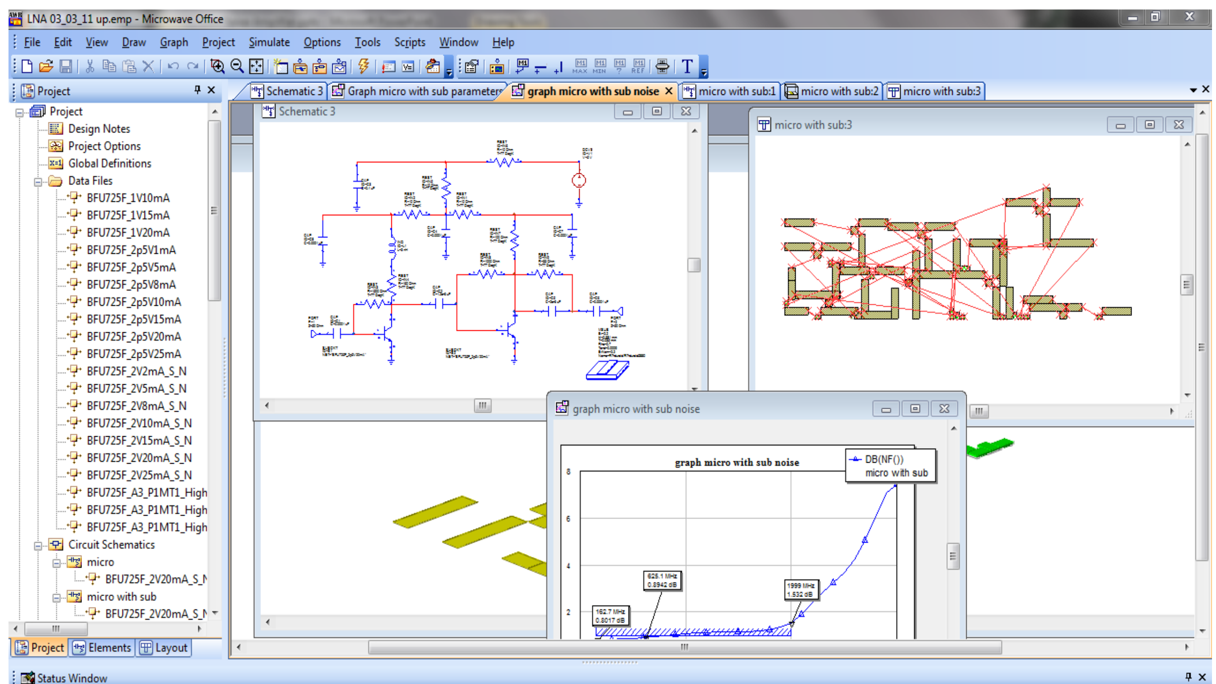


Fig. 3.5 A snapshot of AWR

3.6.2 GENESYS FROM AGILENT TECHNOLOGIES

GENESYS is an excellent tool for preparation of layout. After reaching the layout stage in our design the layout was finally prepared and edited with the help of GENESYS. Some of its features are listed below.

- Create layout from schematic, imported artwork, or direct drawing for EM simulation and board fabrication
- 3D viewer for layout with interactive rotation, zoom, vertical stretching, and cut planes to verify correct geometry before fabrication
- Very easy to use layout functionality.
- Full library of pad/package layout footprints
- Import /export masks and drill files in popular printed circuit board (PCB) formats (e.g., Gerber, DXF/DWG, and GDSII) for PCB board realization on fast prototyping machines or chemical etching.

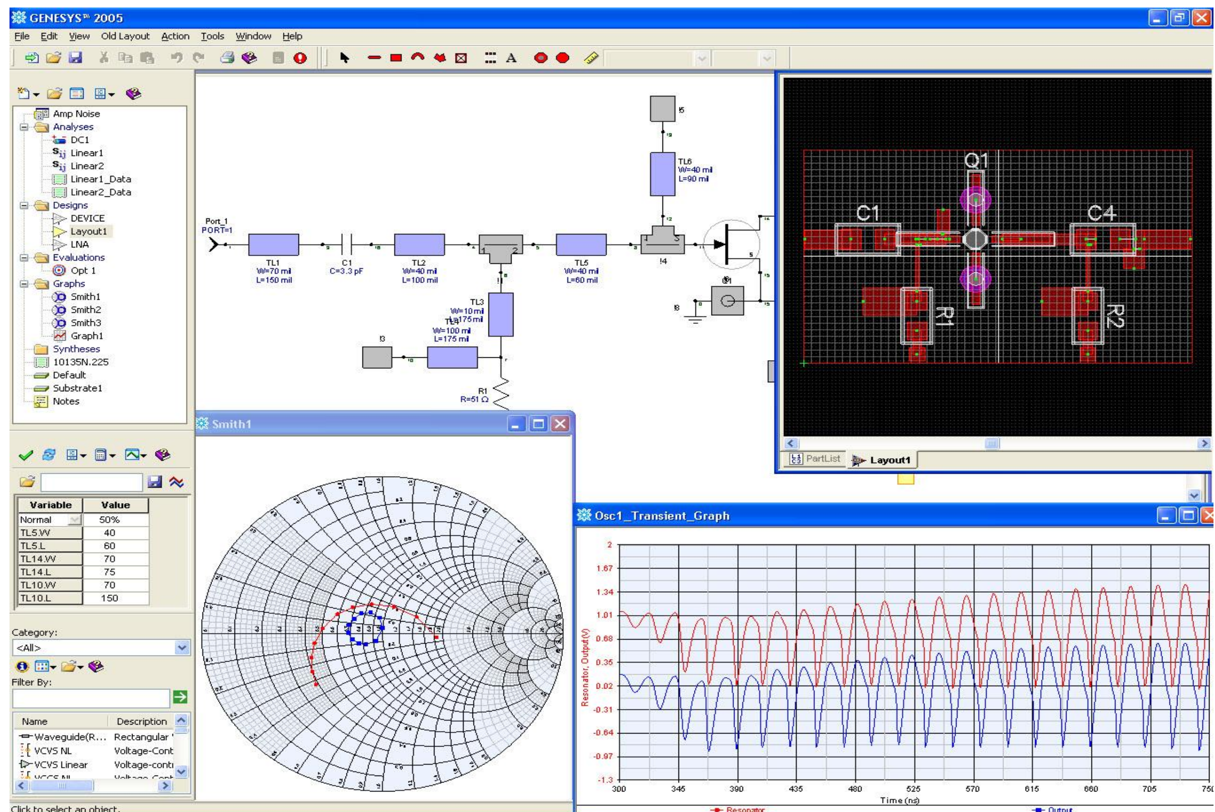


Fig. 3.6 A snapshot of GENESYS

3.6.3 NOISE FIGURE ANALYZER

The noise figure analyzer represents the most recent evolution of noise figure measurement solutions. A noise figure analyzer in its most basic form consists of a receiver with an accurate power detector and a circuit to power the noise source. It provides for ENR entry and displays the resulting noise figure value corresponding to the frequency it is tuned to.

A noise figure analyzer allows the display of swept frequency noise figure and gain and associated features such as markers and limit lines. The Agilent NFA series noise figure analyzers combined with the SNS-Series noise sources offer improvements in accuracy and measurement speed, important factors in manufacturing environments. The NFA is specifically designed and optimized for one purpose: to make noise figure measurements.

We used Agilent N8973A for Noise Figure Analysis.

Fig. 3.7 Agilent N897A Noise Figure Analyzer

Some features of Agilent N8973A:

- The Agilent N8973A is a high performance noise figure analyzer designed to make fast, accurate and repeatable noise figure measurement.
- With the N8973A ease of use features, we can set up complex measurements simply and easily.

- The N8973A offers simultaneous noise figure and gain measurements with the ability to view, print and save the data/display in multiple formats.
- The N8973A offers increased measurement accuracy and faster measurement speed over previous Agilent noise figure meters, as well as six user selectable measurement bandwidths.

Calibration of Noise Figure Analyzer

Noise figure measurements rely on a calibrated noise source as a reference. The general measurement process is shown in the figures below. In Figure 1, the noise source is connected directly to the input of the measuring instrument and a user calibration is performed. This measures and stores the instrument's own noise figure at its various attenuator settings. These results are used to remove the effect of "second-stage" noise contribution during a corrected measurement.

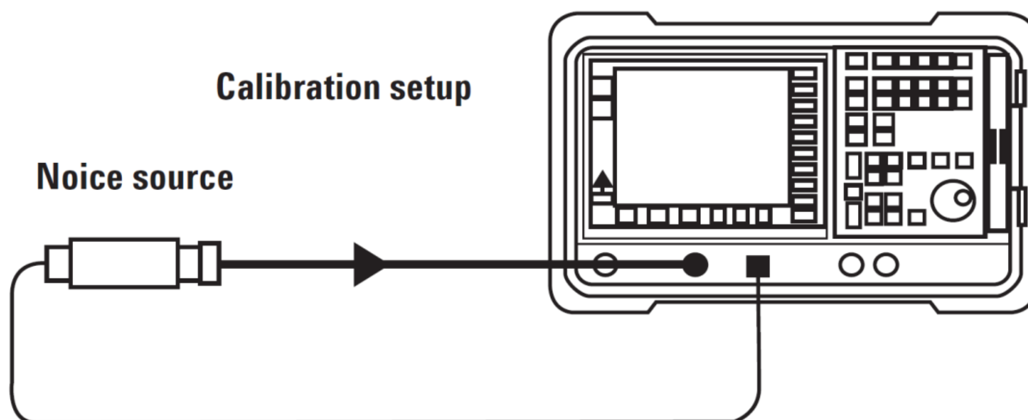


Fig. 3.8 Calibration Setup

The measurement arrangement, with the device-under-test (DUT) inserted between the noise source and the instrument is shown in Figure 2.

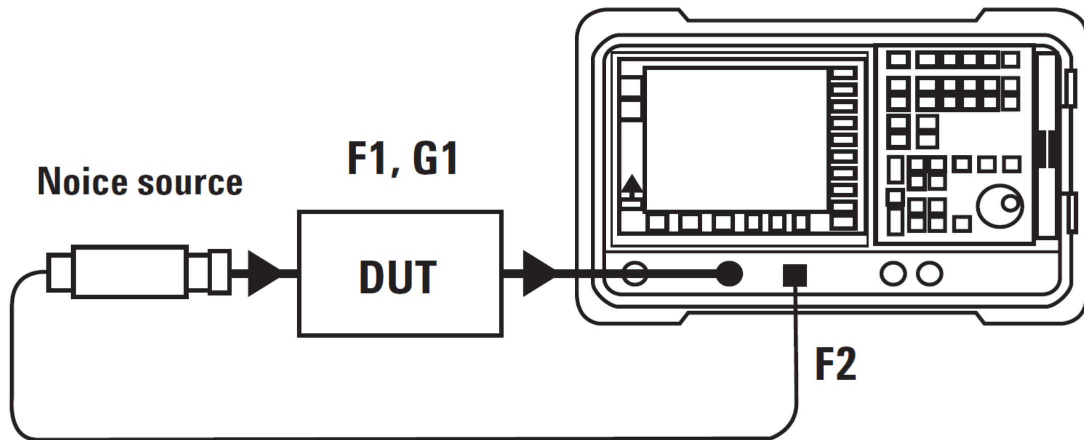


Fig. 3.9 General Noise Figure test setup

Immediately after calibration, the noise source is still connected directly to the instrument, which automatically switches to the corrected measurement mode. In this configuration the instrument would be expected to display a noise figure and gain of 0 dB, because there is no DUT present. In practice however, the instrument may show a noise figure of plus or minus a few tenths of a dB as well as an even lower level of gain, but not zero.

Noise source

To make noise figure measurements a noise source must have a calibrated output noise level, represented by excess noise ratio (ENR). Unique ENR calibration information is supplied with the noise source.

We used noise source NC348A for the calibration.

Loss compensation

To make the experiment and measurement more reliable and accurate we also compensated for the connecting RF Coaxial cables. Each Connecting cable was first analyzed with the help of Network analyzer and their insertion loss values were recorded. These values were then duly noted and compensated for in the actual experiment. Files for the connector's loss were added in the NFA and their loss was compensated by using the Loss Compensation tool of the NFA.

3.6.4 NETWORK ANALYZER

A network analyzer is an instrument that measures the network parameters of electrical networks. Today, network analyzers commonly measure S–parameters because reflection and transmission of electrical networks are easy to measure at high frequencies. They can offer other measurements commonly associated with devices: such as gain and match. Network analyzers do not, by themselves, provide measurement of the noise parameters. The measurement of noise parameters generally requires a tuner and software in addition to the network analyzer. The resulting measurement system can be complex and expensive. Network analyzers are often used to characterize two-port networks such as amplifiers and filters.

We used Agilent E5070B Network Analyzer

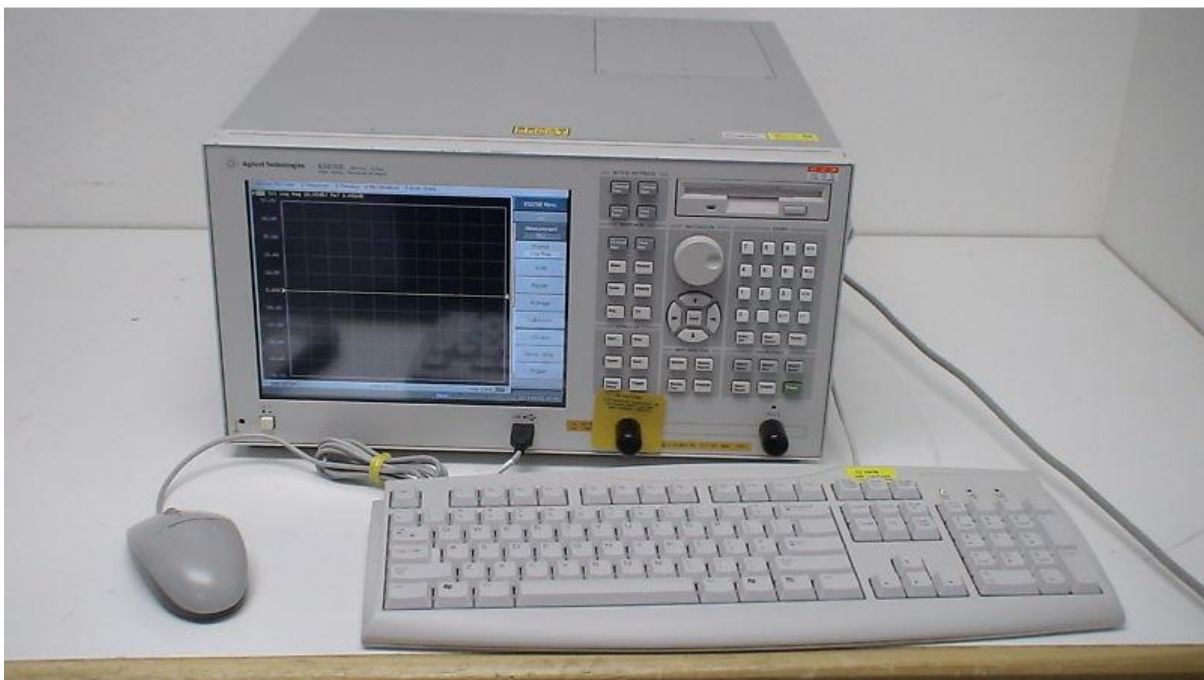


Fig. 3.10 Agilent E5070B Network Analyzer

Calibration of Network Analyzer

The accuracy and repeatability of measurements can be improved with calibration. Calibration involves measuring known standards and using those measurements to compensate for systematic errors. After making these measurements, the network analyzer

can compute some correction values to produce the expected answer. For answers that are supposed to be zero, the analyzer can subtract the residual. For non-zero values, the analyzer could calculate complex factors that will compensate for both phase and amplitude errors. Calibrations can be simple (such as compensating for transmission line length) or involved methods that compensate for losses, mismatches, and feedthroughs.

A network analyzer (or its test set) will have connectors on its front panel, but the measurements are seldom made at the front panel. Usually some test cables will go from the front panel to the device under test (DUT) such as a two-port filter or amplifier. The length of those cables will introduce a time delay and corresponding phase shift; the cables may also introduce some attenuation (affecting SNA and VNA measurements).

CHAPTER FOUR

LNA DESIGN METHODOLOGY

4.1 CIRCUIT CONSTRUCTION

This section of the report illustrates the steps taken to realize the LNA with the goals specified in the objectives section. The methodology is simply the steps taken by us and is not standard steps to realize a LNA. The most basic step to start the design of an amplifier is to choose the transistor to be used in the circuit. Our design uses a SiGe Transistor NXP BFU725F, whose datasheet is given in Appendix 1. SiGe transistors are not easily available in the Indian market and the choice parameters include performance, cost and availability factors. Next we require a design environment to test and simulate our LNA before realizing it and predict its performance. AWR's(Applied Wave Research) Microwave Office is used as Design Environment for developing and simulation of the circuit. AWR's basic features and advantages are mentioned in section 3.6.1. AWR is not the best Design environment when it comes to layout editing. Therefore GENESYS is used for this purpose. More information about GENESYS is provided in section 3.6.2.

The basic schematic of the LNA is given below in figure 4.1. The circuit employs two NXP BFU725F transistors (S1 and S2), both with collector feedback bias configuration. The two stages are connected with a coupling capacitor C2. Coupling capacitor also serves as a high pass filter and flattens the gain curve. It is usually necessary to implement a small bypass capacitor, say 100pF (C4, C3 and C7) near the transistor for microwave frequencies and large capacitor, say 0.1 µF further away for the lower frequency radio frequency interference and static protection.

The path length between two capacitors provides an inductance, which can result in a high impedance and circuit instability (i.e. between C3 and C4; and C4 and C7). Small resistors (IN6 and IN7) are thus utilized between the capacitors to dampen this resonance. C7 and C6 are decoupling capacitors. Resistor IN9 and capacitor C5 forms a feedback system to stabilize the output voltage.

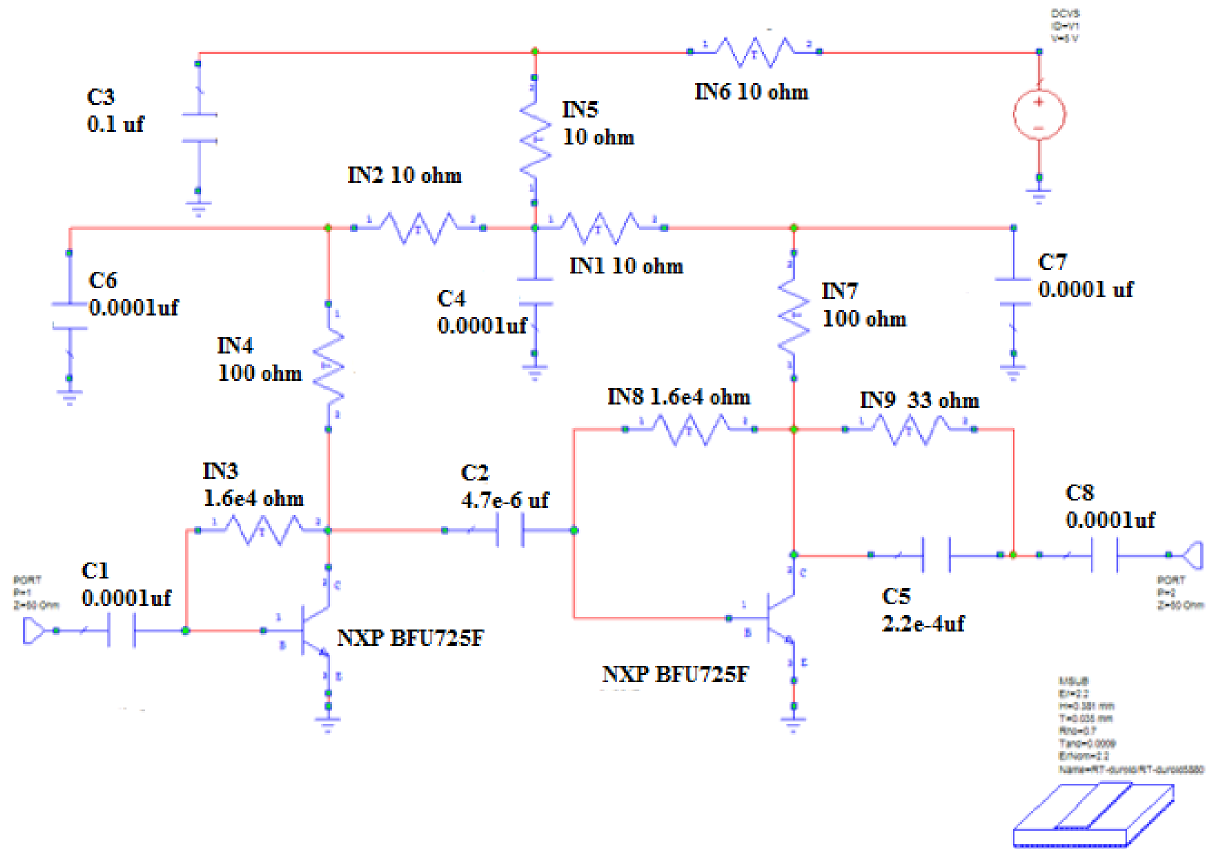


Fig. 4.1 schematic of the circuit

Noise Figure analysis and S-Parameters obtained during simulation of the schematic are displayed below in figure 4.2 and 4.3 respectively.

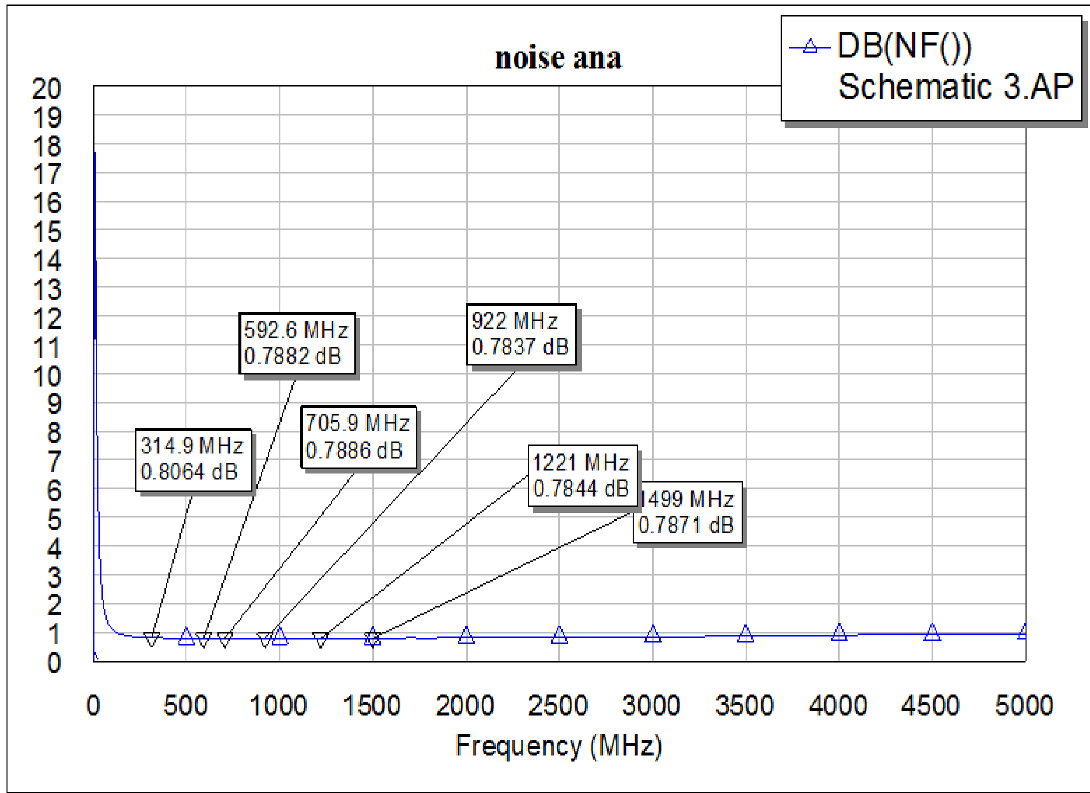


Fig. 4.2 noise figure performance of the LNA schematic

Note: The high noise figure in the start of the curve is due to the extrapolation of S-parameter values from 0-40 MHz values.

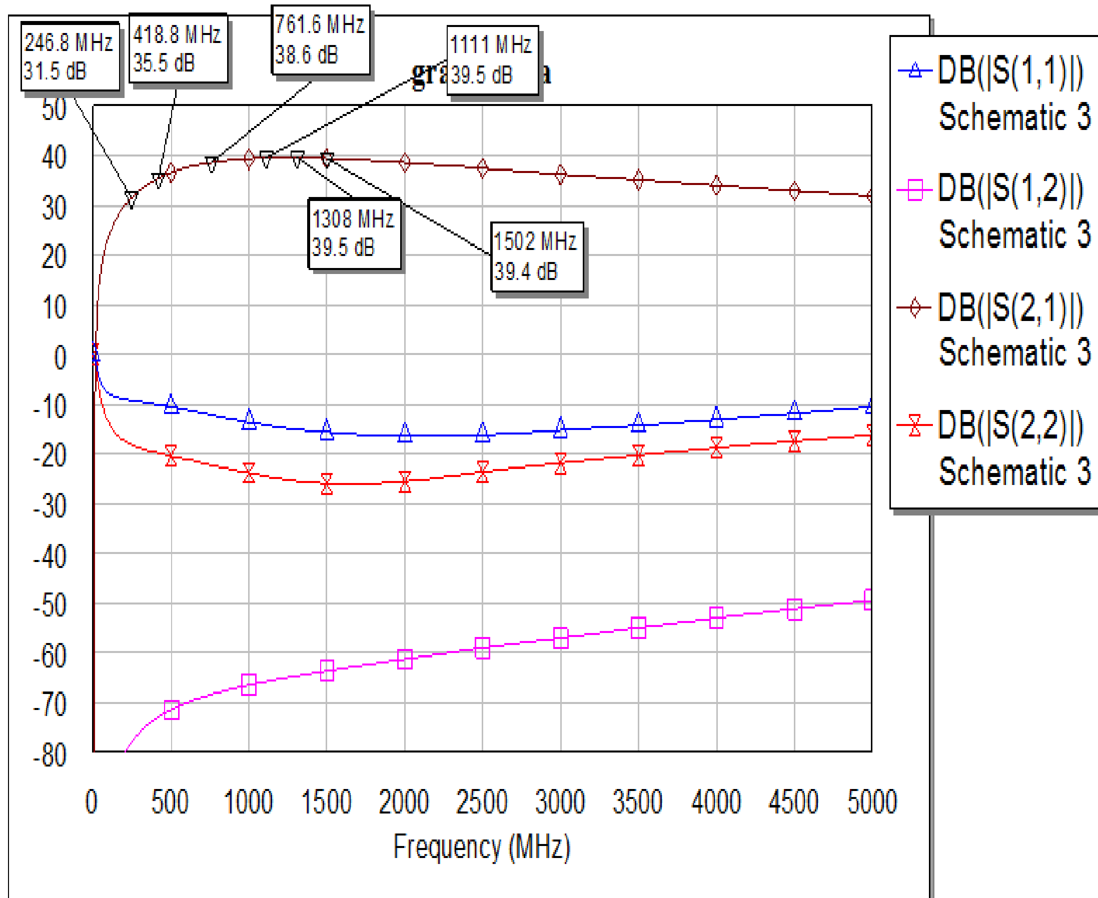


Fig. 4.3 S- Parameters of the LNA schematic.

After verifying that the schematic works normally and gives satisfying results that meets the desired criterion, next step is to make the design realizable. This is done by introducing microstrip lines between the components. In real circuits these microstrip lines will serve as the connecting link between the devices. Microstrip lines have impedance, capacitance and inductance of their own. This affects the working of the circuit and the element values that we have chosen before the schematic as explained in the theory section.

Therefore these values needed to be readjusted using the optimizing and tuning tools provided by the AWR design environment. Optimizer is an excellent tool to design a circuit when we have few goals to achieve. During optimization process we allow AWR to change the values of certain variables as capacitors, width and length of microsrip etc. to achieve a certain goal as a particular gain, reflection coefficients and noise figure etc. Optimizer changes the values of these parameters and evaluates the result till the cost of change no longer improves the result or the specified maximum number of iterations is over. Tuner on the other hand lets you change the value of the parameters by manually tuning them and viewing its effect on the performance curve such as noise figure and S- parameters curve.

But optimizing the circuit is not just one click job. Optimizer changes the values (length and width) of the microstrip without considering the realizability of circuit using these values. Therefore its upto manual insight to use these tools to get an approximation of preferred values and then make necessary compromises between the ideal performance and the realizable values

The modified circuit with optimized and tuned values of the circuit elements and microstrip lines is shown in figure 4.4. This is followed by figure 4.5 and 4.6 which shows the S-Parameter and Noise performance of the final simulated circuit respectively.

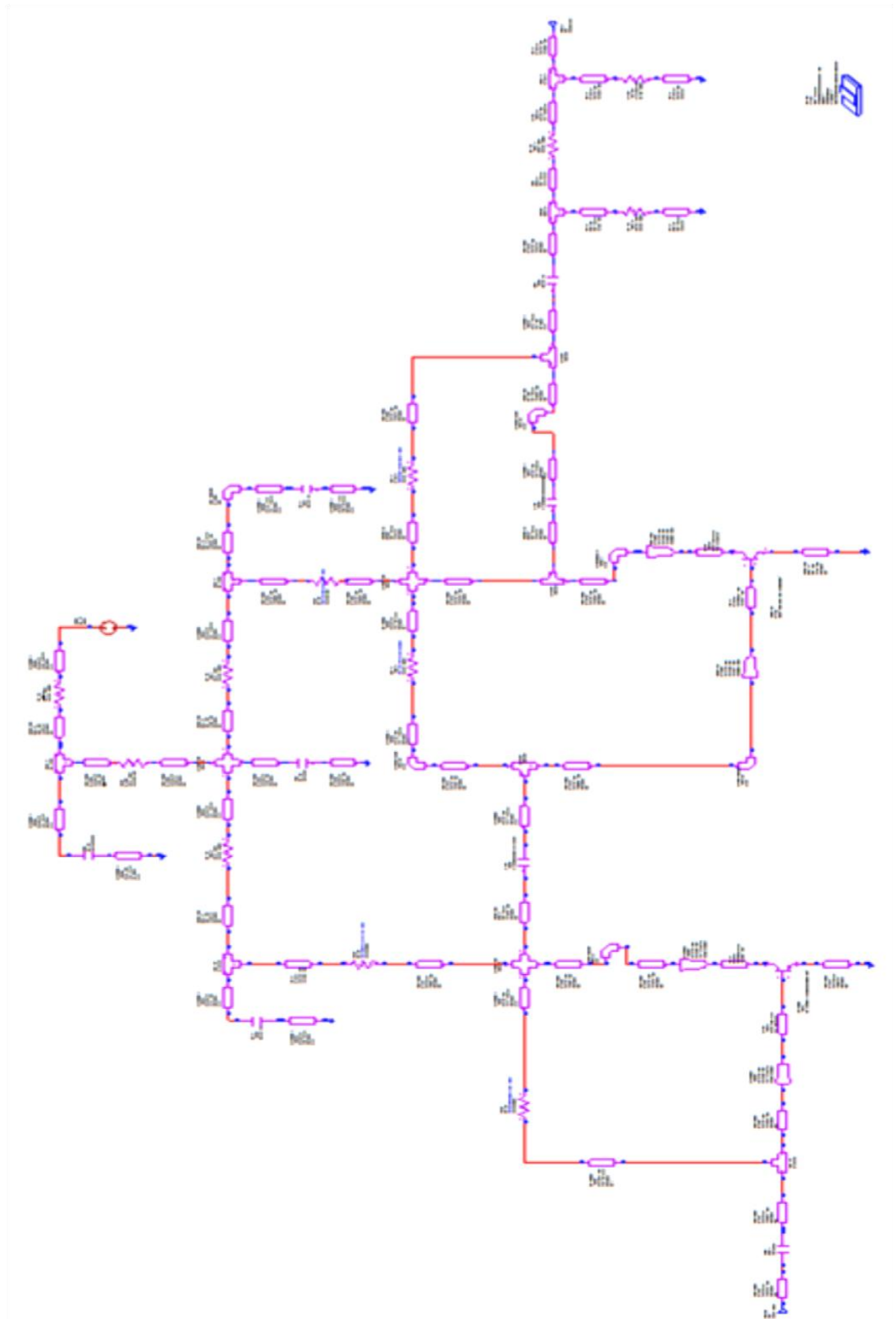


Fig. 4.4 Circuit with tuned values and microstrip line.

The final circuit has all the basic components of the schematic with the addition of microstrip introduced between every two components. The different shapes of microstrip are due to the TEE joints, L joints and tapers introduced to make the layout of the above circuit feasible and presentable. In addition to microstrips we have introduced a Pi attenuator in the circuit, although it was not present in the original schematic. Pi attenuator is the combination of three resistors that appear in a Pi shaped pattern. By adjusting their values we can introduce the desired attenuation in the circuit. Attenuator reduces the output reflection coefficient, but at the cost of the forward gain. We have used a 6 dB attenuator, which means our S_{21} and S_{22}, both are reduced by 6 dB .Various other values of Pi attenuator combination are given here as an example.

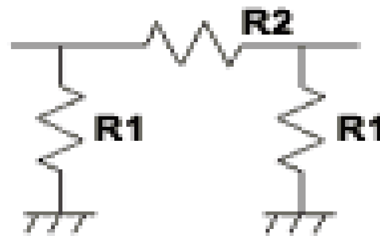
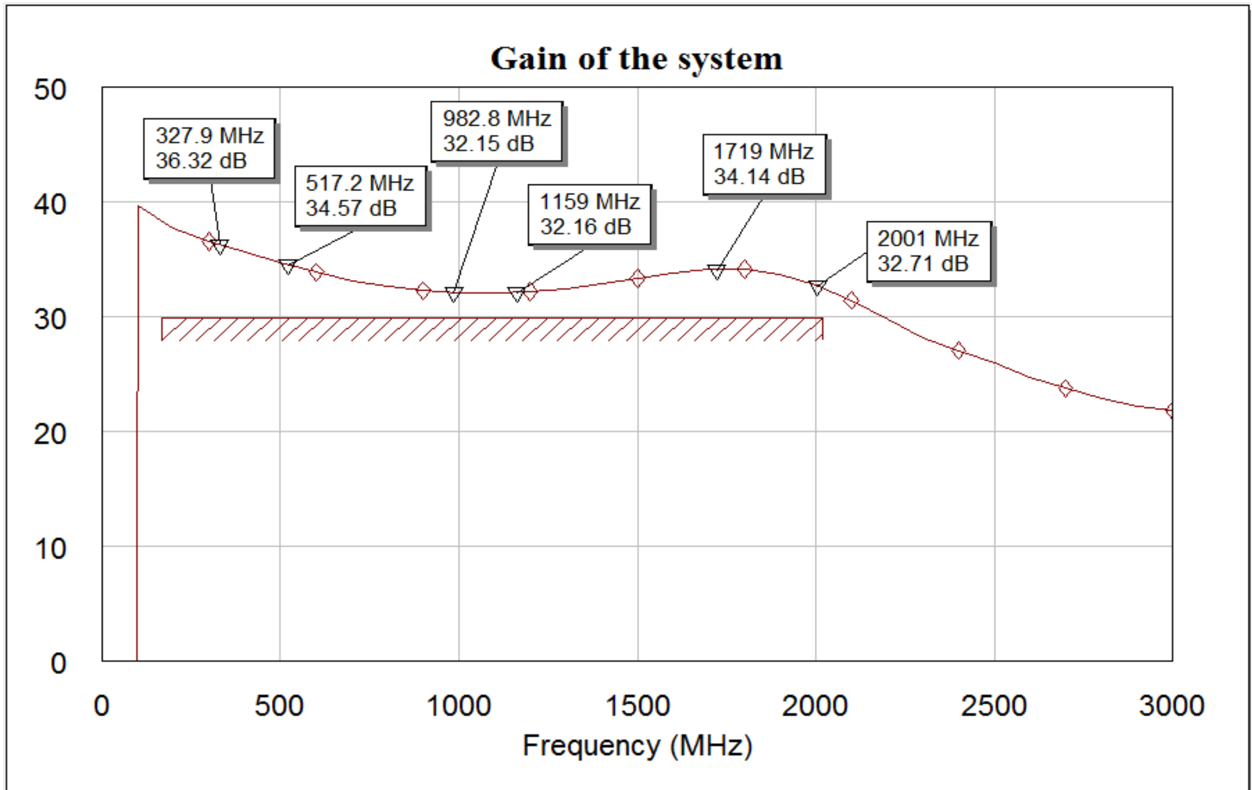


Fig. 4.5 A Pi type attenuator

Here first column gives the required attenuation in dB. R1 gives the value of the two shunt resistances while R2 gives the series resistance to be used

dB	R1	R2
1	870	5.8
2	436	11.6
3	292	17.6
4	221	23.9
5	178	30.4
6	150	37.4
7	131	44.8
8	116	53
9	105	62
10	96	71
12	84	93
14	75	120
16	69	154

Table 1 value of resistance for various attenuations



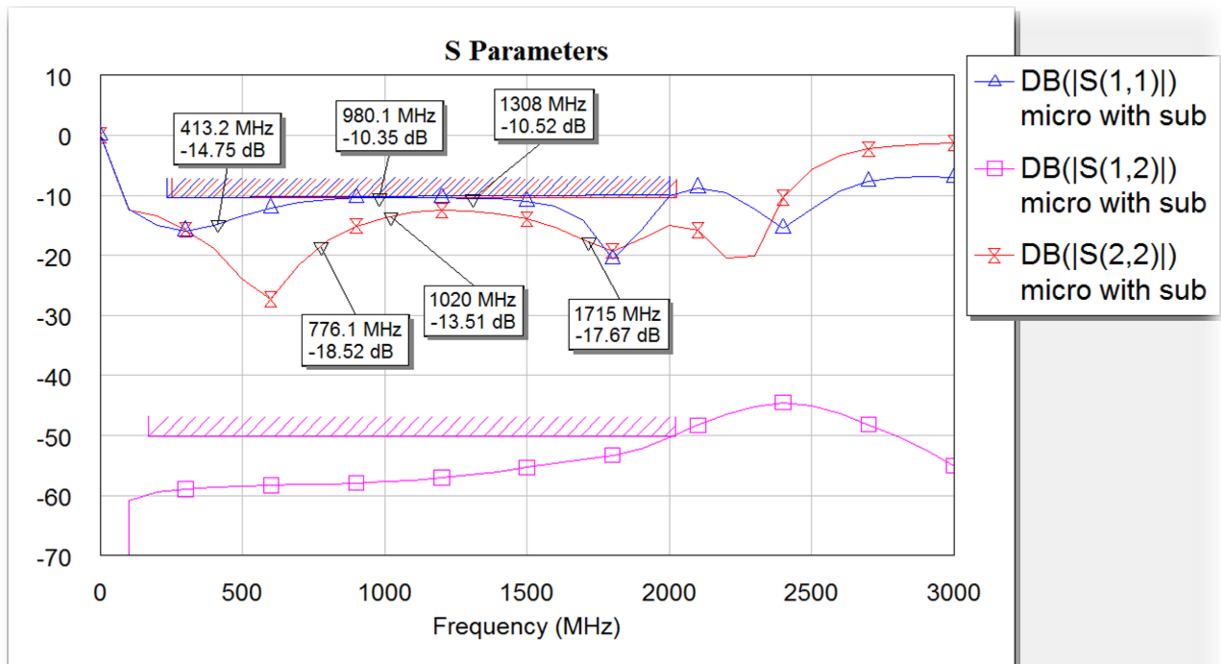


Fig. 4.6 Gain and S-Parameters of the final circuit

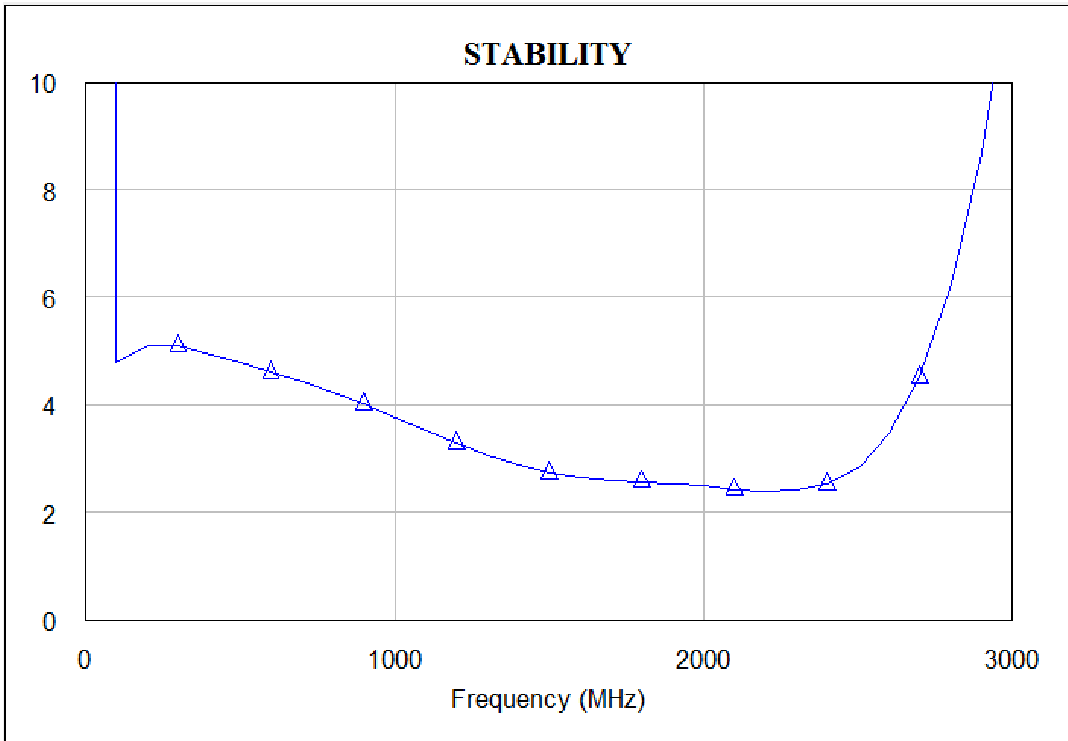


Fig. 4.7 stability factor (K) Vs Freq.

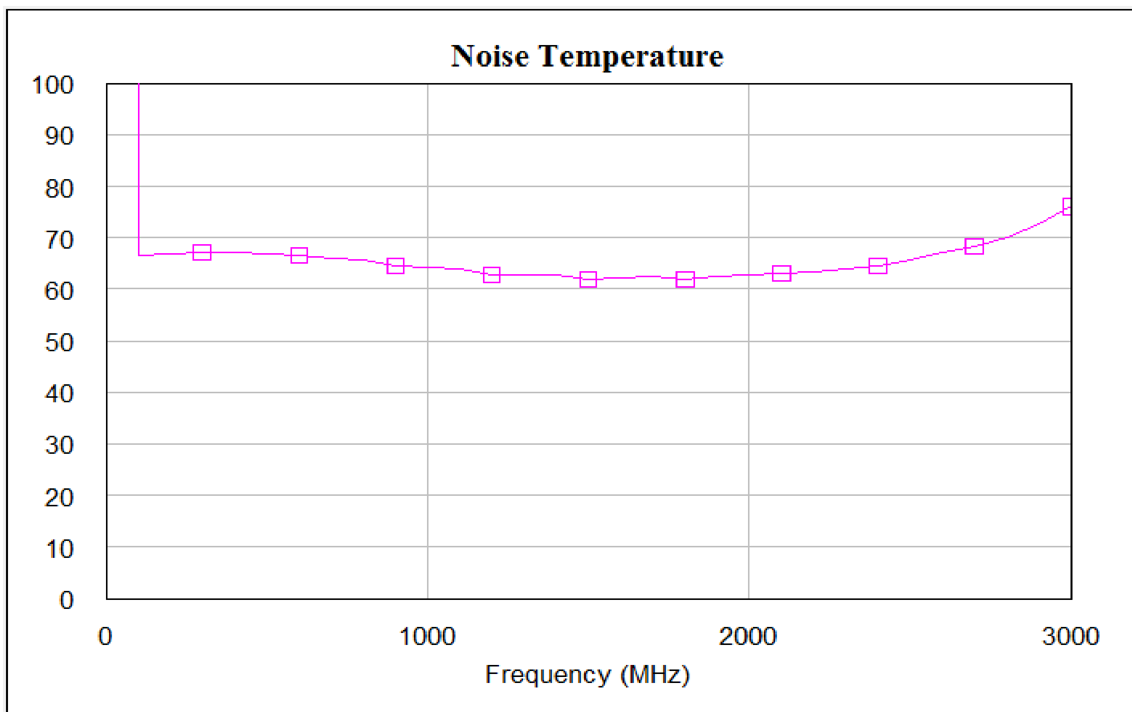


Fig. 4.8 Noise Temperature vs Frequency plot of the final circuit

4.2 DESIGN LAYOUT

In AWR layouts have to be prepared manually. Layout of standard chip components like 0805 and 1206 chip components are available. For any new component the layout have to be prepared. Figure 4.9 shows the layout of the NXPBFU725F transistor. Final layout prepared in AWR is shown in figure 4.10. Using GENESYS tool, Layout editing can be made easy. Therefore GENESYS was used to give a final touch to the layout and also drilling holes etc figure 4.11 shows the Top and Bottom layers of the layout as was provided to the fabricator.

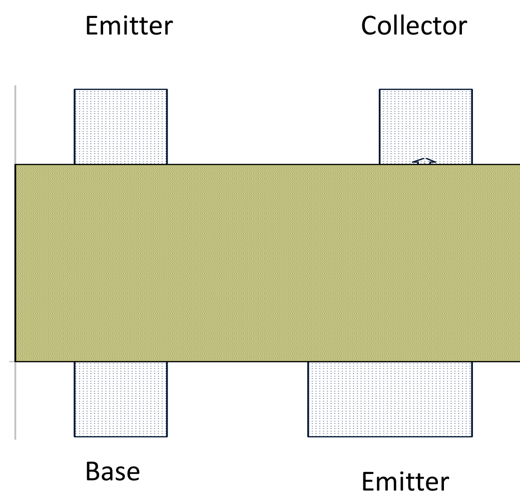


Fig. 4.9 Layout of the transistor NXP BFU725F

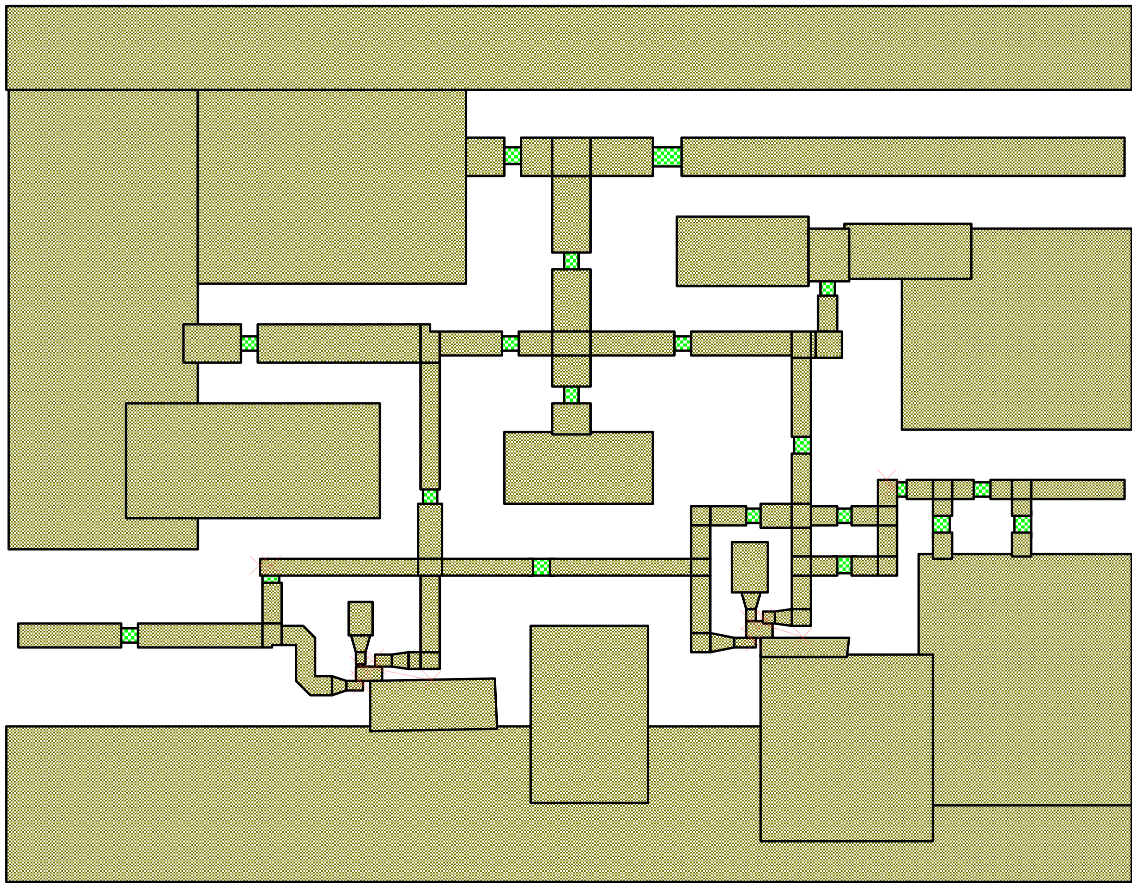


Fig. 4.10 final layout with ground planes as prepared in AWR.

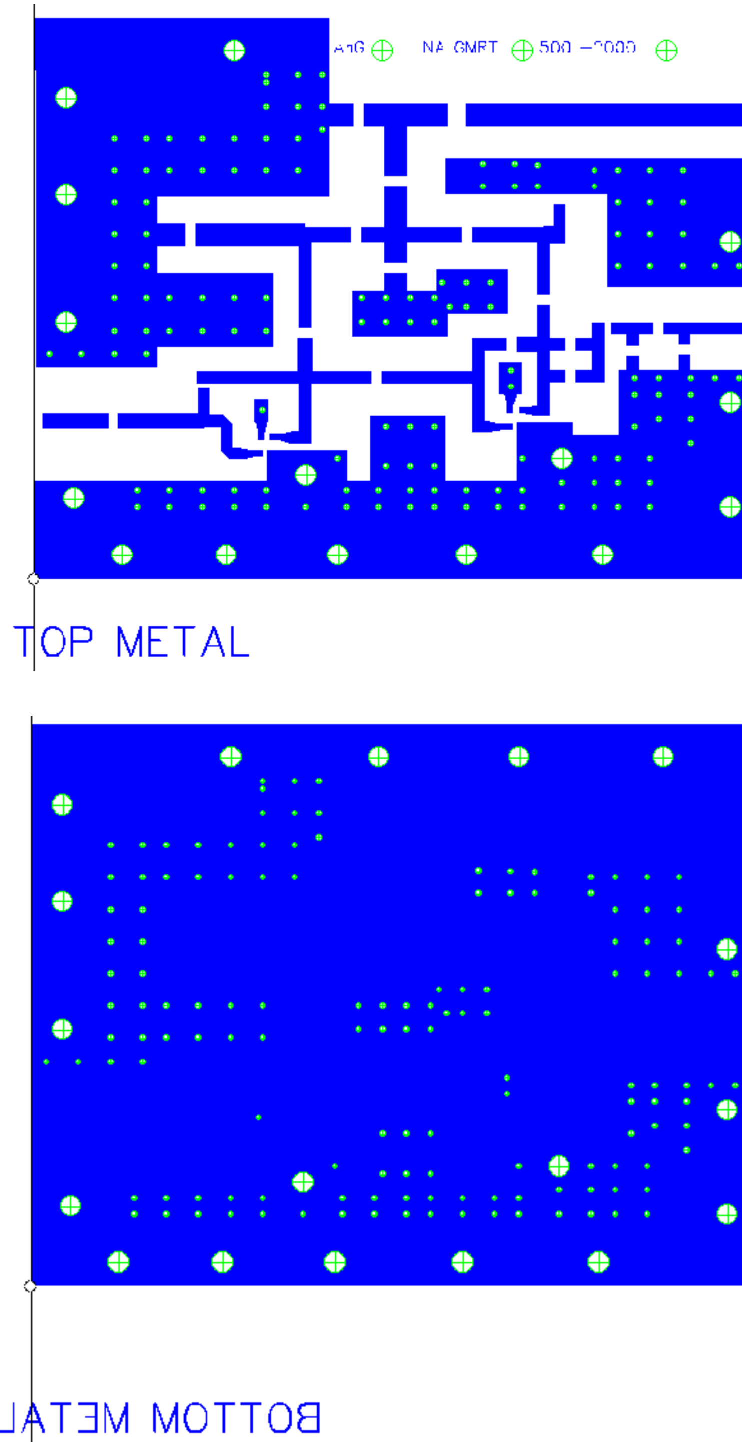


Fig. 4.11 Top and bottom metal layer of the circuit.

4.3 FABRICATION STEPS

The Printed Circuit Board Manufacturing Process:

Process starts when we send the layout files (4 in number) to the fabricator. This includes top metal and bottom metal gereber file, the drill file and ASCII drill list

Patterning | Etching

The majority of printed circuit boards are manufactured by applying a layer of copper over the entire surface of the circuit board substrate either on one side or both sides. This creates what is referred to as a blank printed circuit board, meaning the copper is everywhere on the surface. From here the unwanted areas are removed, this is called a subtractive method, the most common subtractive method is known as photoengraving.

Photoengraving

The photoengraving process uses a mask or photomask combined with chemical etching to subtract the copper areas from the circuit board substrate. The photomask is created with a photoplotter which takes the design from a CAD PCB software program.

Drilling

Each layer of the printed circuit board requires the ability of one layer to connect to another, this is achieved through drilling small holes called "VIAS". These drilled holes require precision placement and are most commonly done with the use of an automated drilling machine. These machines are driven by computer programs and files called numerically controlled drill or (NCD) files also referred to as excellon files. These files determine the position and size of each file in the design.

Solder Plating | Solder Resist

Pads and lands which will require components to be mounted on are plated to allow solderability of the components. Bare copper is not readily solderable and requires the surface to be plated with a material that facilitates soldering. In the past a lead based tin was used to plate the surfaces, but with RoHS compliance enacted newer materials are being used such as nickel and gold to both offer solderability and comply with RoHS standards.

Areas that should not be solderable are covered with a material to resist soldering. Solder resist refers the a polymer coating that acts as a mask and prevents solder from bridging traces and possibly creating short circuits to nearby component leads.

Silk Screen

When visible information needs to be applied to the board such as company logos, part numbers or instructions, silk screening is used to apply the text to the outer surface of the circuit board. Where spacing allows, screened text can indicate component designators, switch setting requirements and additional features to assist in the assembly process.

4.4 CHASSIS DRAWING

A chassis in an electronic device consists of the metal frame on which the circuit boards and other electronics are mounted. Circuit designer have to give the specifications of the PCB for construction of chassis. These specifications include the number and type of connectors, their location, size of the PCB and the screw holes required for mounting the PCB. Figure 4.12 gives the 3D CAD view of the Chassis we used for the project.

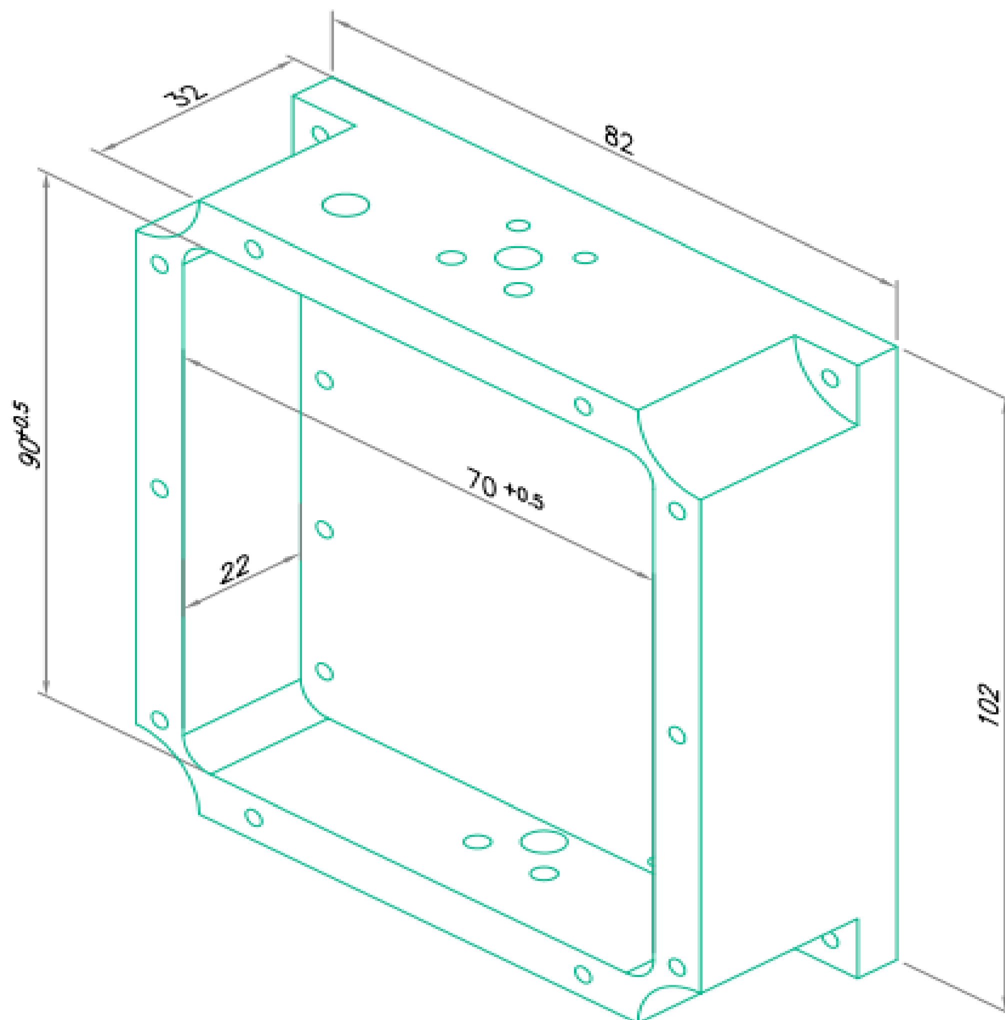


Fig. 4.12 chassis drawing

4.5 CAVITY RESONANCE

The device is prepared after soldering the component on the PCB and then mounting it on the chassis. But after closing the lid of the device an unexpected bump in gain curve was obtained, which was not present without the lid. The reason of this behavior is cavity resonance.

Solutions to the field equations inside an enclosed space reveal that standing wave modes may exist inside a cavity. These modes can exist in an empty rectangular cavity if the largest cavity dimension is greater than or equal to one-half a free-space wavelength. For a rectangular cavity, with dimensions a, b, c and a<b<c, and which is completely filled with a homogeneous material, the equation for the resonant frequency is.

$$(f)_{mnp} = \frac{1}{2\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2 + \left(\frac{p}{c}\right)^2}$$

Where ε is the material permittivity and μ is the material permeability.

How to fix the problem

Cavity resonance becomes an issue when a circuit, which is designed and built and works well, must be protected and/or shielded with a circuit board cover. For shielding purposes, the covers are made of or lined with metal. This creates a cavity above the circuit board where resonances can exist.

Relocating a particular circuit element to a different position in the cavity can often fix the problem. Intelligent positioning of posts or other objects to disrupt the standing wave can also be helpful, but both these methods can involve an investment in engineering design time and possible manufacturing delays.

Using microwave absorbent material in the cavity has proven to be effective at damping the resonance.

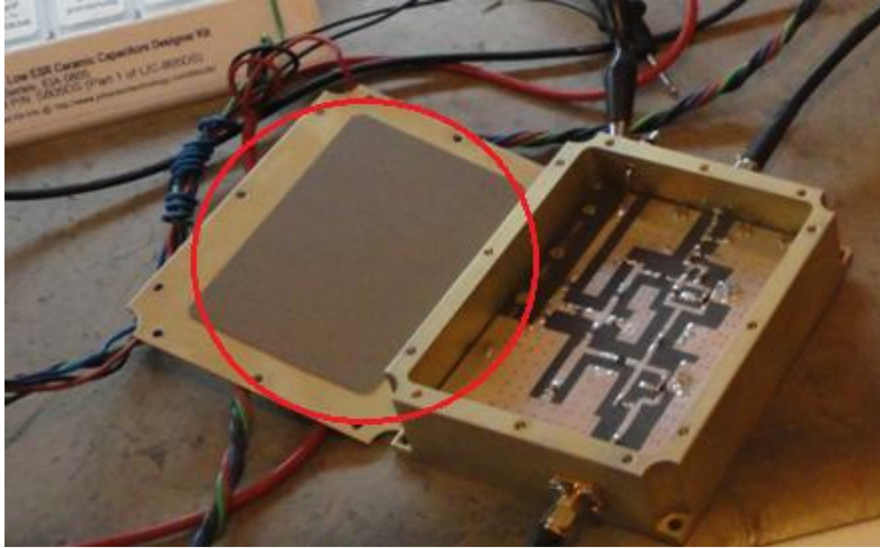


Fig. 4.13 Absorber material at the lid of LNA

We have used ET 400 RF absorber from Leader Tech to eliminate cavity resonance problem. Details about the material can be found in Appendix 2

CHAPTER FIVE

CRYOGENIC COOLING TEST AND OBSERVATION

5.1 CRYOGENIC COOLING TEST

After verifying the normal operation of the device in enclosed condition, the device is prepared for the cryogenic cooling test. This is done by sealing the device with the help of aluminum tape as shown in the figure 5.1 shown below.

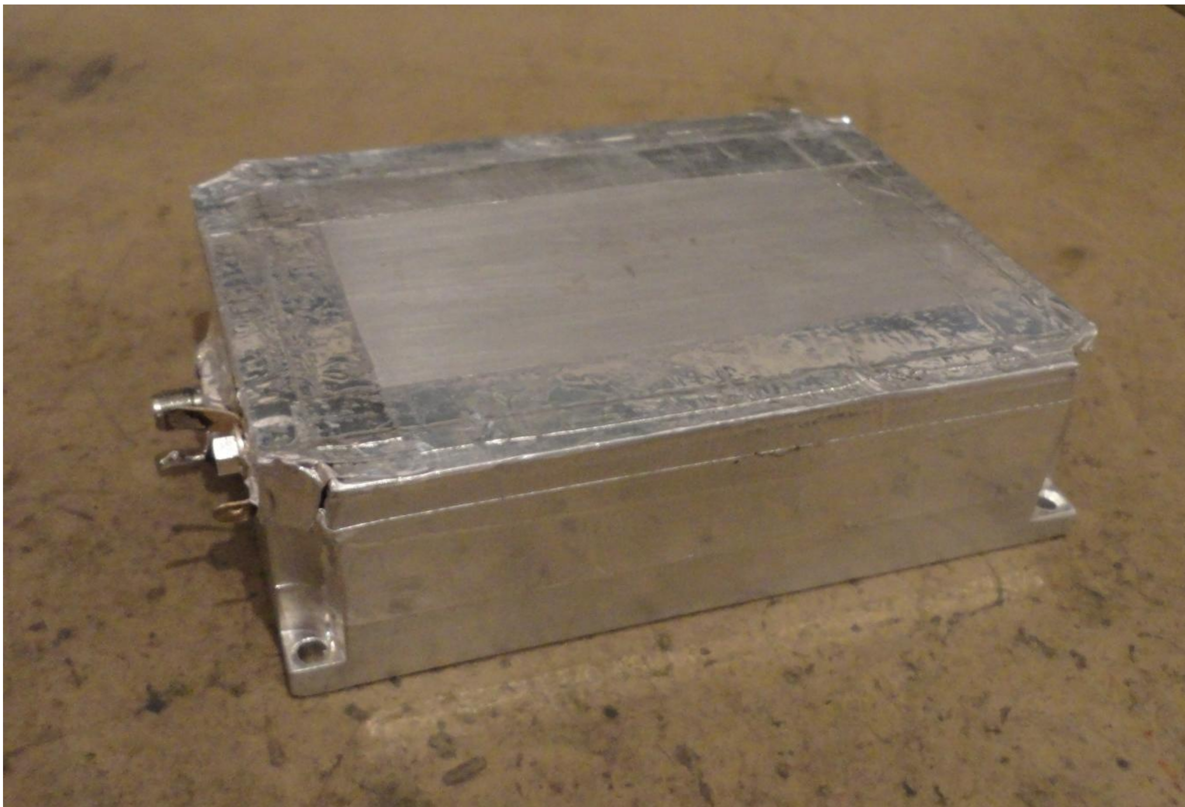


Fig. 5.1 LNA sealed using aluminium tape

The device is cooled using liquid nitrogen, which can cool the device up to its boiling point, which is 77 K. Device is immersed in a Dewar flask and the liquid nitrogen is poured into it.

The test setup can be easily understood by figure 5.2 which represent the block diagram of the test setup.

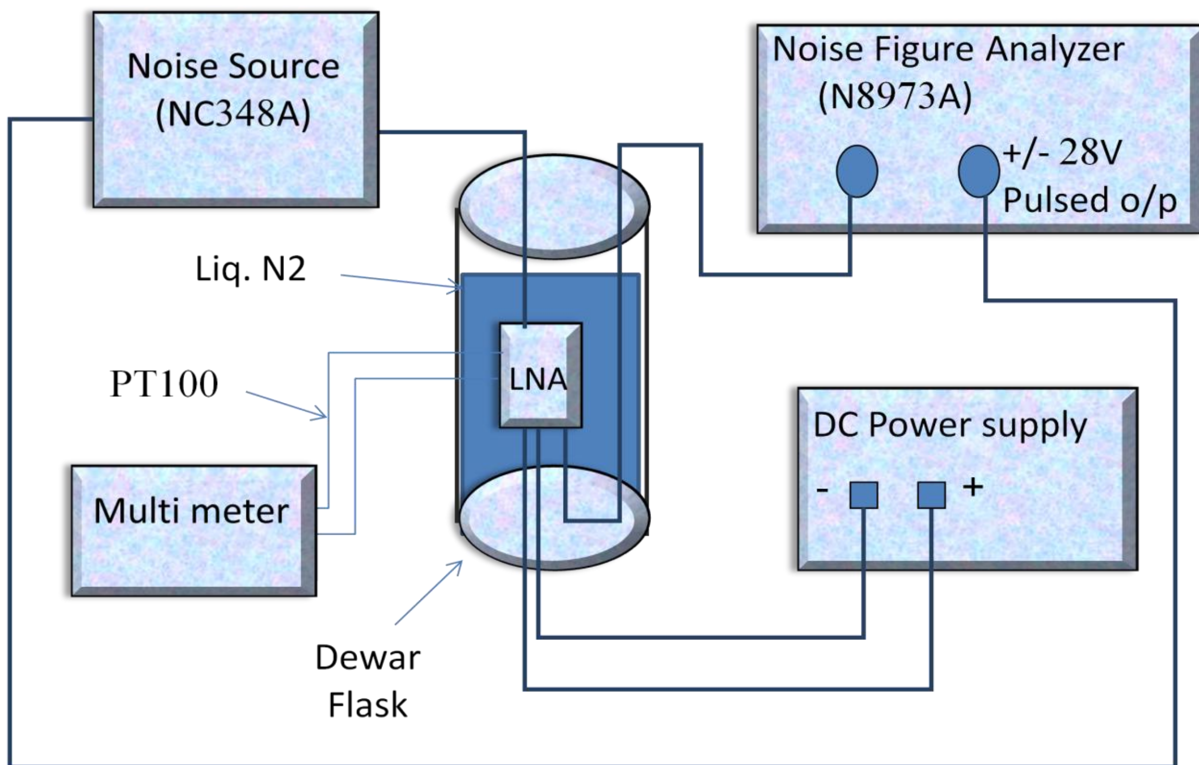


Fig. 5.2 Block diagram of the Test setup.

As clearly seen in figure 5.2, the device is connected to the Agilent noise figure analyzer via a calibrated noise source. The LNA is put into Dewar flask and is connected to the analyzer using semi-Rigid cables. Using a network analyzer the insertion loss of these cables can be calculated and can be fed into the noise figure analyzer for compensation. The flask is left open and liquid nitrogen is poured into the container. To note the temperature of the LNA, PT100 thermocouple is attached to it using an electric tape. Resistance of the thermocouple is recorded by a multimeter. After the flask is filled and LNA is completely submersed inside the liquid nitrogen, temperature is allowed to stabilize. The Dewar flask is left open so that nitrogen starts boiling off slowly after a few minutes. When the temperature starts to increase different sets of readings can be obtained by saving the readings in the noise figure analyzer.

In figure 5.3, one can see the test setup and its various components clearly, while figure 5.4 shows the empty dewar flask.

Fig. 5.3 Test setup

Fig. 5.4 Empty Dewar flask

Agilent noise figure generates bitmap file of the screen. Figure 5.5 shows the noise Temperature performance and Gain of the LNA at 77K, while figure 5.6 shows the same at room temperature.

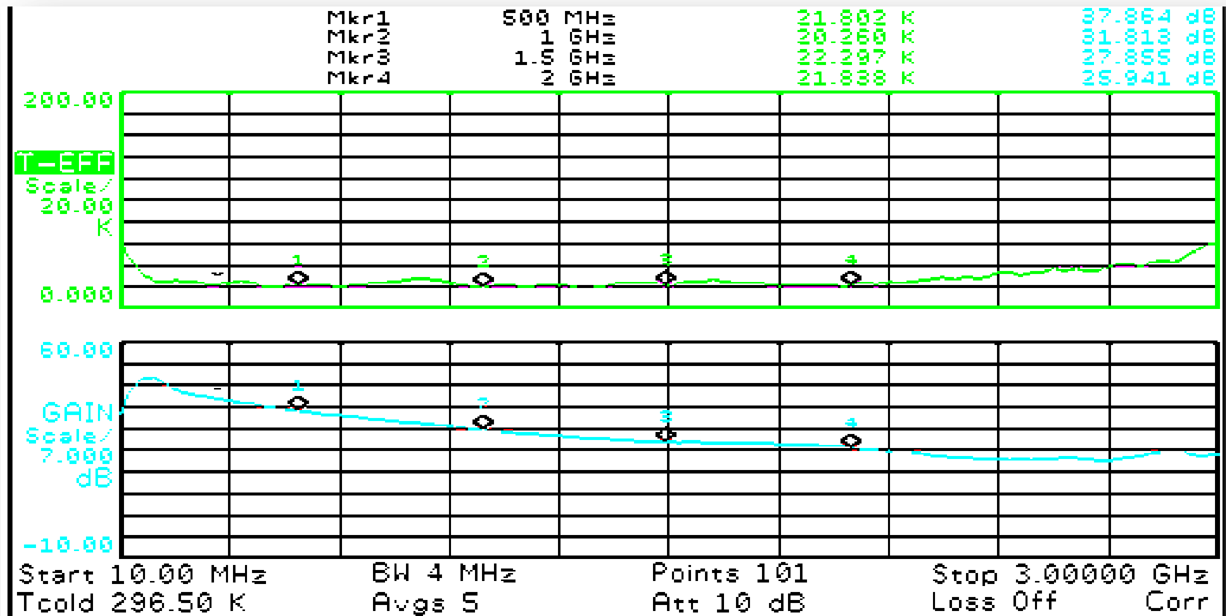


Fig. 5.5 Noise Temperature and Gain curves for the frequency range of operation at 77 K.

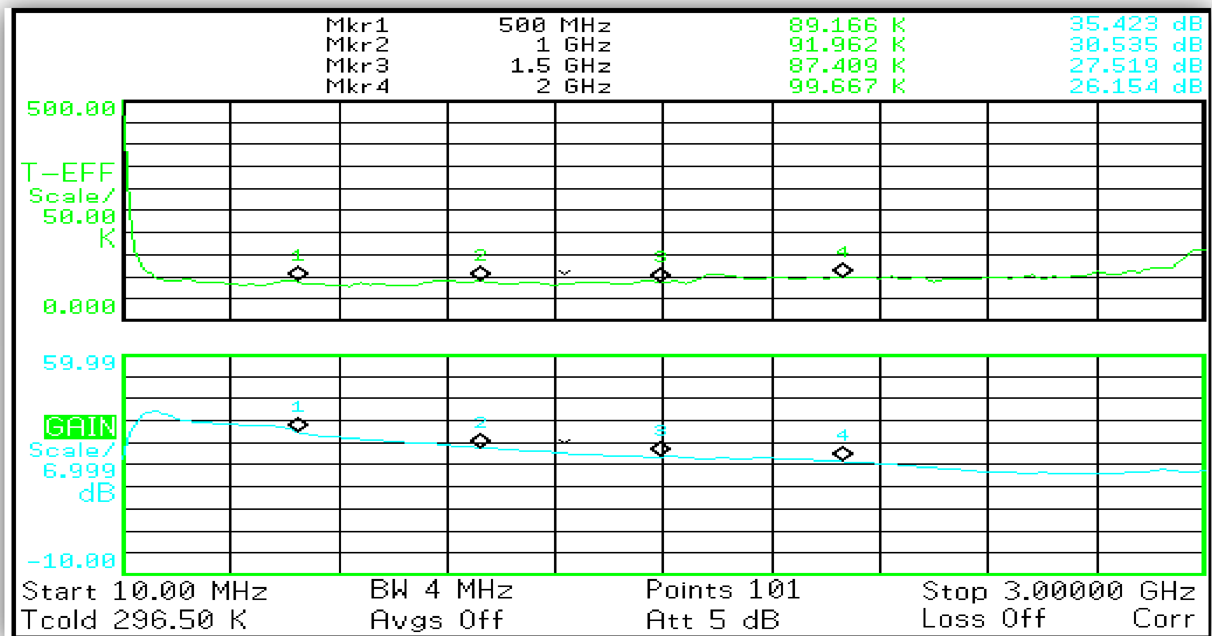


Fig. 5.6 Noise Temperature and Gain curves for the frequency range of operation at room temperature

S- Parameters of the device were analyzed using Agilent E5070B network analyzer. Figure 5.7 is the snapshot of the S-parameter values of the device at room temperature.

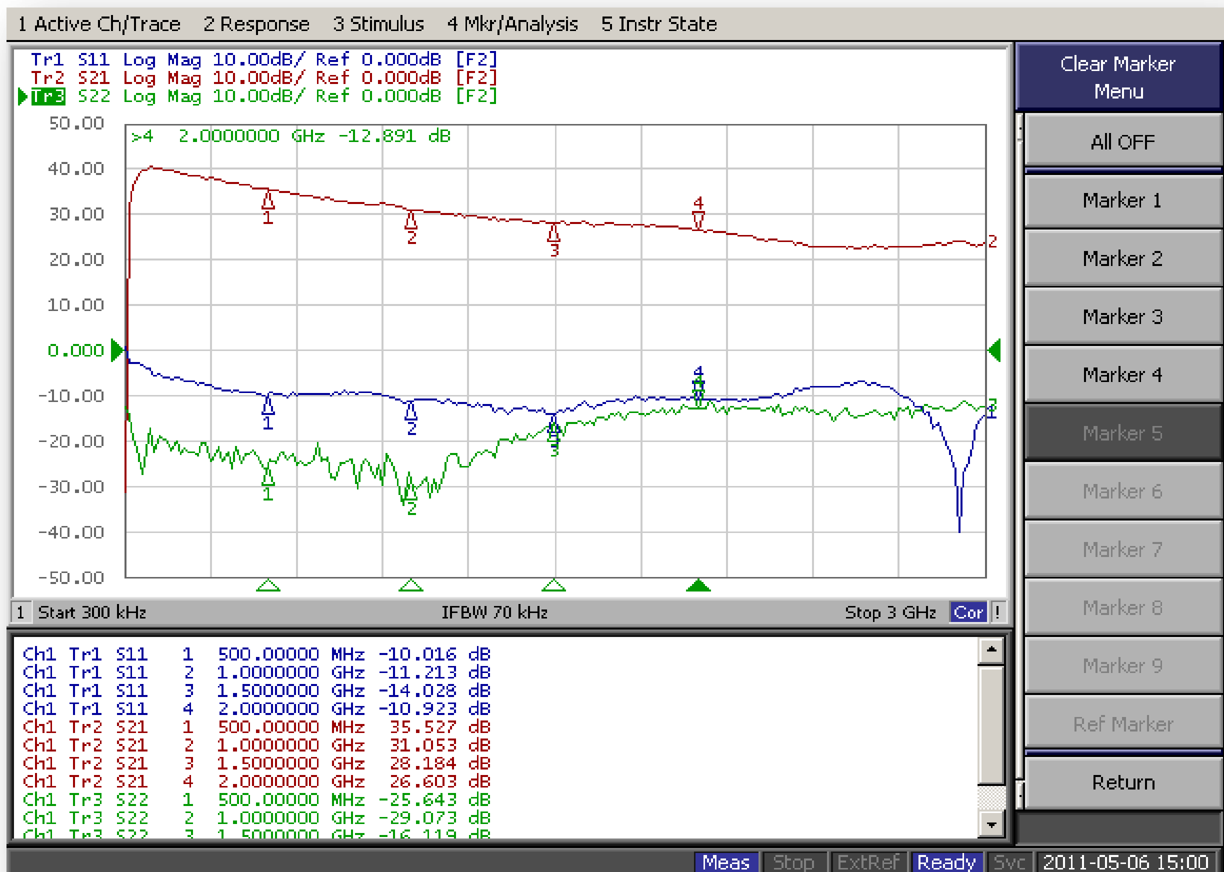


Fig. 5.7 S- Parameters of the device. Red (the topmost) is the gain (S21), Blue (middle curve) represents the input reflection coefficient (S11) and Green (lowermost) represents the output reflection coefficient (S22).

5.2 RESULTS ANALYSIS

From the noise temperature and gain data collected over the temperature range, different curves can be obtained to show the trends. Also few readings at same temperature but different supply voltages were taken. Figures 5.8 to 5.18 are the various graphs that were obtained by processing the data using MATLAB tool. Description of each figure is given below it.

5.2.1 NOISE TEMPERATURE CURVES

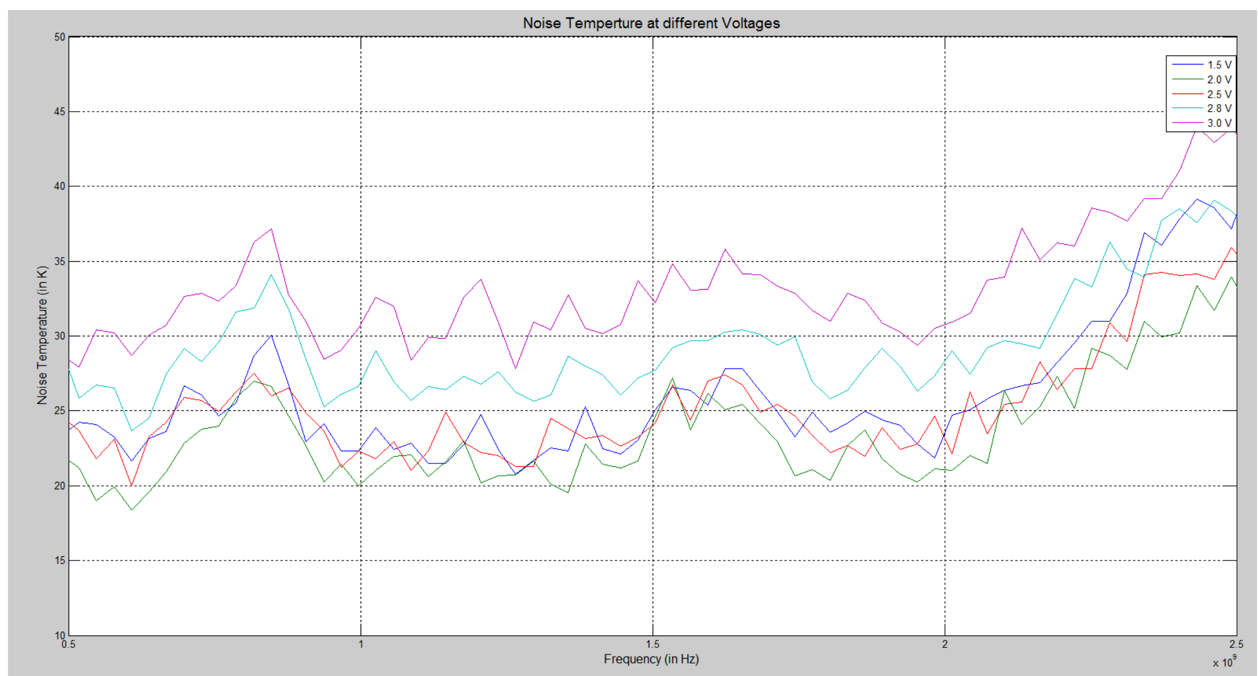


Fig. 5.8 Change of Noise Temperature with Supply Voltage at 77 K temperature.

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Figure 5.8 consists of different curves of Noise Temperature Vs frequency for various values of supply voltages. It is evident from this curves that overall noise performance of the LNA decreases with the decrease in supply voltage. But when we decrease the supply voltage below 2.0 V the noise figure is increased. This situation can be attributed to the change in bias of the Si-Ge HBT . Noise figure decreases initially due to reduction in current, but as the voltage is dropped further, the device could not work properly resulting into increment in noise Temperature.

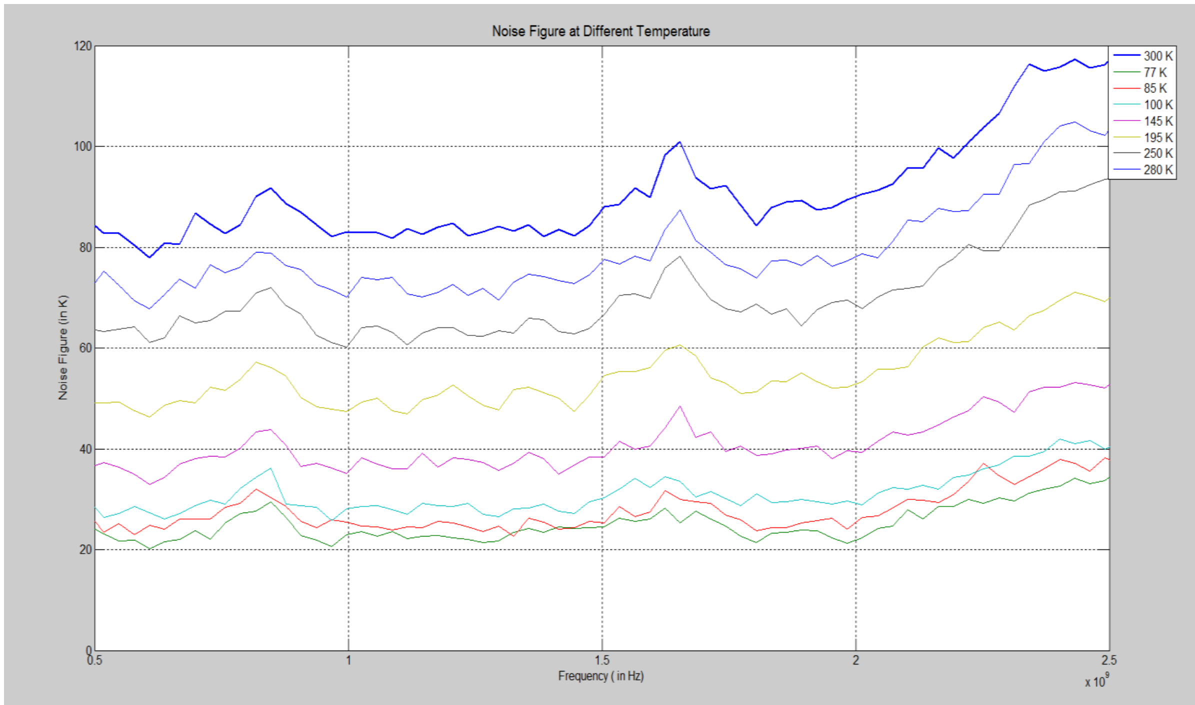


Fig. 5.9 Change of Noise Temperature with temperature

Figure 5.9 shows various Noise Temperature Vs frequency plots at various values of ambient temperature. As expected noise Temperature decreases with the decrease in temperature. The reason behind this is explained in the theory section. Noise figure is both directly proportional to temperature and also decrease with increase in DC gain of the transistor device. DC gain increases with decrease in temperature, further lowering the noise temperature.

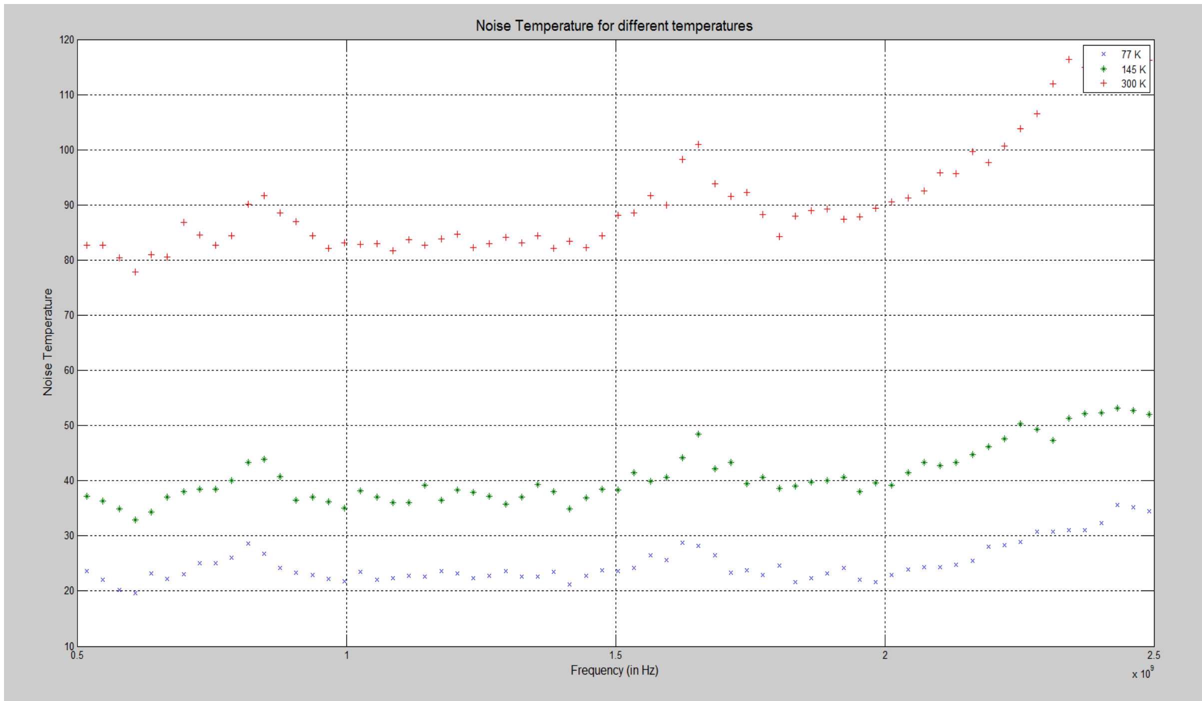


Fig. 5.10 Noise temperature Vs Frequency curves at different temperature showing the data point density

Figure 5.10 represents the same relation as Figure 5.9, but in Figure 5.10 the points are shown using symbols and not joined by a smooth cure as was the case in figure 5.9. This shows the data set density of our figures. There are 101 points between 0 Hz to 3GHz frequency range. 70 points are visible in the above figure where the x axis is limited to 0.5 GHz to 2.5 GHz.

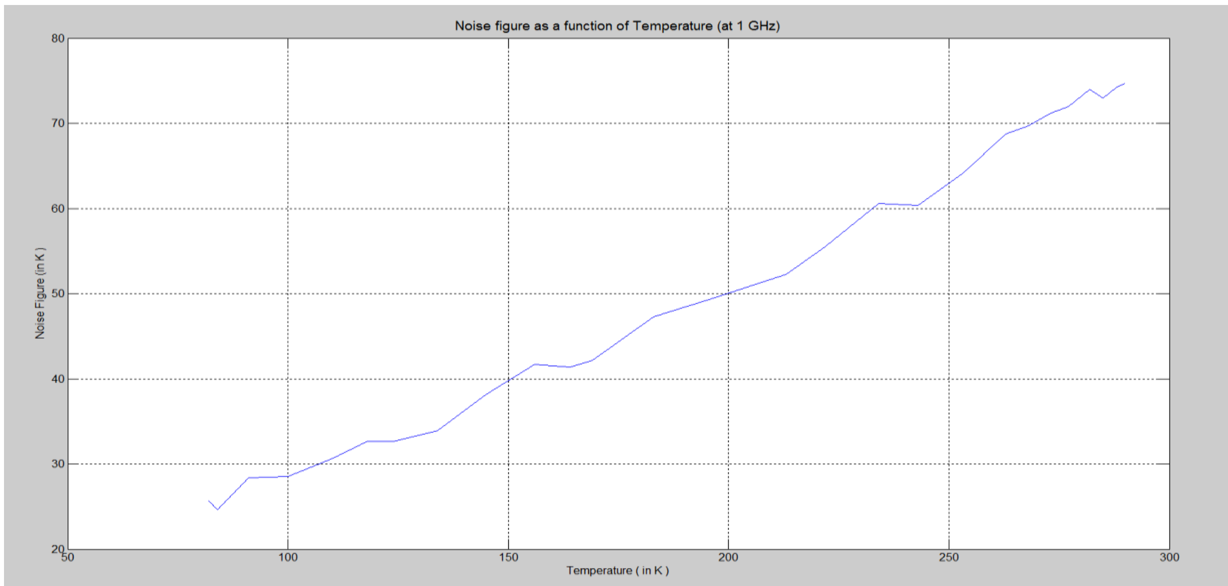


Fig. 5.11 Plot of Noise Temperature with change in temperature at 1 GHz

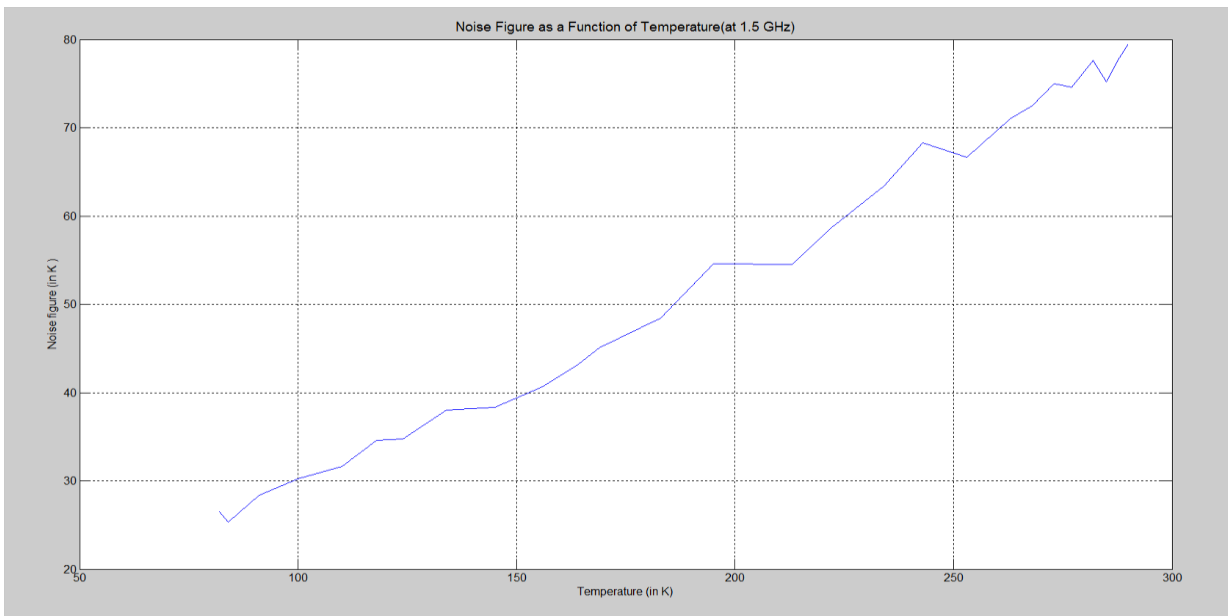


Fig. 5.12 Plot of Noise Temperature with change in temperature at 1.5 GHz

Figure 5.11 is the plot of Noise Temperature Vs Ambient Temperature at a single frequency point of 1 GHz, while Figure 5.12 is the same plot at 1.5GHz. The information conveyed by these two curves is same as Figure 5.9 but way of representation is different.

5.2.2 GAIN CURVES

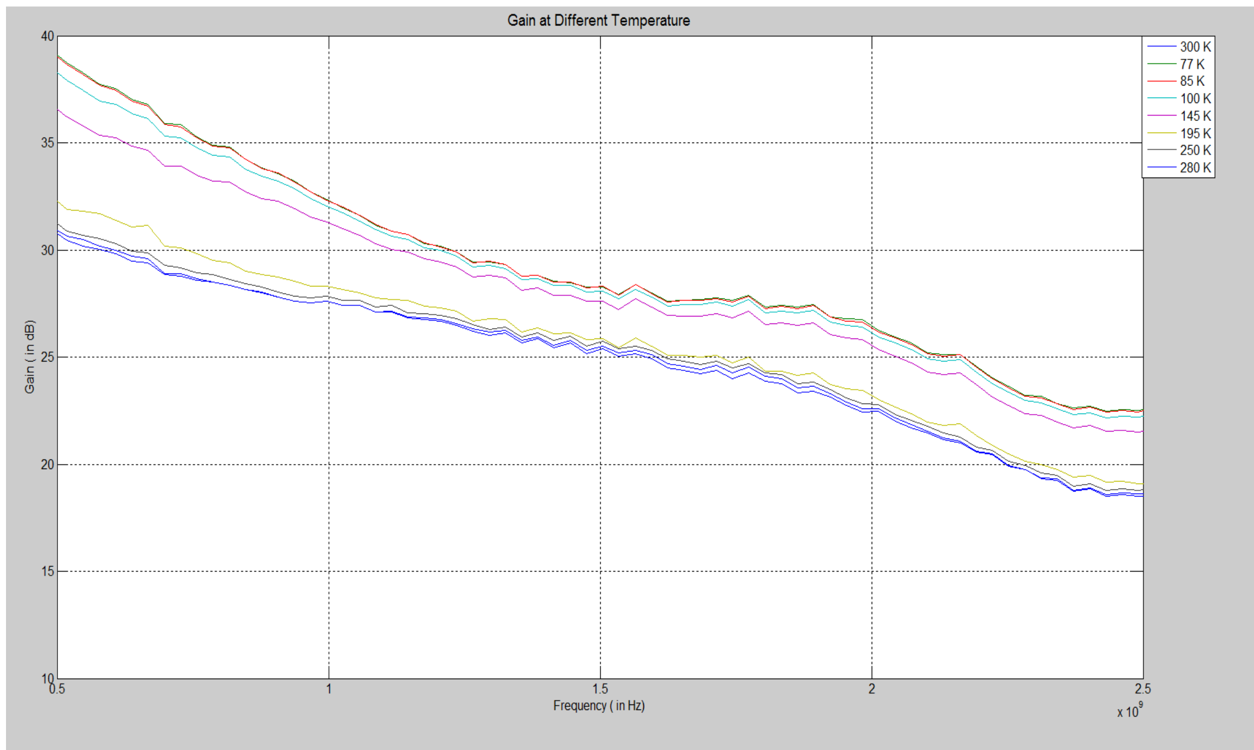


Fig. 5.13. Change of Gain with temperature

Figure 5.13 shows various Gain Vs frequency plots at various values of ambient temperature. There is a steady increase in value of overall gain with decrease in temperature. This characteristic can be attributed to increase of DC gain with decrease in temperature. This effect is explained in the theory section 3.4.2.

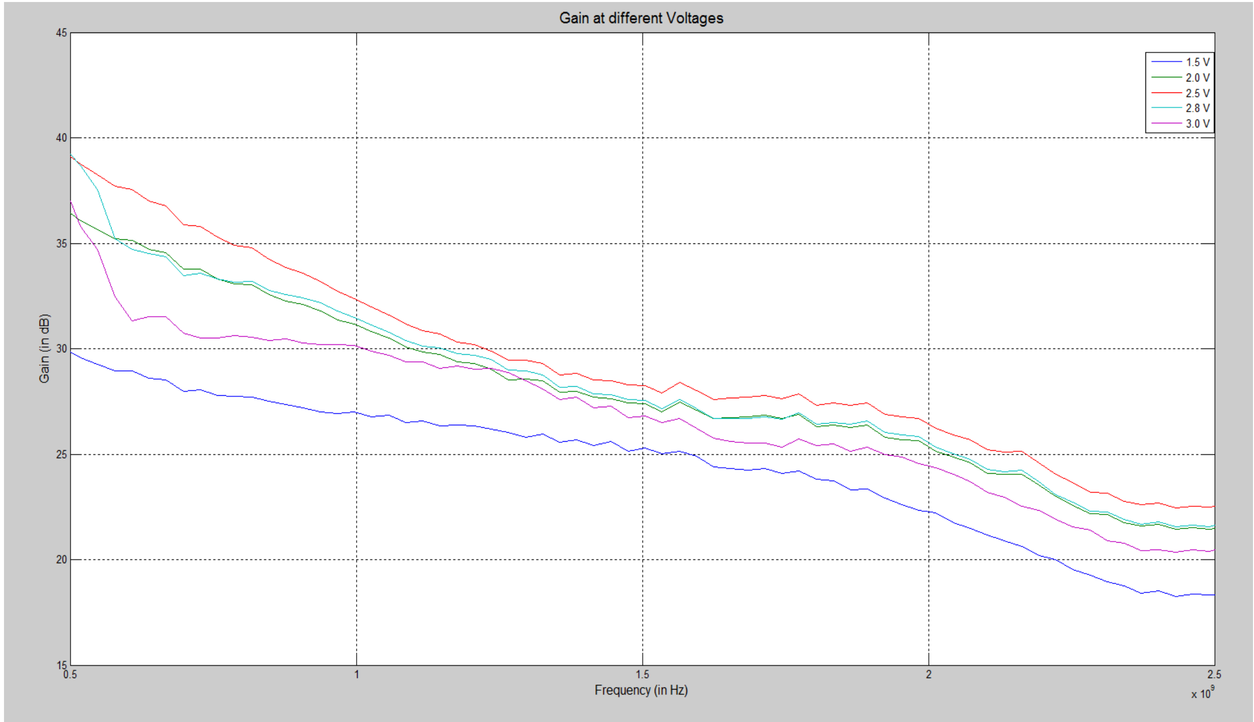


Fig. 5.14 Change of Gain with Supply Voltage at 77K.

Figure 5.14 consists of different curves of Gain Vs frequency for various values of supply voltages. Gain of the LNA increases and also becomes stable as we decrease the supply voltage from 3.0 V to 2.5V, but decreases again with further decrease in voltage from 2.5 V to 1.5 V. this increase of gain with decrease of supply voltage was not observed at room temperature. But at 77 K, the current gain of the device was elevated and hence the proper biasing voltage gave the maximum gain and any deviation from it resulted in decrease in gain.

5.2.3 NOISE FIGURE EXTRAPOLATION

Using the noise figure data available, we calculated the quadratic least square approximation for the data. Using that equation, noise figure values at 17K and 4K were predicted. Figure 5.14 contains the curves representing the approximated values of noise temperature at 17 and 4 K. these curves are valid only if noise temperature varies with the ambient temperature in the same way throughout the temperature range. Here we will explain the steps to extract the extrapolated values using simple figures. All steps are performed in MATLAB.

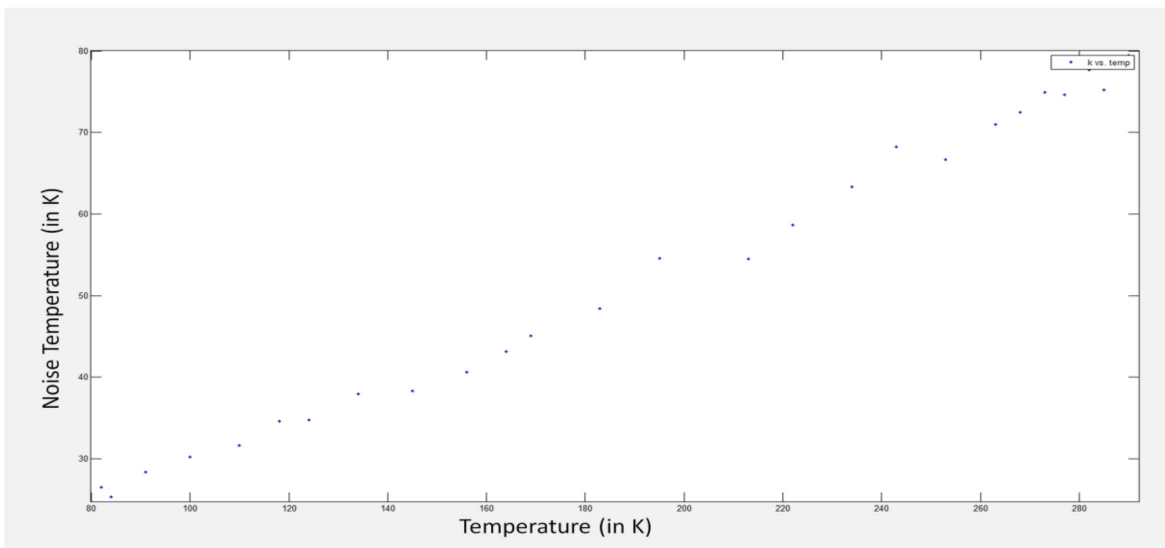


Fig. 5.15 Data points

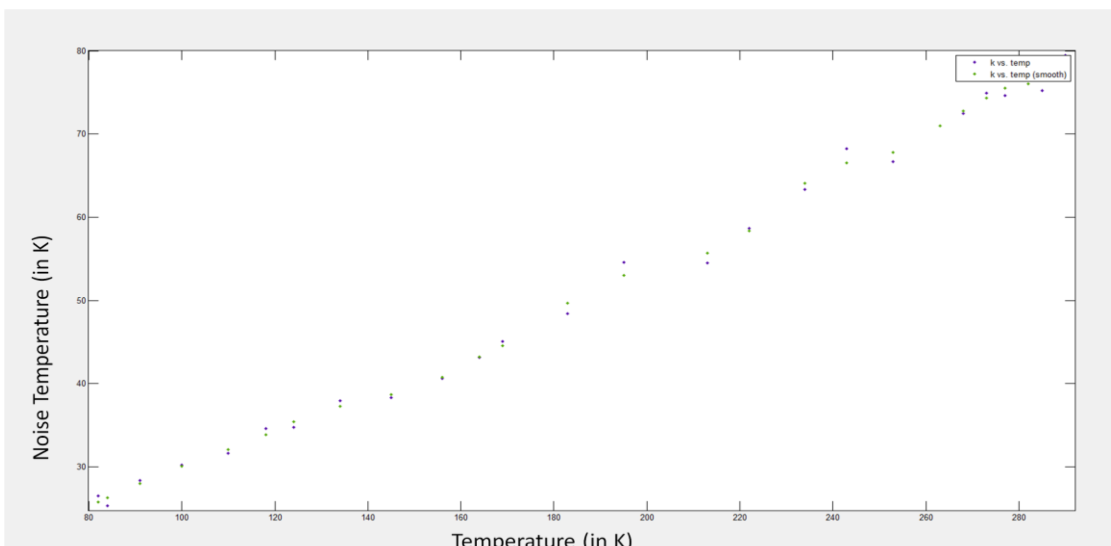
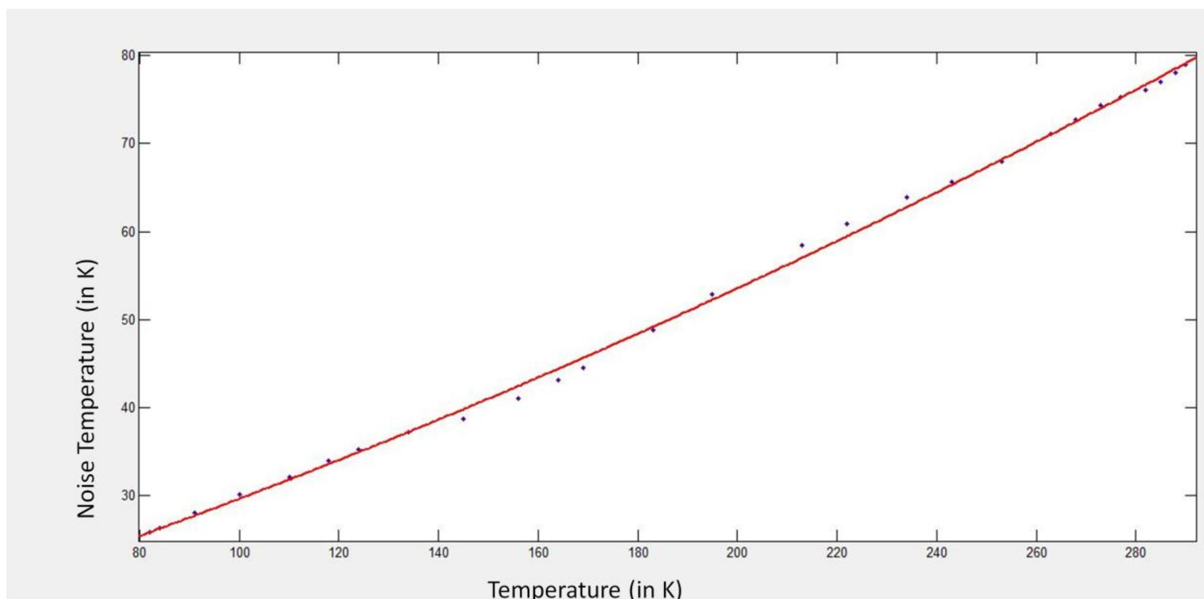


Fig. 5.16 Smoothed Data points

First step is to obtain Noise Temperature at different temperatures but same frequency. Here we have obtained the points at 1.5GHz. Using 'cftool' command curve fitting tool can be opened and data points can be entered by clicking on the Data command box. Our data set is displayed in figure 5.15. Next step is to smooth the given data. We have used quadratic fit smoothening to smooth the data. Figure 5.16 shows the raw and smooth data set. Now by clicking on 'fitting' command button we can open fit window. We have used quadratic polynomial fit to extract the equation for our data set. The fit is displayed in figure 5.17. After obtaining the equation for the curve we can obtain the value of noise temperature at any temperature. We have calculated noise temperature at 4 and 17 K. After repeating the previous steps at different frequencies, we can plot Noise Temperature Vs Frequency plot at 4 and 17 K. which is shown in figure 5.18.



Equation of the curve : $f(x) = 0.0002367*x^2 + 0.1684*x + 10.4$

Fig. 5.17 Curve Fit through smoothed data set

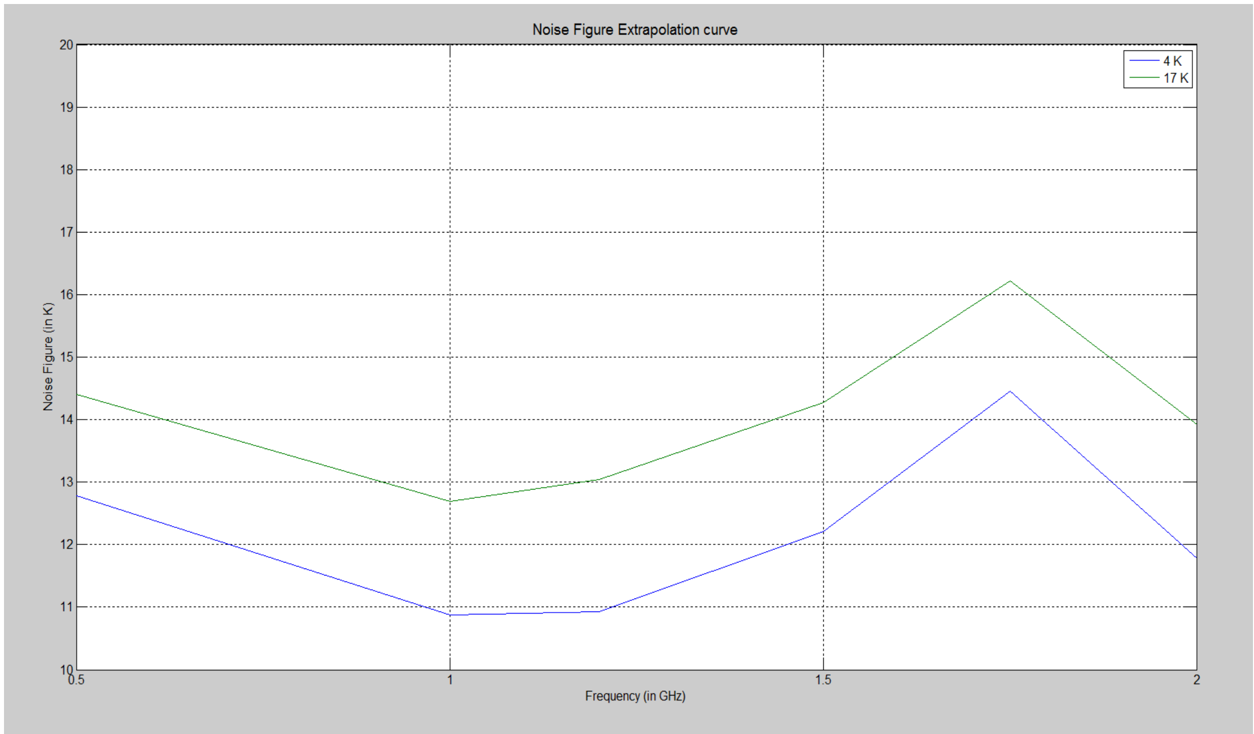


Fig. 5.18 Noise Temperature Extrapolation curve

CHAPTER SIX

CONCLUSION

Based upon the observation and analysis of the data we can conclude that device performance is within the specified limits. The S- Parameter requirements are sufficiently met at both simulation and real test phase. The device is not feasible to be used at room temperature because of the poor noise performance at room temperature. The existing HEMT LNAs at GMRT have lower Noise figure than our SiGe based LNA. But when cooled to a cryogenic temperature, SiGe LNA's performance increases drastically. The Noise figure Falls below the mark set by the HEMT LNAs and gain of the device is also improved. Although the test could only be performed till 77K, using our calculation we can estimate that LNA will give excellent performance once cooled to 17K. Also, LNA performs better at certain supply voltages as inferred from the results in chapter 5. Few points which can make the LNA better are discussed in next few lines. Design can be improved with more optimized values of the components. Cryogenic effects can be studied under both cooling and warming up phase using closed circuit cooling chamber. The LNA can be designed for optimum supply voltage obtained from the report. Work can be done on realizing the design and to be interfaced with the other components of front end at GMRT. Field test can be performed to evaluate the effect of parameters that are negligible inside lab environment. Design can be optimized to eliminate cavity resonance without the use of RF absorber material. LNA can be made compact in size so that it is easier to install at feed of the antenna.

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APPENDIX 1

This appendix contains the datasheet of the transistor used in the design.

BFU725F/N1

NPN wideband silicon germanium RF transistor

Rev. 01 — 13 July 2009 Product data sheet

1. Product profile

1.1 General description

NPN silicon germanium microwave transistor for high speed, low noise applications in a plastic, 4-pin dual-emitter SOT343F package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

1.2 Features

- Low noise high gain microwave transistor
- Noise figure (NF) = 0.7 dB at 5.8 GHz
- High maximum stable gain 27 dB at 1.8 GHz
- 110 GHz f_T silicon germanium technology

1.3 Applications

- 2nd LNA stage and mixer stage in DBS LNB's
- Satellite radio
- Low noise amplifiers for microwave communications systems
- WLAN and CDMA applications
- Analog/digital cordless applications
- Ka band oscillators (DRO's)

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-	10	V
V_{CEO}	collector-emitter voltage	open base		-	-	2.8	V
V_{EBO}	emitter-base voltage	open collector		-	-	0.55	V
I_C	collector current			-	25	40	mA
P_{tot}	total power dissipation	$T_{sp} \leq 90$ °C	[1]	-	-	136	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 2 V; T_j = 25 °C		160	280	400	

Table 1. Quick reference data ...*continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{CBS}	collector-base capacitance	V_{CB} = 2 V; f = 1 MHz		-	70	-	fF
f_T	transition frequency	I_C = 25 mA; V_{CE} = 2 V; f = 2 GHz; T_{amb} = 25 °C		-	55	-	GHz
$G_{p(max)}$	maximum power gain	I_C = 25 mA; V_{CE} = 2 V; f = 5.8 GHz; T_{amb} = 25 °C	[2]	-	18	-	dB
NF	noise figure	I_C = 5 mA; V_{CE} = 2 V; f = 5.8 GHz; $\Gamma_S = \Gamma_{opt}$; T_{amb} = 25 °C		-	0.7	-	dB

[1] T_{sp} is the temperature at the solder point of the emitter lead.

[2] $G_{p(max)}$ is the maximum power gain, if K > 1. If K < 1 then $G_{p(max)}$ = Maximum Stable Gain (MSG).

2. Pinning information

Table 2. Discrete pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter		
2	base		
3	emitter		
4	collector		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BFU725F/N1	-	plastic surface-mounted flat pack package; reverse pinning; 4 leads	SOT343F

4. Marking

Table 4. Marking

Type number	Marking	Description
BFU725F/N1	B7*	* = p : made in Hong Kong
		* = t : made in Malaysia
		* = W : made in China

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5. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	10	V
V_{CEO}	collector-emitter voltage	open base		-	2.8	V
V_{EBO}	emitter-base voltage	open collector		-	0.55	V
I_C	collector current			-	40	mA
P_{tot}	total power dissipation	$T_{sp} \leq 90$ °C	[1]	-	136	mW
T_{stg}	storage temperature			−65	+150	°C
T_j	junction temperature			-	150	°C

[1] T_{sp} is the temperature at the solder point of the emitter lead.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		440	K/W

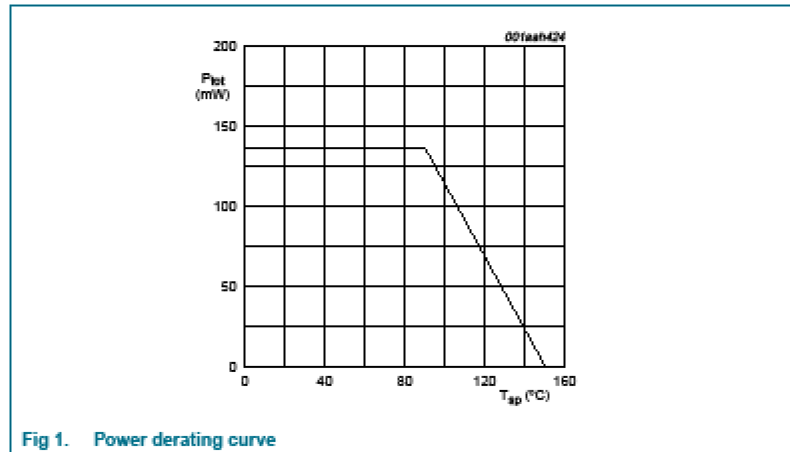

Fig 1. Power derating curve

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7. Characteristics

Table 7. Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 2.5 µA; I_E = 0 mA		10	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 1 mA; I_B = 0 mA		2.8	-	-	V
I_C	collector current			-	25	40	mA
I_{CBO}	collector-base cut-off current	I_E = 0 mA; V_{CB} = 4.5 V		-	-	100	nA
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 2 V		160	280	400	
C_{CES}	collector-emitter capacitance	V_{CB} = 2 V; f = 1 MHz		-	268	-	fF
C_{EBS}	emitter-base capacitance	V_{EB} = 0.5 V; f = 1 MHz		-	400	-	fF
C_{CBS}	collector-base capacitance	V_{CB} = 2 V; f = 1 MHz		-	70	-	fF
f_T	transition frequency	I_C = 25 mA; V_{CE} = 2 V; f = 2 GHz; T_{amb} = 25 °C		-	55	-	GHz
$G_{p(max)}$	maximum power gain	I_C = 25 mA; V_{CE} = 2 V; T_{amb} = 25 °C	[1]				
		f = 1.5 GHz		-	28	-	dB
		f = 1.8 GHz		-	27	-	dB
		f = 2.4 GHz		-	25.5	-	dB
		f = 5.8 GHz		-	18	-	dB
		f = 12 GHz		-	13	-	dB
$\lvert s_{21}\rvert^2$	insertion power gain	I_C = 25 mA; V_{CE} = 2 V; T_{amb} = 25 °C					
		f = 1.5 GHz		-	26.7	-	dB
		f = 1.8 GHz		-	25.4	-	dB
		f = 2.4 GHz		-	23	-	dB
		f = 5.8 GHz		-	16	-	dB
		f = 12 GHz		-	9.3	-	dB
NF	noise figure	I_C = 5 mA; V_{CE} = 2 V; $\Gamma_S = \Gamma_{opt}$; T_{amb} = 25 °C					
		f = 1.5 GHz		-	0.42	-	dB
		f = 1.8 GHz		-	0.43	-	dB
		f = 2.4 GHz		-	0.47	-	dB
		f = 5.8 GHz		-	0.7	-	dB
		f = 12 GHz		-	1.1	-	dB
G_{ass}	associated gain	I_C = 5 mA; V_{CE} = 2 V; $\Gamma_S = \Gamma_{opt}$; T_{amb} = 25 °C					
		f = 1.5 GHz		-	24	-	dB
		f = 1.8 GHz		-	22	-	dB
		f = 2.4 GHz		-	20	-	dB
		f = 5.8 GHz		-	13.5	-	dB
		f = 12 GHz		-	10	-	dB

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Table 7. Characteristics *...continued*

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	I_C = 25 mA; V_{CE} = 2 V; Z_S = Z_L = 50 Ω; T_{amb} = 25 °C				
		f = 1.5 GHz	-	8.5	-	dBm
		f = 1.8 GHz	-	9	-	dBm
		f = 2.4 GHz	-	8.5	-	dBm
		f = 5.8 GHz	-	8	-	dBm
IP3	third-order intercept point	I_C = 25 mA; V_{CE} = 2 V; Z_S = Z_L = 50 Ω; T_{amb} = 25 °C; $f_2 = f_1$ + 1 MHz				
		f_1 = 1.5 GHz	-	17	-	dBm
		f_1 = 1.8 GHz	-	17	-	dBm
		f_1 = 2.4 GHz	-	17	-	dBm
		f_1 = 5.8 GHz	-	19	-	dBm

[1] $G_{p(max)}$ is the maximum power gain, if K > 1. If K < 1 then $G_{p(max)}$ = MSG.

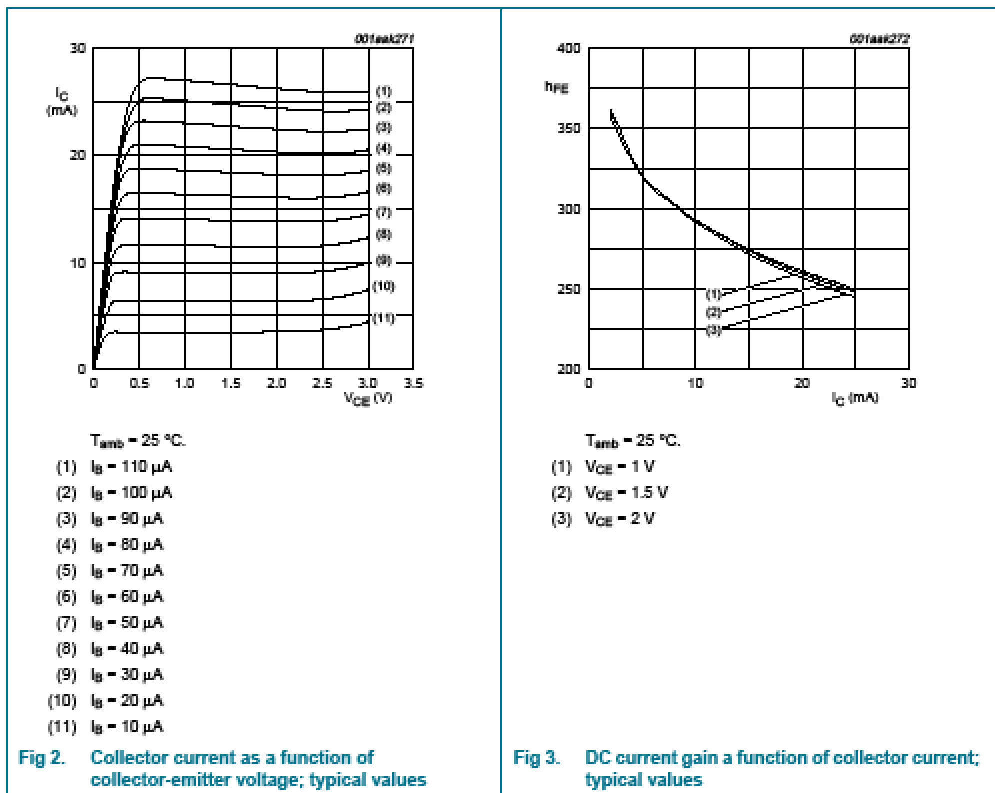

Fig 2. Collector current as a function of collector-emitter voltage; typical values

Fig 3. DC current gain a function of collector current; typical values

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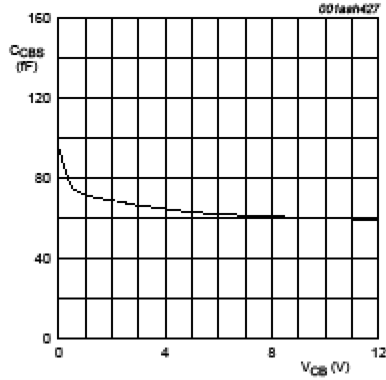
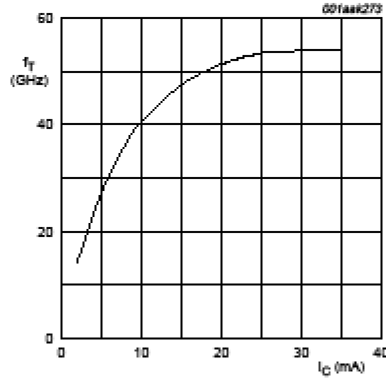


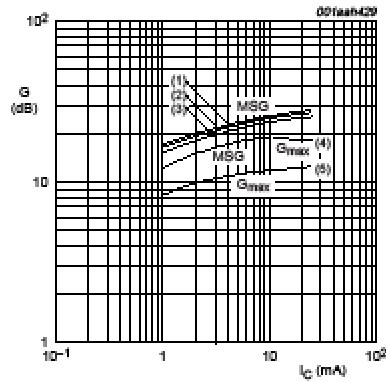
f = 1 MHz, T_{amb} = 25 °C.

Fig 4. Collector-base capacitance as a function of collector-base voltage; typical values



V_{CE} = 2 V; f = 2 GHz; T_{amb} = 25 °C.

Fig 5. Transition frequency as a function of collector current; typical values



V_{CE} = 2 V; T_{amb} = 25 °C.

(1) f = 1.5 GHz

(2) f = 1.8 GHz

(3) f = 2.4 GHz

(4) f = 5.8 GHz

(5) f = 12 GHz

Fig 6. Gain as a function of collector current; typical value

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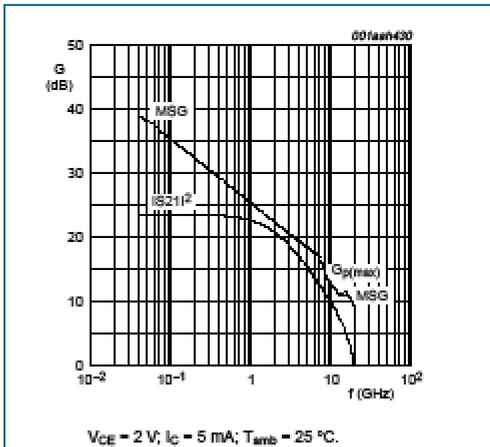
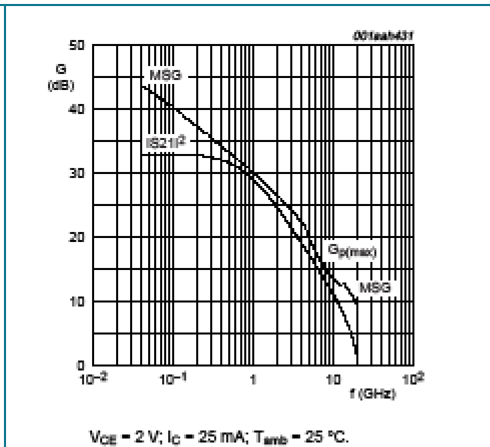


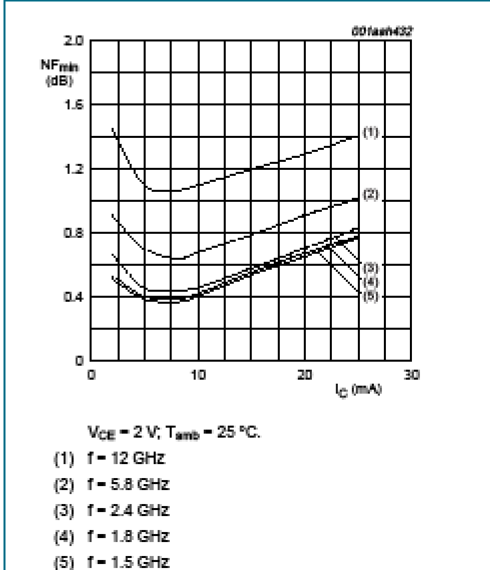
V_{CE} = 2 V; I_C = 5 mA; T_{amb} = 25 °C.

Fig 7. Gain as a function of frequency; typical values



V_{CE} = 2 V; I_C = 25 mA; T_{amb} = 25 °C.

Fig 8. Gain as a function of frequency; typical values



V_{CE} = 2 V; T_{amb} = 25 °C.

(1) f = 12 GHz

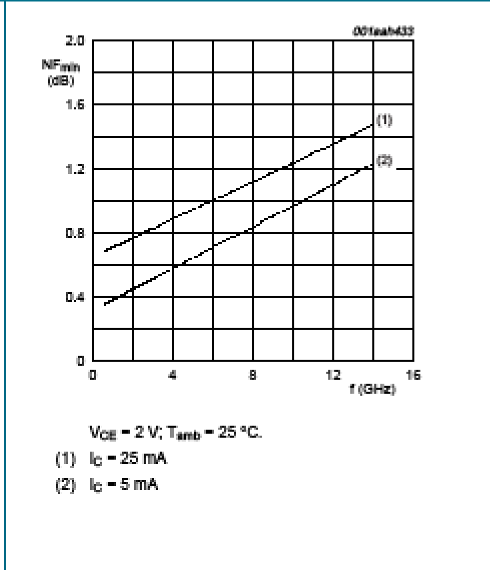
(2) f = 5.8 GHz

(3) f = 2.4 GHz

(4) f = 1.8 GHz

(5) f = 1.5 GHz

Fig 9. Minimum noise figure as a function of collector current; typical values



V_{CE} = 2 V; T_{amb} = 25 °C.

(1) I_C = 25 mA

(2) I_C = 5 mA

Fig 10. Minimum noise figure as a function of frequency; typical values

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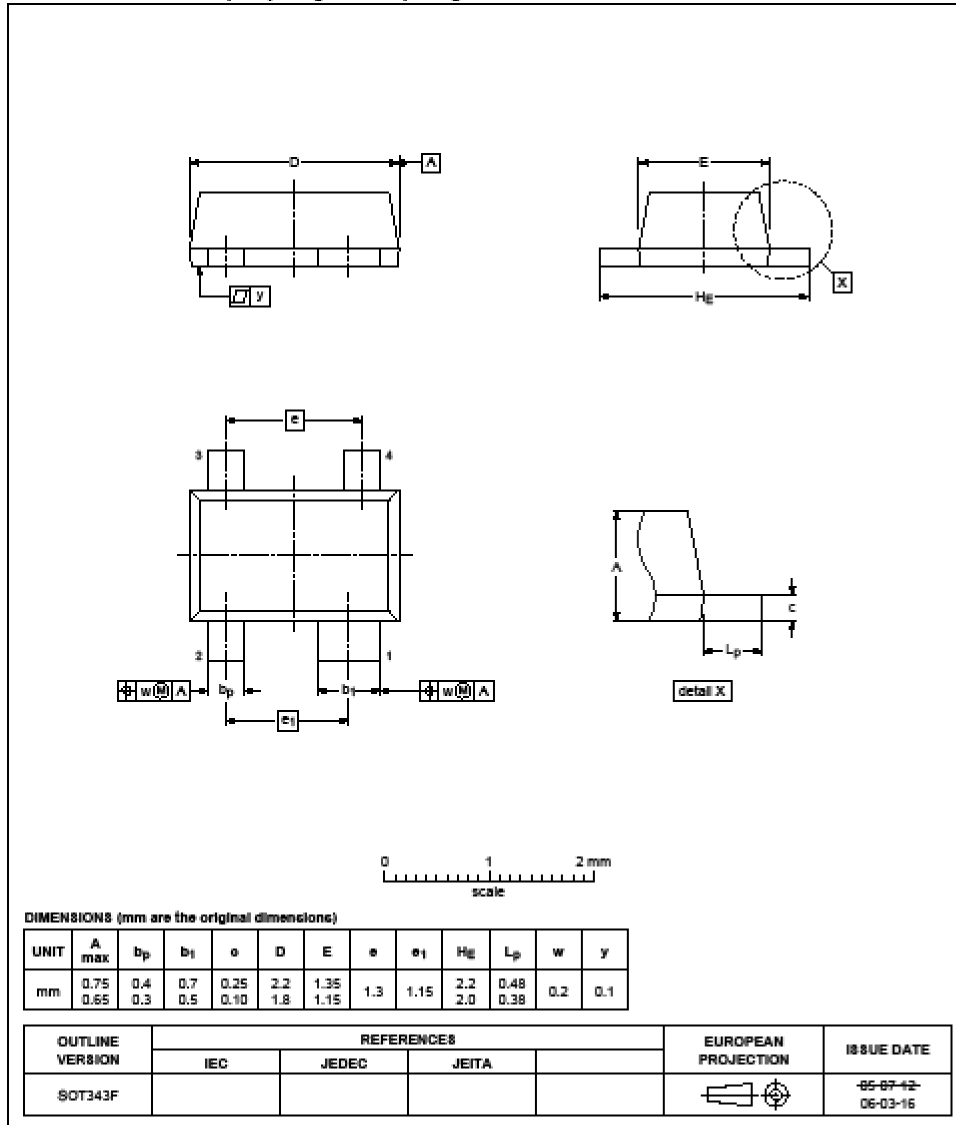
8. Package outline

Plastic surface-mounted flat pack package; reverse pinning; 4 leads — SOT343F



DIMENSIONS (mm are the original dimensions)

UNIT	A max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.75 0.65	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.48 0.38	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT343F						~~05-07-12~~ 06-03-16

Fig 11. Package outline SOT343F

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9. Abbreviations

Table 8. Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
DBS	Direct Broadcast Satellite
DC	Direct Current
DRO	Dielectric Resonator Oscillator
LNA	Low Noise Amplifier
LNB	Low Noise Block
Ka	Kurtz above
NPN	Negative-Positive-Negative
RF	Radio Frequency
WLAN	Wireless Local Area Network

10. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BFU725F_N1_1	20090713	Product data sheet	-	-

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11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 13 July 2009

Document identifier: BFU725F_N1_1

S-Parameters file for the device NXP BFU725F

Filename:	BFU725F	2V10mA	with noise					
MHz	S	MA	R	50				
Freq-MHz	S11-mag	S11-arg	S21-mag	S21-arg	S12-mag	S12-arg	S22-mag	S22-arg
40	0.93642	-2.84	25.66	177.01	0.002012	88.42	0.9987	-1.65
50	0.93093	-3.41	25.572	176.84	0.002085	87.38	0.9986	-2.07
60	0.93432	-3.97	25.613	176.35	0.002529	87.05	0.9961	-2.44
70	0.93268	-4.85	25.613	175.8	0.003045	88.83	0.99961	-3.11
80	0.9295	-5.46	25.536	175.36	0.003566	86.88	0.99719	-3.61
90	0.92706	-6.22	25.558	175.05	0.003946	86.94	0.99719	-4.13
100	0.92704	-7.01	25.523	174.36	0.004516	85.29	0.9965	-4.74
120	0.92424	-8.24	25.452	173.51	0.005245	83.44	0.99444	-5.55
140	0.92499	-9.73	25.415	172.44	0.006099	84.4	0.99447	-6.57
160	0.92812	-10.98	25.434	171.54	0.006919	83.86	0.99344	-7.47
180	0.92599	-12.33	25.364	170.49	0.007735	82.42	0.99046	-8.38
200	0.92589	-13.69	25.363	169.45	0.008692	82.07	0.98936	-9.4
220	0.92269	-15.11	25.276	168.34	0.009533	80.77	0.98623	-10.37
240	0.92185	-16.45	25.223	167.33	0.010364	80.67	0.98486	-11.32
260	0.91827	-17.74	25.131	166.31	0.011134	79.45	0.98175	-12.2
280	0.91459	-19.2	25.047	165.31	0.012038	78.75	0.97918	-13.2
300	0.911	-20.58	24.968	164.32	0.012813	78.06	0.97653	-14.09
320	0.90901	-21.85	24.883	163.38	0.013614	77.31	0.97389	-14.97
340	0.9072	-23.22	24.783	162.43	0.014434	76.68	0.97122	-15.89
360	0.90659	-24.55	24.728	161.47	0.015282	75.8	0.96799	-16.83
380	0.90589	-25.86	24.663	160.49	0.016071	75	0.96454	-17.75
400	0.90317	-27.17	24.597	159.47	0.016845	74.46	0.96135	-18.65
420	0.89984	-28.44	24.503	158.4	0.017616	73.62	0.95748	-19.52
440	0.89615	-29.69	24.391	157.41	0.018375	72.76	0.95268	-20.42
460	0.89178	-31	24.268	156.44	0.019162	72	0.94837	-21.31
480	0.88692	-32.31	24.146	155.46	0.019878	71.44	0.94483	-22.16
500	0.88305	-33.63	24.031	154.53	0.020592	70.7	0.94034	-22.99
550	0.87533	-36.77	23.723	152.18	0.022437	69.04	0.93009	-25.16
600	0.8692	-39.81	23.434	149.85	0.024235	67.21	0.91771	-27.32

650	0.85868	-42.83	23.109	147.56	0.025871	65.39	0.90403	-29.34
700	0.84469	-45.94	22.719	145.33	0.027418	63.82	0.89108	-31.27
750	0.83666	-48.91	22.361	143.31	0.028935	62.27	0.87845	-33.19
800	0.83098	-51.63	22.018	141.27	0.030475	60.8	0.86594	-35.18
850	0.81988	-54.42	21.664	139.17	0.031906	59.28	0.85125	-37.06
900	0.80691	-57.3	21.297	137.19	0.033218	57.88	0.83767	-38.7
950	0.79838	-60.17	20.951	135.28	0.034557	56.6	0.8256	-40.43
1000	0.79156	-62.83	20.63	133.38	0.03586	55.16	0.81183	-42.25
1050	0.78005	-65.41	20.275	131.42	0.037059	53.74	0.7963	-44
1100	0.76623	-68.08	19.894	129.61	0.038049	52.59	0.78252	-45.47
1150	0.75759	-70.69	19.539	127.87	0.039171	51.39	0.76999	-47.07
1200	0.74963	-73.11	19.206	126.12	0.040222	50.18	0.75704	-48.68
1250	0.73984	-75.44	18.855	124.37	0.041211	49.01	0.743	-50.23
1300	0.72695	-77.98	18.49	122.72	0.042101	47.92	0.72847	-51.57
1350	0.71869	-80.38	18.159	121.22	0.042964	46.97	0.71665	-52.91
1400	0.71299	-82.6	17.858	119.65	0.043874	45.96	0.70521	-54.37
1450	0.70339	-84.71	17.538	118.06	0.044666	44.88	0.69159	-55.81
1500	0.69254	-87.03	17.212	116.53	0.045386	43.9	0.67791	-57.05
1550	0.68427	-89.33	16.897	115.14	0.046097	43.09	0.66603	-58.23
1600	0.67828	-91.3	16.604	113.73	0.046822	42.22	0.65525	-59.52
1650	0.67065	-93.32	16.309	112.28	0.047522	41.35	0.64349	-60.82
1700	0.65996	-95.5	16.003	110.87	0.048087	40.45	0.63128	-62.01
1750	0.65293	-97.55	15.715	109.58	0.048672	39.71	0.62094	-63.06
1800	0.64844	-99.47	15.447	108.3	0.049341	39.03	0.61184	-64.16
1850	0.64169	-101.2	15.191	107.01	0.049901	38.23	0.60111	-65.35
1900	0.63262	-103.3	14.921	105.66	0.05041	37.4	0.58867	-66.51
1950	0.62583	-105.3	14.646	104.47	0.050848	36.87	0.57812	-67.41
2000	0.62105	-107.09	14.393	103.3	0.051341	36.24	0.56984	-68.41
2050	0.61545	-108.7	14.164	102.04	0.051912	35.53	0.56056	-69.68
2100	0.60778	-110.41	13.914	100.89	0.052309	34.92	0.55005	-70.58
2150	0.60082	-112.35	13.664	99.76	0.052742	34.36	0.54083	-71.45
2200	0.59907	-114.08	13.453	98.73	0.053194	33.88	0.53332	-72.31
2250	0.59476	-115.6	13.241	97.62	0.053645	33.23	0.52561	-73.32

2300	0.58617	-117.29	13.016	96.41	0.05402	32.6	0.51634	-74.42
2350	0.57947	-119.18	12.795	95.36	0.054375	32.12	0.50736	-75.23
2400	0.57689	-120.65	12.594	94.43	0.054762	31.72	0.50052	-75.89
2450	0.57414	-122.06	12.409	93.42	0.055209	31.2	0.49421	-76.86
2500	0.56811	-123.77	12.216	92.32	0.055616	30.59	0.48515	-77.99
2600	0.55995	-126.86	11.818	90.46	0.056143	29.76	0.47048	-79.47
2700	0.55259	-129.66	11.486	88.54	0.056911	28.8	0.45877	-81.44
2800	0.546	-132.61	11.132	86.75	0.057321	28.08	0.44326	-82.72
2900	0.54156	-135.35	10.839	84.93	0.058038	27.26	0.43182	-84.66
3000	0.53521	-138.27	10.519	83.25	0.05844	26.56	0.41808	-86
3100	0.53099	-140.79	10.273	81.48	0.059099	25.89	0.40724	-87.75
3200	0.52513	-143.69	9.9729	79.85	0.059499	25.39	0.39474	-88.94
3300	0.52103	-146.06	9.7438	78.24	0.060232	24.74	0.38762	-90.43
3400	0.51566	-148.83	9.4918	76.58	0.060644	24.13	0.37486	-91.71
3500	0.51464	-151.06	9.2803	74.98	0.061343	23.61	0.36701	-93.3
3600	0.50742	-153.67	9.0289	73.31	0.061612	22.97	0.35672	-94.89
3700	0.50647	-155.74	8.8471	71.84	0.062274	22.55	0.35062	-96.07
3800	0.50186	-158.37	8.6281	70.22	0.062723	21.9	0.33895	-97.55
3900	0.50086	-160.37	8.4391	68.76	0.063285	21.59	0.33247	-98.84
4000	0.49548	-162.89	8.2406	67.21	0.063759	20.95	0.32458	-100.44
4100	0.49616	-164.88	8.0746	65.77	0.064266	20.6	0.31754	-101.57
4200	0.49171	-167.15	7.8946	64.24	0.064778	20.05	0.31061	-103.3
4300	0.49105	-169.2	7.7297	62.93	0.065179	19.73	0.30447	-104.27
4400	0.48864	-171.36	7.5781	61.42	0.065767	19.26	0.29564	-105.92
4500	0.48899	-173.24	7.426	60.07	0.066218	18.92	0.28903	-107.24
4600	0.48595	-175.26	7.2763	58.56	0.066743	18.4	0.28552	-108.95
4700	0.48644	-177.28	7.1343	57.28	0.067215	18.03	0.27721	-109.75
4800	0.4848	-179.24	7.0019	55.75	0.067777	17.51	0.27158	-111.78
4900	0.48225	178.7	6.8592	54.47	0.068135	17.27	0.2657	-112.9
5000	0.48294	177.03	6.74	53.06	0.068812	16.8	0.26125	-114.38
5200	0.48275	173.33	6.4978	50.44	0.069904	16.09	0.2531	-117.41
5400	0.48304	169.63	6.2811	47.78	0.070885	15.39	0.23858	-120.51
5600	0.48205	166.13	6.0637	45.22	0.071965	14.67	0.23313	-123.09

5800	0.48314	162.71	5.8685	42.57	0.073003	13.84	0.22311	-126.71
6000	0.4861	159.38	5.6848	40.03	0.074143	13.05	0.21318	-130.16
6200	0.485	156.22	5.5009	37.64	0.07516	12.53	0.20661	-132.55
6400	0.48794	152.88	5.3352	35.11	0.076271	11.85	0.19908	-137.24
6600	0.49034	149.69	5.1832	32.62	0.077523	11.05	0.19124	-140.41
6800	0.49229	146.84	5.0304	30.13	0.078758	10.37	0.18608	-144.05
7000	0.49507	144	4.8913	27.7	0.080066	9.63	0.18149	-148.87
7200	0.49821	140.92	4.7565	25.28	0.081273	8.79	0.17261	-152.63
7400	0.49993	138.31	4.6224	22.89	0.082465	8.05	0.17046	-156.92
7600	0.50359	135.87	4.5156	20.67	0.084085	7.39	0.16808	-161.06
7800	0.50975	133.01	4.401	18.11	0.085466	6.44	0.16368	-166.3
8000	0.51435	130.11	4.2968	15.67	0.086924	5.47	0.16514	-170.91
8200	0.5207	127.4	4.1896	13.2	0.08826	4.5	0.16027	-177.19
8400	0.5231	125.07	4.079	11	0.089537	3.67	0.15824	178.46
8600	0.52793	122.35	3.9999	8.52	0.091204	2.63	0.16038	174
8800	0.53705	119.9	3.9135	6.17	0.092455	1.84	0.16114	168.88
9000	0.5425	117.41	3.8219	3.72	0.093953	0.84	0.16286	164.84
9200	0.54845	115.01	3.7397	1.33	0.095791	-0.2	0.16727	157.98
9400	0.55528	112.22	3.6538	-0.96	0.097421	-1.19	0.17008	153.15
9600	0.56204	109.77	3.5745	-3.48	0.098769	-2.54	0.17194	148.28
9800	0.56826	107.41	3.4972	-5.71	0.099847	-3.54	0.17576	142.42
10000	0.57055	104.82	3.4404	-7.72	0.10204	-4.16	0.1743	141.11
10500	0.58662	99.67	3.2494	-14.14	0.10605	-7.62	0.20377	128.08
11000	0.60957	93.81	3.1233	-19.95	0.11028	-10.76	0.22286	116.68
11500	0.62557	88.76	2.9675	-25.66	0.11394	-13.58	0.24197	108.39
12000	0.64352	83.29	2.7788	-31.59	0.11722	-17.44	0.28098	99.7
12500	0.6678	78.47	2.6718	-37.68	0.12073	-20.9	0.30819	91.59
13000	0.68869	73.59	2.5314	-43.91	0.12455	-25.01	0.33822	85.48
13500	0.71944	68.5	2.4177	-49.11	0.12787	-29.05	0.37395	79.02
14000	0.73765	62.22	2.3058	-56.16	0.12948	-33.47	0.41297	72.29
14500	0.7463	57.61	2.173	-62.19	0.13091	-38.03	0.45189	67.45
15000	0.77207	53.66	2.0369	-67.48	0.13249	-41.35	0.48927	61.73
15500	0.78186	48.93	1.9262	-73.4	0.13306	-46.17	0.53089	56.4

16000	0.80181	45.19	1.8179	-78.51	0.13235	-50.35	0.56614	51.23
16500	0.83489	41.34	1.7329	-84.03	0.13164	-53.07	0.59945	46.02
17000	0.84366	35.84	1.6318	-90.29	0.13252	-58.23	0.62715	41.47
17500	0.87344	32	1.5356	-95.85	0.12867	-62.37	0.65762	37.32
18000	0.88323	27.94	1.4282	-101.33	0.12674	-63.36	0.67776	32.34
18500	0.87778	23.58	1.336	-106.2	0.12902	-65.21	0.69711	28.88
19000	0.90226	20.45	1.2392	-110.67	0.13074	-68.23	0.72466	25.54
19500	0.90564	16.66	1.1687	-115.28	0.13325	-73.79	0.73892	22.15
20000	0.92285	12.38	1.0892	-120.2	0.1305	-74.64	0.76863	19.96
20500	0.93441	7.64	1.0268	-124.33	0.13654	-81.18	0.79362	16.93
21000	0.91128	4.38	0.9698	-129.13	0.14042	-84.42	0.80452	13.76
21500	0.87328	2.31	0.90941	-131.83	0.14248	-89.64	0.83319	12.99
22000	0.88198	-0.03	0.85082	-137.11	0.1351	-99.39	0.85549	7.41
22500	0.89283	-1.44	0.80582	-140.66	0.12664	-101.23	0.85124	6.97
23000	0.90704	-3.74	0.76663	-146.03	0.12559	-106.72	0.88514	3.32
23500	0.93185	-6.38	0.69754	-150.65	0.11695	-109.81	0.87502	0.65
24000	0.93281	-9.75	0.63473	-154.69	0.11436	-113.64	0.91415	-0.14
24500	0.88163	-8.26	0.61853	-154.97	0.10989	-114.88	0.91141	-4.09
25000	0.93991	-3.58	0.59939	-155.98	0.10798	-112.4	0.91034	-5.17

Noise Parameter file

!	Noise	Parameters	BFU725F	
! Freq-MHz	F_{min}-dB	Γ_{opt}-mag.	Γ_{opt}-Ang.	R_n/50
600	0.36	0.5098	6.89	0.183
700	0.36	0.5009	8.73	0.179
800	0.37	0.4921	10.57	0.176
900	0.38	0.4835	12.42	0.172
1000	0.38	0.475	14.28	0.169
1100	0.39	0.4666	16.14	0.165
1200	0.4	0.4583	18.01	0.162
1300	0.4	0.4501	19.88	0.159
1400	0.41	0.4421	21.76	0.156
1500	0.41	0.4341	23.65	0.153
1600	0.42	0.4263	25.54	0.15
1700	0.43	0.4186	27.44	0.148
1800	0.43	0.4111	29.35	0.145
1900	0.44	0.4036	31.26	0.142
2000	0.45	0.3963	33.18	0.14
2200	0.46	0.382	37.03	0.135
2400	0.47	0.3681	40.91	0.13
2600	0.49	0.3547	44.81	0.126
2800	0.5	0.3418	48.73	0.122
3000	0.51	0.3294	52.68	0.119
4000	0.58	0.2744	72.8	0.105
5000	0.64	0.2312	93.53	0.097
5400	0.67	0.2172	102	0.095
5800	0.7	0.2051	110.56	0.094
6000	0.71	0.1998	114.87	0.093
7000	0.77	0.1803	136.83	0.094
8000	0.84	0.1726	159.39	0.098
9000	0.91	0.1767	-158.09	0.104
10000	0.97	0.1927	-142.3	0.11
11000	1.04	0.2204	-126.51	0.117

11500	1.07	0.2388	-118.62	0.12
12000	1.1	0.2601	-110.72	0.123
12500	1.13	0.2843	-102.83	0.125
13000	1.17	0.3115	-94.93	0.126
14000	1.23	0.3748	-79.15	0.127

ROGERS CORPORATION

Advanced Circuit Materials

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Data Sheet
RT/duroid® 5870/5880 Laminates

RT/duroid® 5870 /5880 High Frequency Laminates

Features:	
•	Lowest electrical loss for reinforced PTFE material.
•	Low moisture absorption.
•	Isotropic
•	Uniform electrical properties over frequency.
•	Excellent chemical resistance.
Some Typical Applications:	
•	Commercial Airline Telephones
•	Microstrip and Stripline Circuits
•	Millimeter Wave Applications
•	Military Radar Systems
•	Missile Guidance Systems
•	Point to Point Digital Radio Antennas

RT/duroid® 5870 and 5880 glass microfiber reinforced PTFE composites are designed for exacting stripline and microstrip circuit applications.

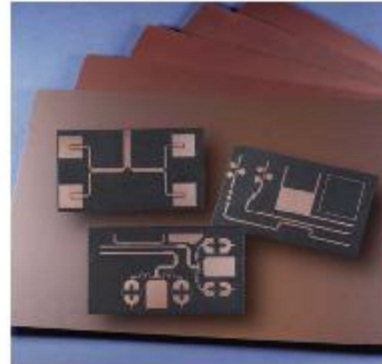
Glass reinforcing microfibers are randomly oriented to maximize benefits of fiber reinforcement in the directions most valuable to circuit producers and in the final circuit application.

The dielectric constant of RT/duroid 5870 and 5880 laminates is uniform from panel to panel and is constant over a wide frequency range.
Its low dissipation factor extends the usefulness of RT/duroid 5870 and 5880 laminates to Ku-band and above.

RT/duroid 5870 and 5880 laminates are easily cut, sheared and machined to shape. They are resistant to all solvents and reagents, hot or cold, normally used in etching printed circuits or in plating edges and holes.

Normally supplied as a laminate with electrodeposited copper of ¼ to 2 ounces/ft.^{2} (8 to 70μm) on both sides, RT/duroid 5870 and 5880 composites can also be clad with rolled copper foil for more critical electrical applications. Cladding with aluminum, copper or brass plate may also be specified.

When ordering RT/duroid 5870 and 5880 laminates, it is important to specify dielectric thickness, tolerance, rolled or electrodeposited copper foil, and weight of copper foil required.



The world runs better with Rogers.®

RT/duroid 5870/5880 Laminates

PROPERTY	TYPICAL VALUE [2]				DIRECTION	UNITS[3]	CONDITION	TEST METHOD
	RT/duroid 5870		RT/duroid 5880					
Dielectric Constant, ε_r [1]	2.33 2.33 ± 0.02 spec.		2.20 2.20 ± 0.02 spec.		Z Z		C24/23/50 C24/23/50	1 MHz IPC-TM-650 2.5.5.3 10 GHz IPC-TM 2.5.5.5
Dissipation Factor, tan δ	0.0005 0.0012		0.0004 0.0009		Z Z		C24/23/50 C24/23/50	1 MHz IPC-TM-650, 2.5.5.3 10 GHz IPC-TM-2.5.5.5
Thermal Coefficient of ε_r	-115		-125			ppm/°C	-50 - 150°C	IPC-TM-650, 2.5.5.5
Volume Resistivity	2 X 10^7		2 X 10^7		Z	Mohm cm	C96/35/90	ASTM D257
Surface Resistivity	2 X 10^7		3 X 10^7		Z	Mohm	C/96/35/90	ASTM D257
Tensile Modulus	Test at 23°C	Test at 100°C	Test at 23°C	Test at 100°C		MPa (kpsi)	A	ASTM D638
	1300 (189)	490 (71)	1070 (156)	450 (65)	X			
	1280 (185	430 (63)	860 (125)	380 (55)	Y			
ultimate stress	50 (7.3)	34 (4.8)	29 (4.2)	20 (2.9)	X			
	42 (6.1)	34 (4.8)	27 (3.9)	18 (2.6)	Y			
ultimate strain	9.8	8.7	6.0	7.2	X	%		
	9.8	8.6	4.9	5.8	Y			
Compressive Modulus	1210 (176)	680 (99)	710 (103)	500 (73)	X	MPa (kpsi)	A	ASTM D695
	1360 (198)	860 (125)	710 (103)	500 (73)	Y			
	803 (120)	520 (76)	940 (136)	670 (97)	Z			
ultimate stress	30 (4.4)	23 (3.4)	27 (3.9)	22 (3.2)	X			
	37 (5.3)	25 (3.7)	29 (5.3)	21 (3.1)	Y			
	54 (7.8)	37 (5.3)	52 (7.5)	43 (6.3)	Z			
ultimate strain	4.0	4.3	8.5	8.4	X	%		
	3.3	3.3	7.7	7.8	Y			
	8.7	8.5	12.5	17.6	Z			
Deformation Under Load, Test at 150°C			1.0		Z	%	24hr/14 MPa (2 Kpsi)	ASTM D621
Heat Distortion Temperature	>260 (>500)		>260 (>500)		X,Y	°C (°F)	1.82 MPa (264 psi)	ASTM D648
Specific Heat	0.96 (0.23)		0.96 (0.23)			J/g/K (cal/g/C)		Calculated
Moisture Absorption	13 (0.015)		13 (0.015)			mg (%)	.062" (1.6mm) D24/23	ASTM D570
Thermal Conductivity	0.22		0.20		Z	W/m/K	80°C	ASTM C518
Coefficient of Thermal Expansion	22 28 173		31 48 237		X Y Z	ppm/°C	0-100°C	ASTM D3386
Td	500		500			°C TGA		ASTM D3850
Density	2.2		2.2					ASTM D792
Copper Peel	20.8 (3.7)		22.8 (4.0)			pli (N/mm)	after solder float	IPC-TM-650 2.4.8
Flammability	V-0		V-0					UL94
Lead-Free Process Compatible	Yes		Yes					

[1] Specification values are measured per IPC-TM-650, method 2.5.5.5 @ ~10GHz, 23°C. Testing based on 1 oz. electrodeposited copper foil. ε_r values and tolerance reported by IPC-TM-650 method 2.5.5.5 are the basis for quality acceptance, but for some products these values may be incorrect for design purposes, especially microstrip designs. We recommend that prototype boards for a new designs be verified for desired electrical performance.
[2] Typical values should not be used for specification limits, except where noted.
[3] SI unit given first with other frequently used units in parentheses.
[4] References: Internal TR's 1430, 2224, 2854. Test were at 23°C unless otherwise noted.

STANDARD THICKNESS		STANDARD PANEL SIZE	STANDARD COPPER CLADDING
0.005" (0.127mm), 0.010" (0.254mm), 0.015" (0.381mm), 0.020" (0.508mm),	0.031" (0.787mm) 0.062" (1.575mm) 0.125" (3.175mm)	18" X 12" (457 X 305mm) 18" X 24" (457 X 610mm) 18" X 36" (457 X 915mm) 18" X 48" (457 X 1.224m)	5 µm, ¼ oz. (9 µm) electrodeposited copper foil. ½ oz. (17µm), 1 oz. (35µm), 2 oz. (70µm) electrodeposited and rolled copper foil.

The information in this data sheet is intended to assist you in designing with Rogers' circuit material laminates. It is not intended to and does not create any warranties express or implied, including any warranty of merchantability or fitness for a particular purpose or that the results shown on this data sheet will be achieved by a user for a particular purpose. The user should determine the suitability of Rogers' circuit material laminates for each application.

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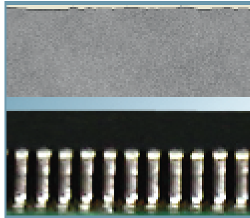
Revised 05/2010, 0905-0510-0.5CC Publication #92-101

APPENDIX 2

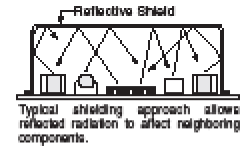
The Leading Source for EMI Shielding
Reliable Board, Enclosure and Cable Solutions



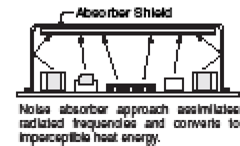
electromagnetic radio wave absorbers

Radio frequencies emanating from electronic components such as the printed circuit board sketch at the right are addressed in three ways: sometimes no shielding is required; a reflective shield in the form of a local cover for the components, or the entire electronic enclosure can be fitted up as a shield; an absorber pad shield which soaks up the RF and converts it to imperceptible heat energy.

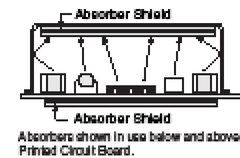
The latter Absorber Shield method deals with the unwanted RF energy right at the source and prevents re-radiation and reflection of the signals so that neighboring components are unaffected; also, second, third and fourth order harmonics are nullified or greatly minimized.



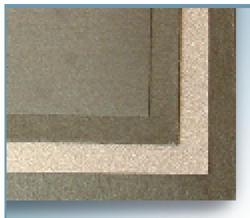
Typical shielding approach allows reflected radiation to affect neighboring components.



Noise absorber approach assimilates radiated frequencies and converts to imperceptible heat energy.



Absorbers shown in use below and above Printed Circuit Board.



EMC wave absorber

40MHz TO 5GHz EA SERIES. The EA series is a high frequency noise absorber in a range of formulations addressing 40MHz to 5GHz radiations from electronic components. It has a multi-layered structure of screened coating matrixes adjusted for discrete impedance matching to absorb electromagnetic waves at various peak frequencies depending on which of the seven different constructions is used.

applications:

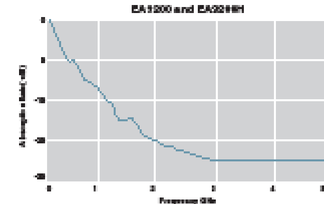
PCB's, PCB components, electronic enclosures, shielded boxes, all microprocessor based electronic, EDP, telecom, scientific, medical, architectural shielding, RF test chambers, shielded facilities

extra wideband series

40MHz TO 5GHz @ 3.2GHZ PEAK. This all-around universal wideband formula is available in a standard temperature type and a high temperature type (up to 200°C). Excellent performance from 40MHz to 5GHz.

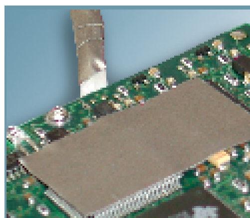
Material Characteristic		Measure		
Frequency range		40 MHz - 5 GHz		
Peak frequency		3.2 GHz		
Temperature range		-20°C to 100°C and -10°C to 200°C (high temp)		
Flammability rating		UL94-V0		
Adhesive:	standard temp.	0°F to 180°F	-18°C to 83°C	ASTM D-3575
	high temp.	50°F to 312°F	10°C to 200°C	ASTM D-3575
	tack	8.4 p.s.i. (stainless steel standard)		ASTM D-3575
		8.3 p.s.i. (stainless steel high temperature)		ASTM D-3575
	shear	300+ hrs. @ 2 p.s.i. @ 22°C		ASTM D-3575
Dimensions:	standard	8.25" W x 15.75 " L x .004" max.	209,6 x 400,0 x 0,10	
	maximum	3'-0" W x 65'-0" L x .004" max	1,0 x 20,0 M x 0,10	

typical absorption rate



PART No.	Width		Length*		Thickness		Frequency Range	Peak Frequency – Attenuation
EA3200	8.25	209,6	15.75	400,0	.005	0,13	40 MHz to 5 GHz	3.2 GHz @ -31.3 dB
EA3200H (hi temp)	8.25	209,6	15.75	400,0	.005	0,13	40 MHz to 5 GHz	3.2 GHz @ -31.3 dB

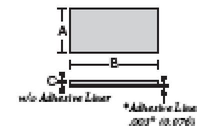
Available in standard rolls 8.25" 210mm x 65'-0" 20M



shielding patches®

FOR PCB COMPONENTS AND WIRE CIRCUITS. A quick and easy way to gain 1 to 2 dB without invasive circuit changes. The EA3200H RF absorber matrix provides a measurable effect from 40MHz to 5GHz depending on frequency, existing circuit load, and area covered by the patch*. Peak performance is at 3.2GHz to 5.0GHz.

Installs simply by removing protective adhesive liner. Convenient 6.00" x 8.00" *(152 x 203mm)* sheets with (24) patches per sheet.



PART No.	A		B		C		Frequency – Attenuation
EA3200H-SP12	1.00	25,4	1.937	49,2	.005	0,13	40MHz - 5GHz: peak @ 3.2GHz @ -31.2dB

"H" signifies high temperature version. See specifications above.

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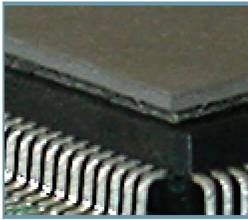


standard series – 50 MHz to 1 GHz

Material Characteristic		Measure		
Frequency range		50 MHz - 1 GHz		
Peak frequency choices		100, 300, 400, 500 or 800 MHz		
Temperature range		-20˚C to 100˚C		
Flammability rating		UL94-V0		
Adhesive:	temperature	0˚F to 180˚F	-18˚C to 83˚C	ASTM D-3575
	tack	8.4 p.s.i. (stainless steel)		ASTM D-3575
	shear	300+ hrs. @ 2 p.s.i. @ 22˚C		ASTM D-3575
Dimensions:	standard	15.75" W x 15.75 " L x .020" max.	400,0 x 400,0 x 0,50	
	maximum	3'-0" W x 65'-0" L x .020" max	1,0 x 20,0 M x 0,50	

PART No.	Width		Length*		Thickness		Frequency Range	Peak Frequency – Attenuation
EA100	15.75	400,0	15.75	400,0	.002	0,05	-5 dB min. @ 50 MHz to 1 GHz	100 MHz @ -17.3 dB
EA300	15.75	400,0	15.75	400,0	.007	0,18	-5 dB min. @ 50 MHz to 1 GHz	300 MHz @ -17.6 dB
EA400	15.75	400,0	15.75	400,0	.012	0,30	-5 dB min. @ 50 MHz to 1 GHz	400 MHz @ -17.2 dB
EA500	15.75	400,0	15.75	400,0	.020	0,50	-5 dB min. @ 50 MHz to 1 GHz	500 MHz @ -17.8 dB
EA800	15.75	400,0	15.75	400,0	.014	0,36	-5 dB min. @ 50 MHz to 1 GHz	800 MHz @ -17.9 dB

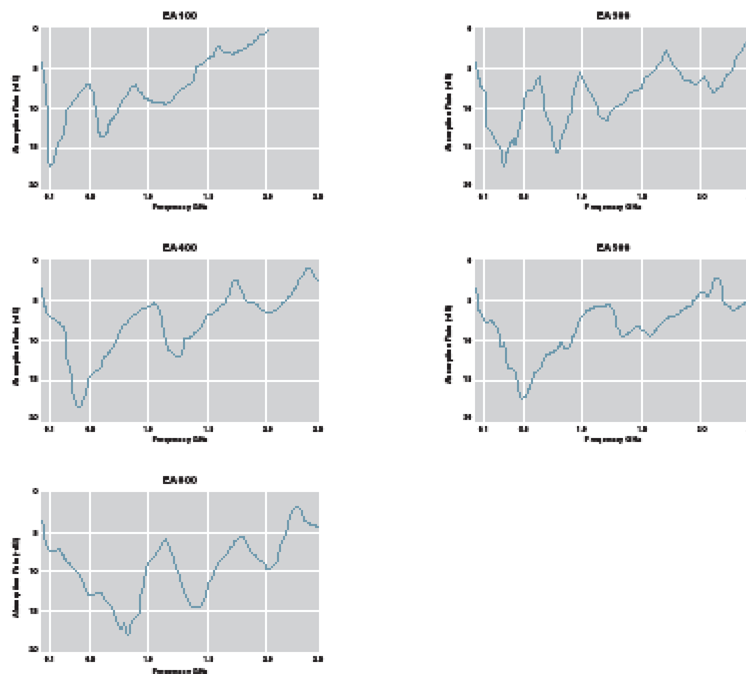
*Available in standard rolls 15.75 400mm x 65'-0" 20M

typical absorption rate by part number

The following data displays the insertion loss characteristics of each formula of absorber material by part number. Of particular interest in engineering a given application is the peak absorption frequency and its correlation to the part number nomenclature; i.e., the peak frequency of the EA300 material is 300MHz. Of course, any of the formulations can be used for neighboring frequencies – in the case of EA300, a logical selection can be made for 200MHz or 400MHz situations.

Note that laminations of multiple part numbers will effectively yield a combination of results.

EMC standard series: typical absorption rate by part number



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