Pocket Beamformer (PoBe) on FPGA

STUDENT PROJECT

By

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Abstract

The Pocket Beamformer (PoBe) is an FPGA based digital design that implements the beamforming algorithm for 2-4 antennas required for pulsar studies at the Giant Metrewave Radio Telescope (GMRT). The PoBe is an add-on to the Pocket Correlator (PoCo) which is a 2-4 antenna design that is used for correlation and has been developed a part of the GMRT upgrade. The PoBe will be the first beamformer of its kind to be working at a bandwidth of 400 MHz on the ROACH board. This project report explains the PoBe digital design in terms of modification on PoCo, beamforming algorithm and packetised design. It demonstrates the use of a 10Gbps network link for faster integration necessary for beamforming. The report breifly describes depacketisation and offline data processing. Results of sky tests performed with the PoBe are also provided suggesting the beamformer is functional.

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Chapter 1

Introduction

The aim of this project is to design and implement a beamforming algorithm on FPGA. Beamforming is a standard signal processing technique used to control the directivity of the reception or transmission of a signal. This work carries out beamforming targetting the field of radio astronomy, to receive data from a source using an array of antennas at the Giant Metrewave Radio Telescope (GMRT). Beamforming hardware was implementated using the Center for Astronomy Signal Processing and Electronics Research (CASPER) tool flow.

The introductory section will be giving a brief overview into radio astronomy, the GMRT, beamforming and CASPER technology. The final Section 1.5 will discuss the design approach in implementing the beamformer on FPGA.

1.1 Radio Astronomy

Radio astronomy is the study of radio waves originating outside the earth [1]. Since its discovery in the 1930's by Karl Jansky, the field of radio astronomy has revolutionized our view of the sky. This is because radio astronomy allows us to see things that are not detectable in optical astronomy. Radio astronomy has contributed immensely to astronomical knowledge, particularly with the discovery of several classes of new objects, including pulsars, quasars and radio galaxies.

Over the years, radio astronomy has seen major changes in engineering and instrumentation techniques. Traditionally a radio telescope was a huge single dish directive antenna. Due to various constraints, the big dish antenna has been superceded by multiple smaller antennas that combine signals to effectively make a larger radio telescope. This is done by means of radio interferometry. Interferometry not only increases the signal collected but also improves resolution. The Giant Metrewave Radio Telescope (GMRT) [2] is an example of this new generation of telescopes.

1.2 GMRT

The Giant Metrewave Radio Telescope, located near Pune in India, is the world's largest array of radio telescopes at metre wavelengths. It is operated by the National Centre for Radio Astrophysics, a part of the Tata Institute of Fundamental Research, Mumbai.

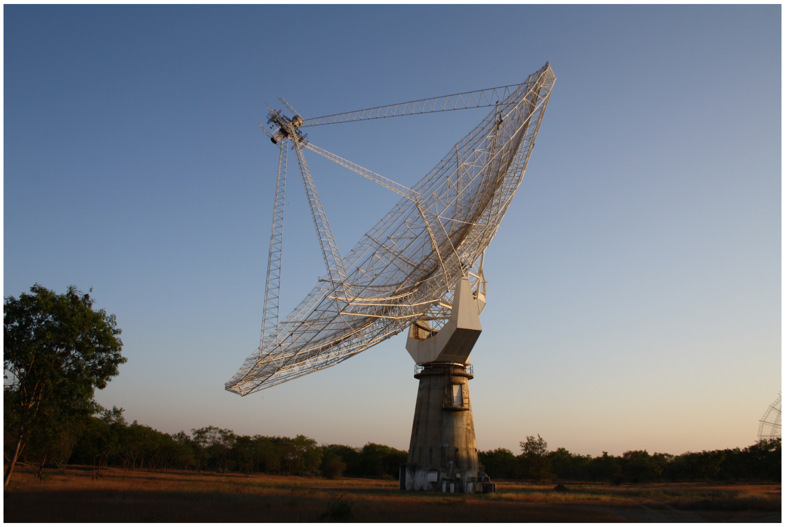


Figure 1.1: C8 Antenna at GMRT Central Square
(Photo courtesy of Dipak Buch)

The GMRT contains 30 fully steerable telescopes, each 45 metres in diameter with the reflector made of wire rope stretched between metal struts in a parabolic configuration. This configuration works fine as the telescope operates at long wavelengths (21 cm and above). Every antenna has four different receivers mounted at the focus. Each individual receiver assembly can rotate, enabling the user to select any of them for the observation. GMRT antennas operate in five frequency bands, centered at 153, 233, 327, 610, and 1420 MHz.

Out of the 30 telescopes at GMRT, fourteen telescopes are randomly arranged in the central square of 1 km by 1 km in size. Rest sixteen telescopes are arranged in three arms of a nearly "Y"-shaped array each having a length of 14 km from the array centre. Therefore GMRT can act as an interferometer which uses a technique known as aperture synthesis to make images of radio sources. The maximum baseline in the array gives the telescope an angular resolution (the smallest angular scale that can be distinguished) of about 1 arc-second, at the frequency of neutral hydrogen.

Currently, the GMRT is undergoing an upgrade. As part of the upgrade, the GMRT plans to increase the bandwidth of the GMRT from the present value of 32 MHz to about 400 MHz as it would further increase the sensitivity by a factor of about $\sqrt{400/32}$. A larger bandwidth could be of great value in the L band, say 1000-1430 MHz. For pulsar studies this would be revolutionary and is likely to yield several major discoveries. [3]

1.3 Beamforming

In its essence, beamforming combines different signals, received from many antennas, and to form a single coherent signal, called a beam. As mentioned earlier, it allows us to give directionality to an array of non-directional antennas. Beamforming application in radio astronomy is mainly used for pulsar research.

A pulsar is a rapidly rotating, highly magnetised neutron star, which emits electromagnetic radiation from its poles. Similar to the behaviour of a lighthouse, the radiation is visible to us only if one of the poles points towards the Earth, and appears to us as a very regular series of pulses, with a period being as low as milliseconds. Pulsars are weak radio sources, and their individual pulses often do not rise above the background noise that fills our universe [4]. Beamforming is the standard signal processing approach for their study.

There are two types of techniques that are required for phased arrays: incoherent and coherent beamforming.

1. **Incoherent Beamforming**:
   - Power Signal from N dishes are combined to give final signal
   - $\sqrt{N}$ improvement in sensitivity
   - Beamwidth of a single dish
   - Application in large scale pulsar search
   - The mathematical expression for incoherent beamforming is as shown:

     $$B_i = \Sigma(V_1^2 + V_2^2 + \cdots + V_N^2)$$

     where V is the voltage of an antenna, N is the number of antennas and B_i is the average power of the antennas or the incoherent beamformed output.
2. **Coherent Beamforming**:
   - Voltage signal from N dishes are added to get final signals
   - Requires proper phasing of array to compensate for the delay and phases
   - N times improvement in sensitivity
   - Beamwidth is much narrower than single dish, being λ/D, where D is the largest spacing between antennas in the array.
   - Application in studying individual pulsar, polarimetry etc.
   - The mathematical expression for coherent beamforming is as shown:

     $$B_c = \Sigma(V_1 + V_2 + \cdots + V_N)^2$$

     where V is the voltage of an antenna, N is the number of antennas and B_c is the average power of the antennas or coherent beamformed output.

This report will demonstrate the implementation of both types of beamforming on FPGA hardware.

1.4 CASPER

The Center for Astronomy Signal Processing and Electronics Research (CASPER) is a global collaboration dedicated to streamlining and simplifying the design flow of radio astronomy instrumentation by promoting design reuse through the development of platform-independent, open-source hardware and software [5]. The CASPER tool flow is better known as the MSSGE (Matlab/Simulink/System Generator/EDK) or bee_ xps tool flow. It is the platform for FPGA-based CASPER development and is the interface between several design and implementation environments.

CASPER instruments use reconfigurable open-source hardware built around Xilinx FPGAs. The GMRT uses Virtex 5 SXT95 based standalone FPGA processing board also called ROACH (Reconfigurable Open Architecture Computing Hardware). The ROACH board also has the following features:

- A separate PowerPC runs Linux and is used to control the board
- CX4/XAUI/10GbE Networks Interfacing Cards
- ADC2x1000-8: Dual 8-bit, 1000Msps (or single 8-bit 2000Msps), Atmel/e2v AT84AD001B ADC

1.5 Design Approach

The project was conceived to design the beamformer on the existing Pocket Correlator (PoCo) design. The two antennas PoCo design generates 4 outputs- self power spectra of antenna 1, self power spectra of antenna 2, the cross amplitude power spectra and cross phase spectra of both the antennas. The concept behind the Pocket Beamformer (PoBe) was to tap certain outputs from the PoCo system and to use them as building blocks for the beamformer design. The challenge in making the PoBe design is to integrate it at millisecond rate and packetise the beamformed output.

The digital design of the PoBe consists of implementing the beamforming algorithm mathematically (see Section 1.3) and packetising the design suitable for a 10GbE Network Interface card (NIC). The data packets are captured by an open source packet grabbing utility called GULP. For offline post-processing a basic ‘C’ programme was developed to make the data compatible for a GMRT developed software used for dedispersion and fast folding algorithm.

This report methodically discusses the implementation of the beamforming algorithm on ROACH board. Chapter 2 will describes the digital design and packetisation. Chapter 3 discusses the procedure and techniques used in the offline post-processing algorithms. Finally, Chapter 4 presents results and suggests improvements to the current PoBe design.

Chapter 2

Digital Design

This section focuses on the digital system design of the PoBe. The first sub-section explains the PoCo design. It is followed by a section detailing the digital system of the PoBe and a section that explains the packetised design. Finally, the resource utilisation of the ROACH is discussed.

2.1 PoCo Design

The PoCo design has been tested at the GMRT and is the digital-backend for an interferometer. A general system design is given below:

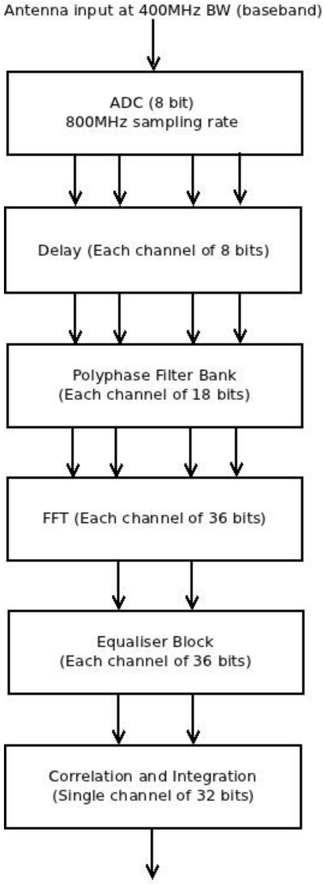

Antenna input at 400MHz BW (baseband)
ADC (8 bit)
800MHz sampling rate
Delay (Each channel of 8 bits)
Polyphase Filter Bank
(Each channel of 18 bits)
FFT (Each channel of 36 bits)
Equaliser Block
(Each channel of 36 bits)
Correlation and Integration
(Single channel of 32 bits)

Figure 2.1: PoCo System Diagram

Each block mentioned Figure. 2.1 is explained in brief below:

1. ADC: The ADCs interfaced to the ROACH board are ADC2x1000-8. They operate at 800MHz and give an 8 bit output through 4 channels each operating at 200MHz. This is done as the FPGA operates at 200MHz.

2. Delay: The coarse delay is usually taken to be 0 for simulation purposes but is taken into consideration during sky tests. In case of the PoBe, we account for delay in coherent mode and neglect it in the incoherent mode. The data rate at the output will be 4 channels of 8 bits at 200MHz.

3. PFB: The polyphase filter bank implements a hamming window. The PFB is used to reduce spectral leakage and to increase signal to noise ratio. The data rate at the output will be 4 channels each of 18 bits at 200MHz.

4. FFT: The FFT block used is FFT Biplex Real 4x (real-sampled biplex FFT). This block computes the real-sampled Fast Fourier Transform using the biplex FFT algorithm to use a complex core to transform two real streams.
   The data rate of operation at FFT output is 36 bits each at 400MHz. One of the streams gives even channels while the other gives odd channels. Each channel consists of an 18 bit real part and an 18 bit imaginary part. The channel itself is 36 bits with 17 bit binary point. This can be best explained from the Figure 2.2 below:

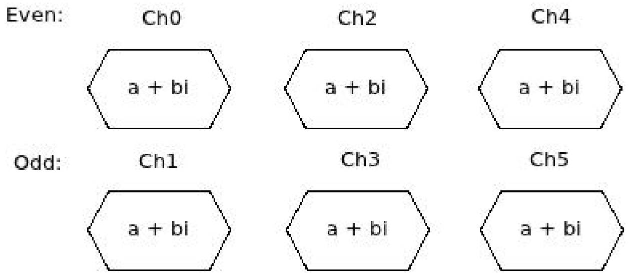


Figure 2.2: FFT Channel Output

   The FFT operation is performed during the period of a synchronisation pulse which is of 0.89s at 300MHz bandwidth. This period is equal to 2^{19} FFT cycles. We calculate this by:

$$\frac{2^{27}\times 4}{2^{10}}$$

   where 2^{27} is the data transferred during a synchronisation pulse, 2^{10} is the 1K point FFT and 4 are the 4 input channels in to the FFT block. In addition to this, a 1K point FFT requires 256 clock cycles.

5. Correlation and Integration: The correlator block in the design performs the product of voltages of two channels. The output of the correlator is 8 bits. This is fed to an integrator which gives a 32 bit output. The typical integration time is 1s.
   After integration, the data is fed into RAM of depth 256 locations. The following channels require the RAM specifications bas follows:

   - A1: 2 RAMs-one for real-even and the other for real-odd
   - A2: 2 RAMs-one for real-even and the other for real-odd

- A1A2: 4 RAMs-one for real-even, one for real-odd, one for imaginary-even and the last for imaginary-odd

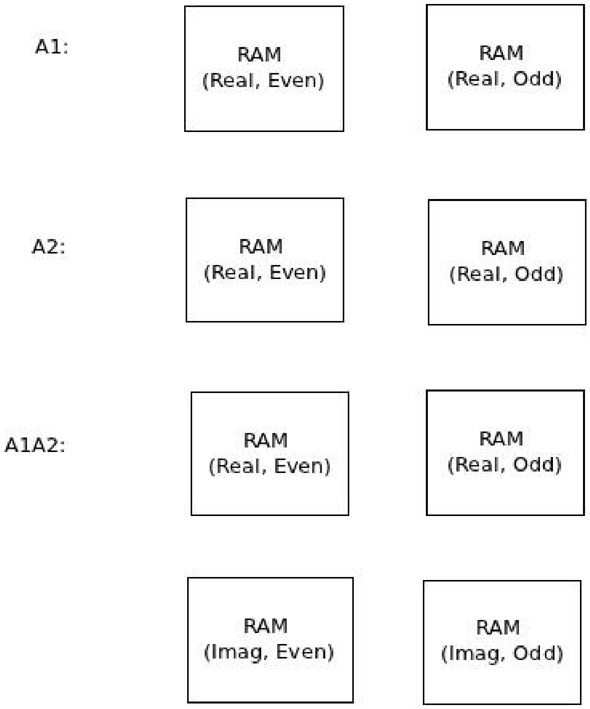


Figure 2.3: RAM Data Configuration

The PoCo design finds its application at the GMRT as a prototype for the large bandwidth ROACH based correlator.

2.2 PoBe Design

2.2.1 Beamformer Implementation

As mentioned previously, the PoBe design is a supplement to the PoCo digital system. The proposed idea was to tap required outputs from PoCo and then process the beamforming alogrithm. This is explained through the diagram below:

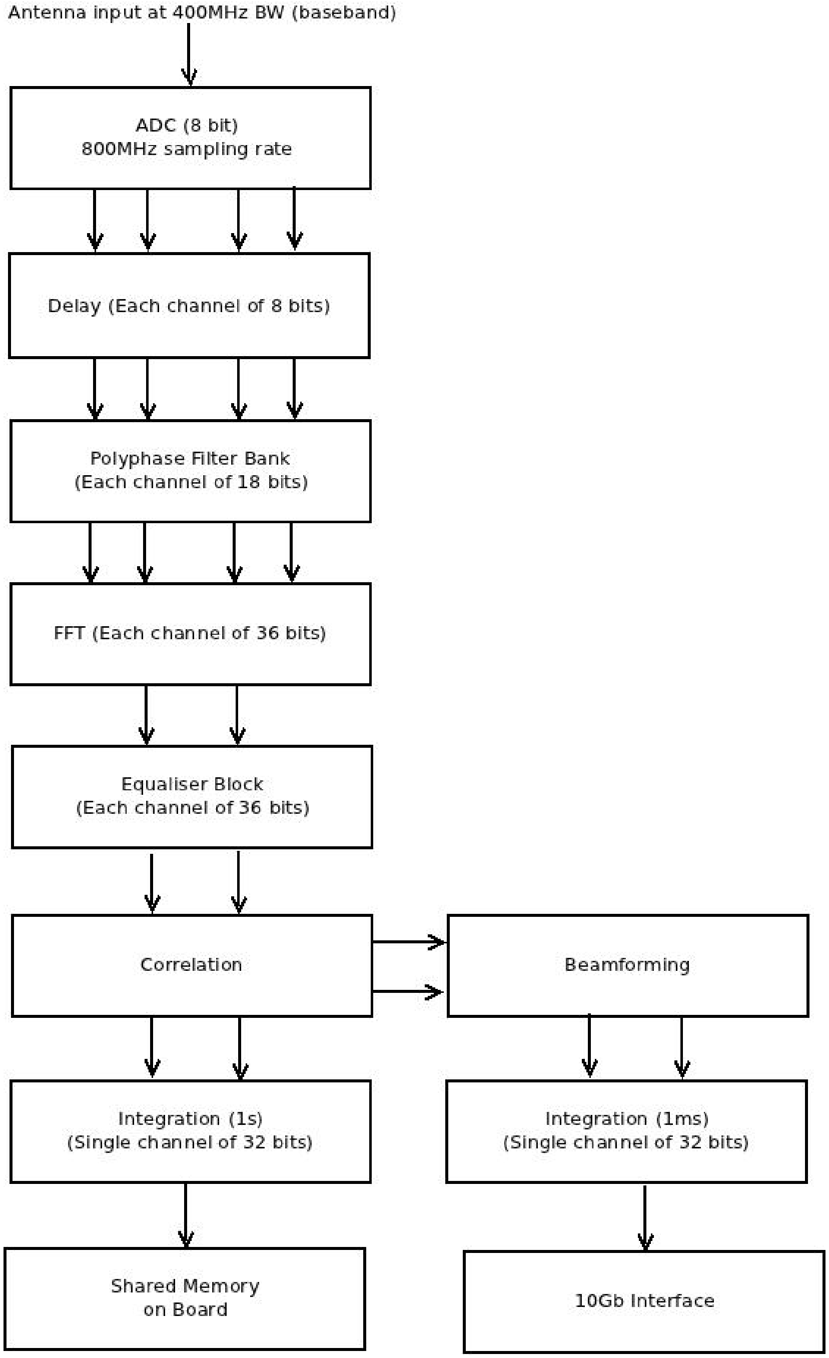

Antenna input at 400MHz BW (baseband)
ADC (8 bit)
800MHz sampling rate
Delay (Each channel of 8 bits)
Polyphase Filter Bank
(Each channel of 18 bits)
FFT (Each channel of 36 bits)
Equaliser Block
(Each channel of 36 bits)
Correlation
Beamforming
Integration (1s)
(Single channel of 32 bits)
Integration (1ms)
(Single channel of 32 bits)
Shared Memory
on Board
10Gb Interface

Figure 2.4: PoBe System Diagram

For two antenna incoherent beamforming, the mathematical expression given in Section 1.3 is referred: $B_i = \Sigma(V_1^2 + V_2^2)$. Similar logic is implemented on the ROACH. This is seen in the diagram below.

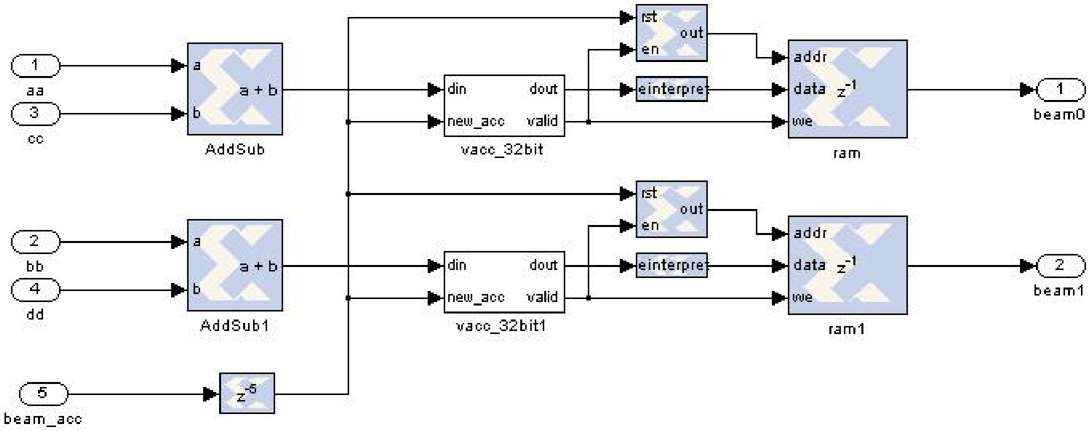


Figure 2.5: System Generator based incoherent beamforming design

In a general, this design is in threefold addition of power, integration and storing data onto a RAM. The following list defines each annotation:

- *aa* is channel V_1^2 (even)
- *cc* is channel V_2^2 (even)
- *bb* is channel V_1^2 (odd)
- *dd* is channel V_2^2 (odd)
- *beam_acc* is the synchronising clock particularly designed for the the beamformer
- *beam*0 is $V_1^2 + V_2^2$ (even)
- *beam*1 is $V_1^2 + V_2^2$ (odd)

From the *AddSub* block it can be seen that the addition of even channels and addition of odd channels are done separately. This output is then taken into the the integration or accumulation block: *vacc_32bit*. The integration block gives 32 bit with 6 binary point data and this is reinterpreted into 32 bit with 0 binary point before sending into the RAM. The RAM data is then packetised and sent to a 10G Ethernet cable at a short time integration.

For two antenna coherent beamforming, the equation, $B_c = \Sigma V_1^2 + 2V_1V_2 + V_2^2$, is referred. This is represented in System Generator as:

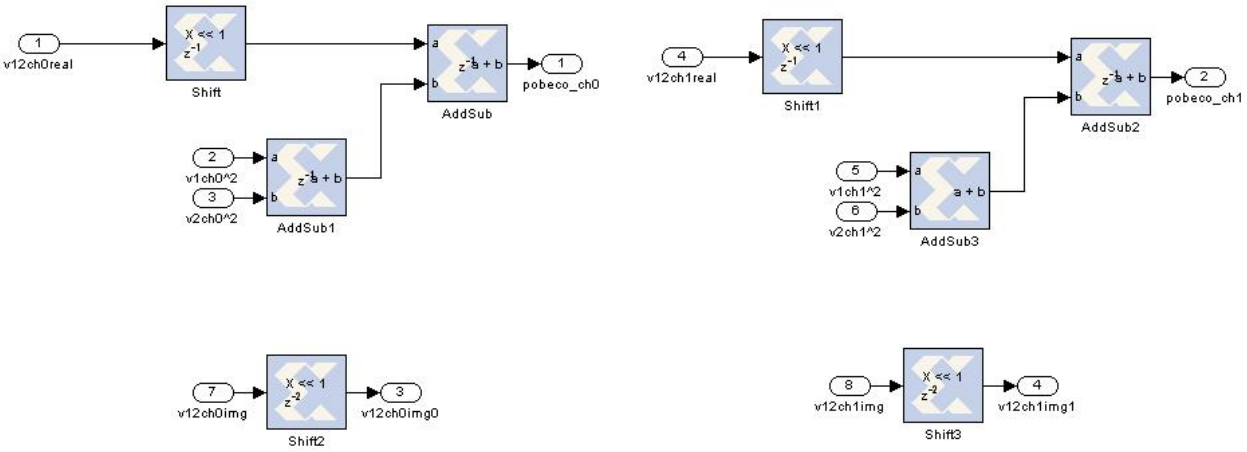


Figure 2.6: System Generator based coherent beamforming design

Before describing the logic, the labels are explained below:

- $v12ch0real$ is channel V_{12} (cross, even and real)
- $v1ch0^2$ is channel V_1^2 (self, even and real)
- $v2ch0^2$ is channel V_2^2 (self, even and real)
- $v12ch1real$ is channel V_{12} (cross, odd and real)
- $v1ch1^2$ is channel V_1^2 (self, odd and real)
- $v2ch1^2$ is channel V_2^2 (self, odd and real)
- $v12ch0img$ is channel V_{12} (cross, even and imaginary)
- $v12ch1img$ is channel V_{12} (cross, odd and imaginary)

Considering the system on the top left, the V_{12} (cross, even and real) is being left shifted by 1 bit which effectively translates to multiplying by 2. The output is added to another block which adds V_1^2 and V_2^2 (self, even and real) resulting in the the output being as $\Sigma(V_1^2 + 2V_1V_2 + V_2^2)$. The system on the top right does the same but for odd channels. The two systems are the even and odd channels of V_{12} (cross and imaginary) being left shifted by 1 bit. All the output of this system are sent to an integrator block and then packetised to be transfered via a 10G Ethernet card.

2.2.2 Synchronisation Clock

An essential requirement for beamforming is integrating for a shorter time span. Section 2.1 mentions that the synchronisation pulse of the PoCo design allows data transfer for 2^{27} clock cycles. As the PoBe is an add-on to the PoCo design, using this synchronisation pulse would result in an integration of only 0.89s. We can also get this by the calculation: $\frac{2^{27}\times 2}{300\times 10^6}$, where 2^{27} is the synchronisation pulse period, 2 is the number FFT channels and 300×10^6 is the operating frequency of the ROACH board. In order to reduce integration time, an alternate PoBe pulse is generated- *beam_acc*. The PoBe *beam_acc* is connected in parallel with the PoCo synchronisation pulse. This gives the PoBe design the ability to work independently from the PoCo synchronisation pulse and set its integration time via configurable register using a python script. However, tapping the data from the PoCo pulse constraints the PoBe design to have its integration time as a multiple of 2^{27}. A visual representation is shown below:

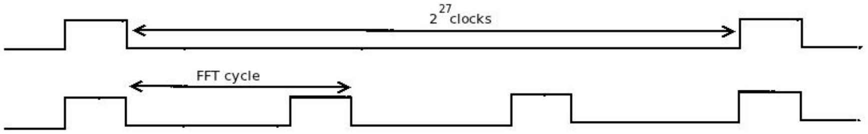


Figure 2.7: Comparison of PoCo Pulse and FFT Cycles

The concept behind the design of the beamformer pulse is heavily borrowed from the PoCo pulse. However, with modifications, the integration time can be adjusted to the required level. It must be noted that number of pulses in the second pulse train correspond to the number of FFT cycles. In fact, while setting the integration time, we are configuring the number of FFT cycles to the software register. Hence, the minimum integration that can be theoretically achieved is $\frac{1024}{300 \times 10^6} = 3.41 \mu s$. However, it is not optimal to operate at such low integration as only the output from the FFT data will be sent.

2.3 Packetised Design

The packetised design is required to assemble the data and transmit at fast integration rate over a 10Gb NIC. Before packetising data for high speed integration, it is necessary to packetise in such a way that we can also verify the functionality of the beamforming algorithm. The inital test packet was to used to test the incoherent beamformer. Thus, the packet stores V_1^2, V_2^2 and $V_1^2 + V_2^2$. It's design is as follows:

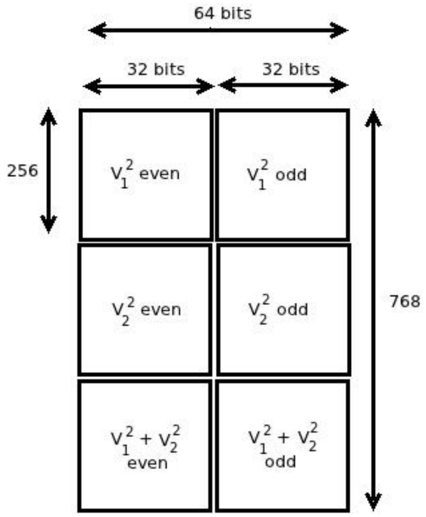


Figure 2.8: Incoherent Packet Design

From the packet dimensions, it can be calculated that the packet size is 64 × 768 = 49152 bits or 6144 bytes. This has been packetised in this format for two reasons. Firstly, for ease of depacketisation. This is because it easy to read the packet horizontally and as we move down the even-odd interleaving is done automatically. Secondly, by displaying V_1^2 and V_2^2 we can calculate offline if the addition $V_1^2 + V_2^2$ is taking place.

The packetised design for the 10G is a fairly complex system. This section will briefly describe the design. The data is concatenated before packetisation in the form of even and odd channels of 32 bit each and resulting in a 64 bit entity. The main block responsible for packaging the data is the FIFO. In the most basic sense the FIFO acts as a memory buffer which can read and write simultaneously. It works such that one 64 bit package is written in one clock and is read in the next immediate clock. This process continues until all 256 channels (of both even and odd) are formed in the packet shape as in Figure 2.7. For the three different, concatenated packages three different FIFOs are used. The 2nd FIFO is delayed by 256 clocks to increase the package depth by 256 bits and similarly the 3rd FIFO is delayed by 768 clocks to increase the package depth by 768. This results in the packet configuration as seen in Figure 2.7.

This packet design can be reused for coherent beamforming as well. The packet design will look as follows:

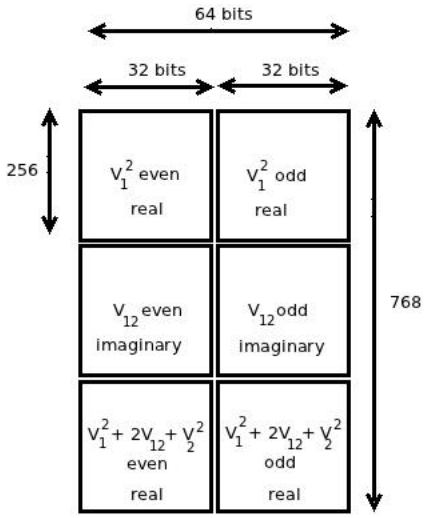


Figure 2.9: Coherent Packet Design

To alternate between incoherent and coherent designs, a multiplexer is placed before packetising. The multiplexer is configurable by a software register which gives the option of incoherent or coherent beamforming.

In case of incoherent beamforming, the packet shape can reduced. This is because V_1^2 and V_2^2 individually are not needed for beamforming. Hence the following desing has been implemented:

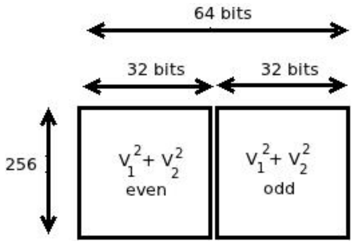


Figure 2.10: Incoherent Optimised Packet Design

The advantage of smaller packet is that it can reduce integration time as transferred data size is being reduced. Moreover, it saves resources on the FPGA and also makes depacketisation easier.

2.4 Resource Utilisation

In FPGA design, resources used are an important parameter to be considered. This tables below compare the PoBe modifications made on an PoCo in terms of resources utilised on the ROACH.

Parameter	Resources Used	Percentage
BUFGs	3 out of 32	9%
DCM_ADVs	2 out of 12	16%
DSP48Es	224 out of 640	35%
ILOGICs	9 out of 800	6%
External IOBs	65 out of 640	10%
External IOBMs	1 out of 320	1%
External IOBSs	1 out of 320	1%
OLOGICs	21 out of 8000	1%
RAMB18X2s	104 out of 244	42%
RAMB18X2s	104 out of 244	42%
RAMB36_EXPs	80 out of 244	32%
Slice Registers	27246 out of 58880	46%
Slice LUTS	20788 out of 58880	35%
Slice LUT-Flip Flop pairs	29468 out of 58880	50%

Table 2.1: PoCo Resource Utilisation on ROACH

Parameter	Resources Used	Percentage
BUFDSs	2 out of 8	25%
BUFGs	9 out of 32	28%
CRC64s	1 out of 16	6%
DCM_ADVs	2 out of 12	16%
DSP48Es	224 out of 640	35%
GTP_DUALs	8 out of 8	100%
ILOGICs	81 out of 800	10%
External IOBs	129 out of 640	20%
LOCed IOBs	129 out of 129	100%
External IOBMs	1 out of 320	1%
External IOBSs	1 out of 320	1%
External IPADs	36 out of 690	5%
OLOGICs	21 out of 800	2%
External OPADs	32 out of 32	100%
PLL_ADVs	2 out of 6	33%
RAMB18X2s	111 out of 244	45%
RAMB36SDP_EXPs	1 out of 244	1%
RAMB36_EXPs	87 out of 244	35%
Slice Registers	30441 out of 58880	51%
Slice LUTS	24189 out of 58880	41%
Slice LUT-Flip Flop pairs	34332 out of 58880	58%

Table 2.2: PoBe Resource Utilisation on ROACH

Chapter 3

Post Processing

This chapter explains processing after the data has left the FPGA. This includes packet capturing, depacketisation and performing dedispersion and folding.

3.1 Packet Capturing

Packet Caputuring is implemented by process of capturing data from a computer network. The standard packet analyser tool, Wireshark, has been used to verify the transfer of packets. This software gives valuable information such as rate of data transfer per packet (integration time), packet size along with various other attributes of the packet as it passes along the network. However, the actual utility for packet capture is GULP. This is an open source software which can read directly from the network interface and write to disk [6]. The packet caputuring capability of GULP is dependent on the data rate. A few data rate calculations give the following results:

- A 6K packet at 7 ms results in 7.02 Mbps data rate
- A 2K packet at 1.75 ms results in 9.36 Mbps data rate
- A 2K packet at 3.41 μs results in 4.8 Gbps

Experimentally, the maximum data rate that GULP was able to sustain was 9.36 Mbps. Furthermore, this if a 2K packet is sent through the 10G link at the lowest theoretical integration rate (3.41 μs), the packet grabber would need to capture packets at 4.8Gbps speed. Hence, an alternate packet capturing utility needs to be looked into to handle higher data rates.

3.2 Depacketisation

Depacketisation is the process of desegmenting the packet in order to make it compatible for further processing. This is done by basic ‘C’ programme. This program has three features:

- Unpacking the data. A packet of size 6144 bytes, is split into 3 packets of size 2048 bytes each. A packet of size 2048 remains unpacked.
- Converting unsigned 32 bit (FPGA output) to 16 bit short int. This is done to meet the compability of the dedispersion and fast folding software.
- Allows user to scale the data. This is done accordingly to meet compatibility of the dedispersion and fast folding software.

3.3 Dedispersion and Folding

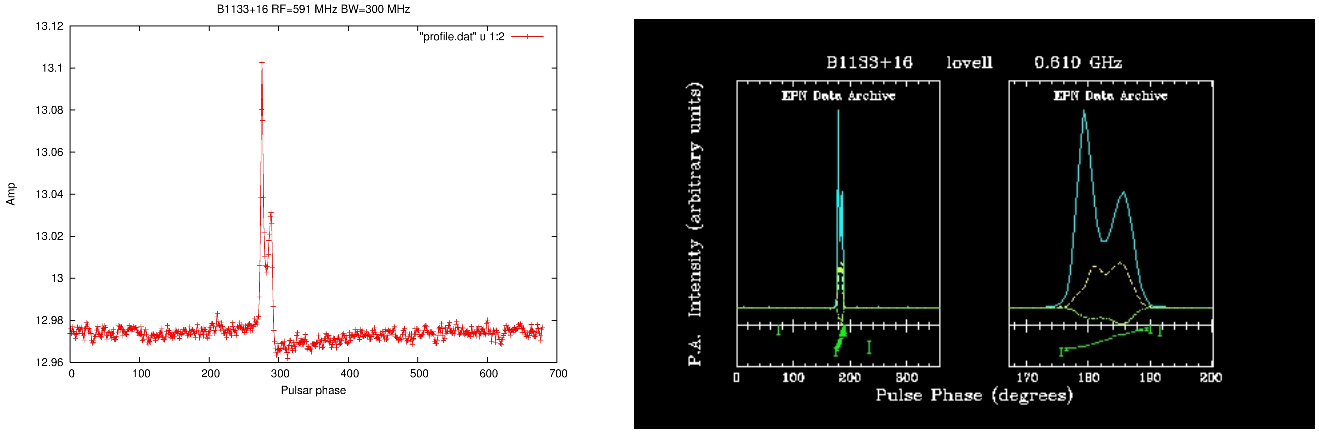
Taylor's dedispersion algorithm and the fast folding algorithm are analysis techniques designed for pulsar search commutation. The dedispersion algorithm is used to account for the delay caused by the interstellar medium while the fast folding technique requires collapsing the pulses in time series to obtain the pulsar peak well above the noise floor [7]. The final step of the offline processing is to enter the data on to a GMRT designed software which performs these algorithms on the data stream.

Chapter 4

Conclusion and Evaluation

4.1 Results

The Pocket Beamformer is a successful addition to the existing PoCo design. This is supported by various sky tests performed through the two antenna design for incoherent beamforming. The plot below shows the the pulsar profile of PSR B1133+16.



(a) PoBe Pulsar Profile of B31133+16

(b) EPN Pulsar Profile of B31133+16

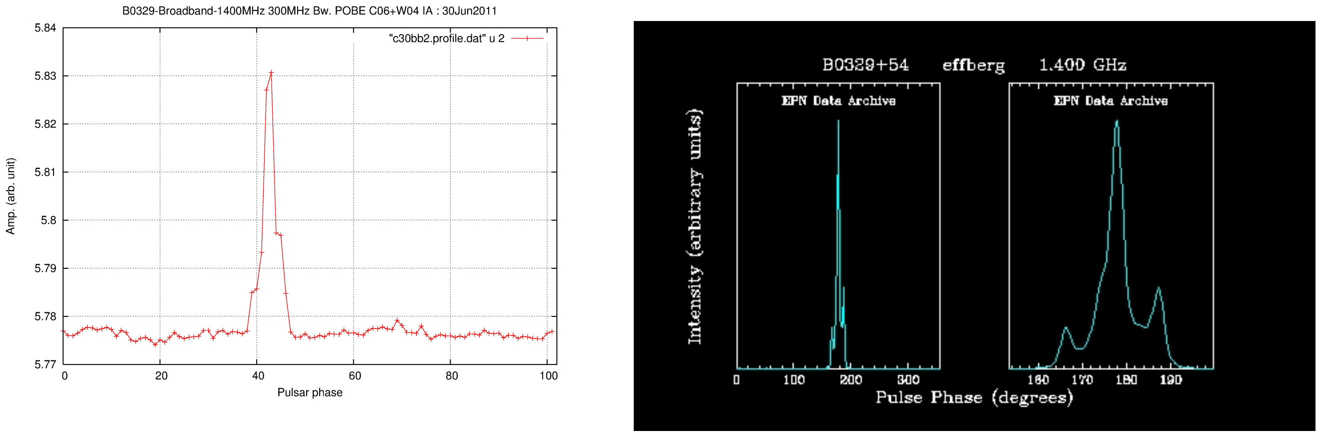
Figure 4.1: Pulsar Profile of B113+16

Observation Summary is given below:

- Name: PSR B1133+16
- Period: 1187.911536 ms
- Observation Frequency: 591 MHz
- Intermediate Frequency: 32 MHz
- Beamformer Frequency: 300 MHz
- Baseband LO: 51 MHz
- Integration time: 1.75 ms

- Maximum Channels: 512
- Date: 7 July 2011
- Time: 16:00-16:15 (IST)
- ALC: On
- No delay correction

The result is compared with the same pulsar from the European Pulsar Network (EPN) Database [8] in Figure 2.4 (b). Clearly, the results in agreement with the archived profile. In addition to this, the sky test for PSR B0329+54 shows similar results.



(a) PoBe Pulsar Profile of B0329+54

(b) EPN Pulsar Profile of B0329+54

Figure 4.2: Pulsar Profile of B0329+54

Observation Summary for B0329+54 is given below:

- Name: PSR B0329+54
- Period: 714.518664 ms
- Observation Frequency: 1400 MHz
- Intermediate Frequency: 100 MHz
- Beamformer Bandwidth: 300 MHz
- Integration time: 6.99 ms
- Maximum Channels: 512
- Date: 30 June 2011
- Time: 11:15-11:30 (IST)
- No delay correction

By comparing the plots we can conclude that the PoBe design is fully operationalfor inchorent beamforming. However, there have been some irregularities in the results as well. One such result is of B0329+54 is given below:

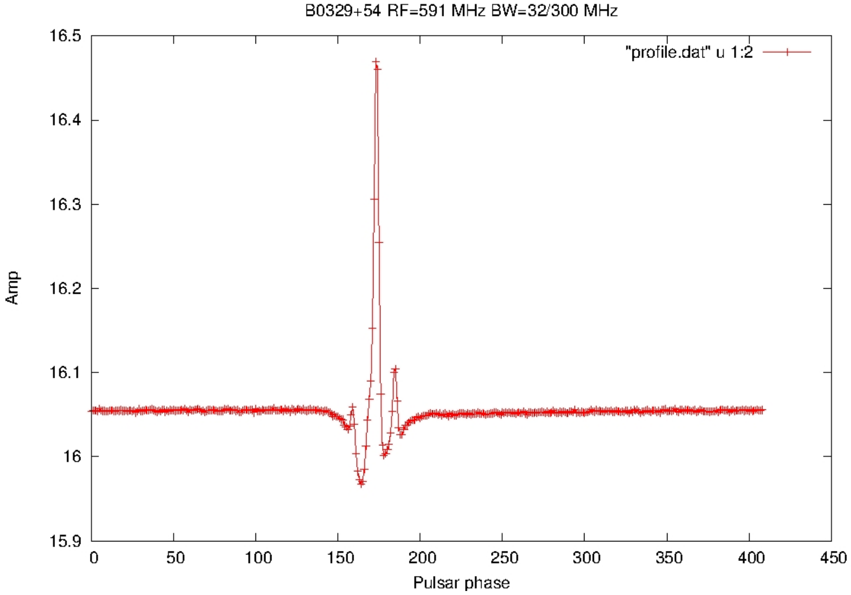


Figure 4.3: B0329+54 - Irregular Data

This data is an unusaul anomaly to the data. The secondary peaks of the pulsar are below the noise floor. The reason for this is still being sought after.

4.2 Evaluation and Future Scope

The PoBe design shows promising results and can be claimed to be a reliable system. This section will put forth the advantages of the PoBe and also suggest improvements to the digital system.

The advantages of the Pocket Beamformer are listed below:

1. The PoBe is a supplement to the PoCo design. This implies that both options of correlation and beamforming are available. This is a useful feature that can be used for troubleshooting if there any bugs in the latter part of the system.
2. The integration time for the PoBE is seperate from that of PoCo. This allows the Poco desing to integrate at 1s while the the PoBe can funtion independently at lower integration time.
3. Successful sky tests using incoherent beamforming algorithm

The list below points out weaknesses and suggests improvements to the PoBe design.

1. The Pocket Beamformer is limited to 1.75 ms integration, however theoretically it could go to $3.41\mu s$. This is because the packet grabbing utility-GULP cannot capture packets at such high speeds. It is suggested that we use an alternate utility that maximises the capability of the 10Gbps link.
2. The beamfomer with coherent design and four antenna design are yet to be tested with an actual source. Coherent beamforming will also require python scripts for coarse and fine delay correction.

3. In all sky tests, the ALC must be off. Otherwise, data near the noise floor maybe slightly disfigured as Figure 4.1. ALC must also be avoided because it could increase variation on the noise floor after folding.

In conclusion, the Pocket Beamformer is a dependable and useable design that could be used along side with the Pocket Correlator. This design finds its application in testing correlation between two antennas and at the same time is applicable for pulsar studies.

Appendix A

Source Code and Project Directory

Please find the DVD attached to the project. All source codes and files related to this work can be found on the DVD.

Appendix B

Equipments Used

B.1 ROACH specifications

- Xilinx Virtex 5 FPGA XCV5SX95 -1 ff1136
- PowerPC that runs Linux and controls the board
- 2 Quad Data Rate (QDR) and 1 DDR2 DIMM
- 2 Z-DOK connectors for ADC and CX4 connectors for high speed data transfer

B.2 Myricom Myri-10G network adapter specifications

- 10 Gigabit Ethernet with 10Gbps data transfer rate
- Full duplex capability and is compliant to IEEE 802.3x
- Processor Clock Speed- 300.0 MHz, RAM- 2.0 MB, Flash Memory- 512.0 KB

B.3 Host System Configuration

- Intel(R) Xeon(R) CPU X5550
- System Clock- 2.67GHz
- Memory- 8GB
- Manufacturer- Dell
- Operating System- CentOS 5.4

Below is a system level design of the setup.

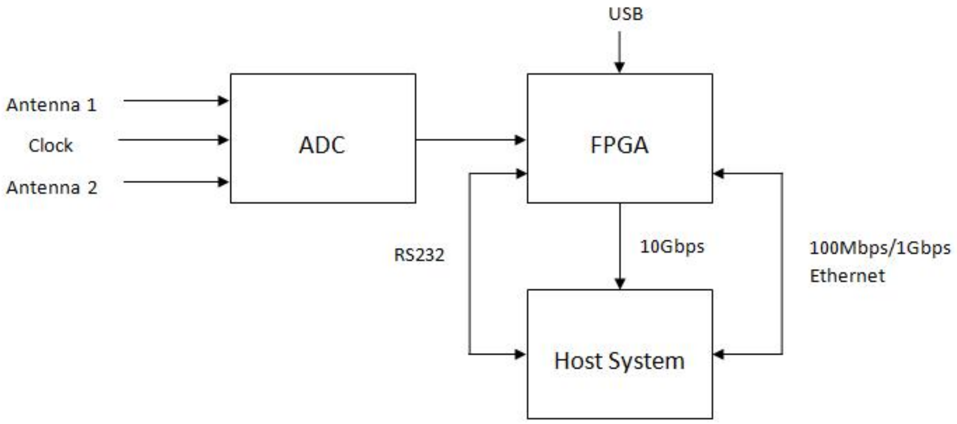


Figure B.1: Experimental Setup

From the figure the following details must be noted:

- The power input levels from the analog back-end or baseband systems are typically 12-14 dBm
- The ADC clock frequency runs at 600 MHz
- RS232 is a communication used to assign IP to the ROACH
- 100Mbps/1Gbps Ethernet cable is used to communicate with the PowerPC
- 10Gpbs link is used for high speed data transfer (faster integration)

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